Theory and Implementation of Time-interleaved Discrete-time Beamformers for Wideband Communications

Chung-Ching Lin, and Subhanshu Gupta
School of Electrical Engineering and Computer Science, Washington State University, Pullman, USA

***Abstract*—Efficient exploitation of wide bandwidth data communication requires antenna array providing high gain across all frequency components for both transmit and receive equipment. However, traditional phased array topology exhibits frequency dependent channel characteristic, leading to performance degrading in terms of beamforming gain and directionality across a wide range of band-of-interest. True-time-delay (TTD) arrays are appealing yet insufficiently investigated alternative for both fast initial access (IA) process and wideband directional data communications. In this work, the design tradeoff and considerations of implementation are first discussed. Then, a 4-element design is fabricated to show two different functions. During the IA process, large delay-bandwidth products are implemented to accelerate the overall process using frequency dependent probing beams. After the link is built, precise beam alignment is achieved to mitigate spatial effects during beamforming for wideband signals. Designed in a standard 65nm CMOS, the TTD spatial signal processor (SSP) successfully demonstrates unique frequency-to-angle mapping with 3.8ns maximum delay with 800MHz bandwidth in the beam-training mode. In the data communications mode, a 7.4% EVM with 614.4MB/s 16-QAM modulated signal.**

***Index Terms*—Wideband beamforming, true-time-delay, time interleaving, discrete-time signal processing.**

I. Introduction

Wideband beamformed yet energy-efficient solutions are highly desirable for next generation communication system to enable high speed data processing. State-of-the-art beamformed systems are, however, limited in the adoption of phase shifter [1], [2], in particular, the frequency-dependent response that sets a limit on their operational fractional bandwidth. TTD technique has been widely used to replace the phase shifter, striving to achieve beam-squint free data receiving, targeting for wide fractional bandwidth operations. Compared to most of the existing TTD approaches, baseband (BB) TTD using sample and hold circuit [3]–[5] has attract attentions owing to its compact, and digital friendly nature. Though operation mechanism, and measurement results have been domonstrated to prove the TTD effectiveness, the circuit design considerations and tradeoff analysis are rarely discussed. This paper aims to build the gaps from circuit/component parameter selection toward architecture scalability.

II. BB TTD and Equivalency to RF TTD

Consider a single channel of a beamformed system, the phase shifter compensation scheme is shown in Fig. 1(a),

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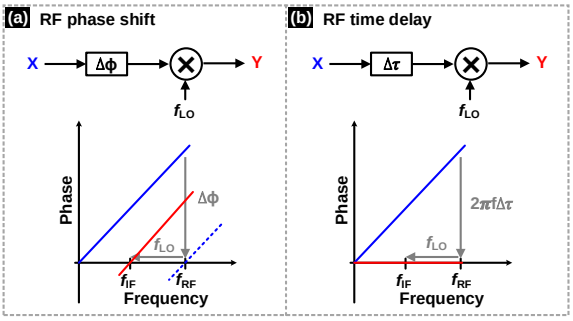

Fig. 1: Signal compensation at RF using (a) phase shifter; and (b) time delay unit.

causing beam squint on the band edges [3]. Intuitively, delay compensation happens at RF, however, several design challenges appears. First, scales the carrier frequency from sub-6-GHz to mmW bands limit the achievable delay range that a unit delay cell can provide. Second, the fine delay tuning (resolution) is hard to control at such high frequency. Third, as one move from one frequency to another, the cell has to be redesign to meet linearity, noise, power consumption specification.

Alternatively, compensation can be performed after the down-conversion, shown in Fig. 2 (a)-(c). Similar to the RF phase shift, the IF phase shift also experience beam squint due to non-constant phase response at the output, Y [6]. If we delay compensate at IF, the received signal Y can be expressed as:

$$\begin{aligned} Y &= X \times e^{-j2\pi f_{LO} t} \times e^{j2\pi(f - f_{LO}\Delta\tau)} \\ &= e^{j2\pi(f-f_{LO})t} \times e^{j2\pi(f\tau_n + f\Delta\tau - f_{LO}\Delta\tau)} \end{aligned} \tag{1}$$

where, $X = e^{j2\pi f(t+\tau_n)}$. Referring (1), zero phase condition only happens at a single frequency f_O with $\Delta\tau$ as:

$$\Delta\tau = -f_O/(f_{LO} + f_O) \times \tau_n \tag{2}$$

This results indicates that the applying a delay at IF only is insufficient and introduces beam squint eventually. To solve the beam squint issue, an additional phase shift is required as shown in Fig. 2(c). The received signal with both phase shift and time delay at IF is expressed as:

$$Y = X \times e^{-j2\pi f_{LO} t} \times e^{j2\pi(f - f_{LO}\Delta\tau)} \times e^{-j\Delta\phi} \tag{3}$$

A frequency-independent output is obtained by combining both IF delay ($\Delta\tau = -\tau_n$) and phase shift ($\Delta\phi = 2\pi(f - f_{LO}) \times \tau_n$) [6]. Furthermore, the phase shift can be moved to the LO side, further simplifying the design of the signal chain. The aforementioned explanation indicates the IF time delay with a corresponding phase shift has an ability to align the phase not only at the single frequency but also at the

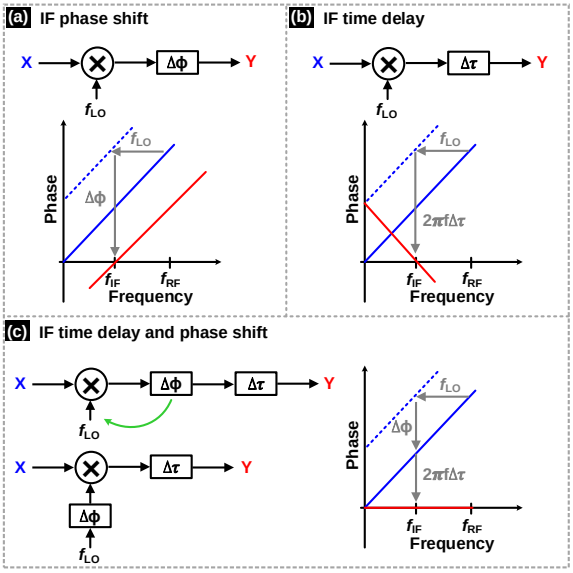

Fig. 2: Signal compensation at IF with (a) phase shift; (b) time delay; and (c) time delay with phase shift.

band edges of the received signal. This key conclusion opens new opportunities to implement large delay range-to-resolution ratio in the baseband. In Section-III, we will analyze and discuss a beamforming architecture that use the baseband delay in the implementation.

III. Analysis and Implementation of Interleaved Switched Capacitor TTD Array

Discrete time delay unit has been widely used for its wide achievable delay range capability and its possible implementations are illustrated in Fig. 3(a)-(d) using switched capacitor circuits. Shown in Fig. 3(a), the key concept to create the delay is to sample a continuous time signal (under Nyquist theorem) and store the sample into the capacitor (i.e.,C_S). Then, by controlling the releasing time of the second switch (right) to transfer the charge to the subsequent stages. A longer delay is feasible to achieve by cascading multiple of the circuits in Fig. 3(a) and constructs as Fig. 3(b). However, additional loss is introduced due to several series sampler [7]. The interleaved sampler [3] is shown in Fig. 3(c). The effective delay is determined by the number of interleaving levels. Nevertheless, the parasitic capacitance (i.e., contribute by the two switches) at the top plate of C_S which degrades the signal-to-noise-and-distortion ratio (SNDR). An improved version with additional two switches are shown in Fig. 3(d), which mitigates the parasitic effect with improved SNDR performance [5].

A. Time-interleaved design tradeoff analysis

Figure 4 shows a generic architecture for implementing N element basedband TTD SSP based on the TI- parasitic insensitive sampler and its design tradeoff analysis is also described here. In the subsequent section, the inclusion of the input buffer, summer design requirement, and the stray capacitance effect at the summer virtual node will be covered. The input buffer is essential in implementing TTD circuits for two reasons. First, since the TTD implementation is based on switches and capacitor, the time constant of the input

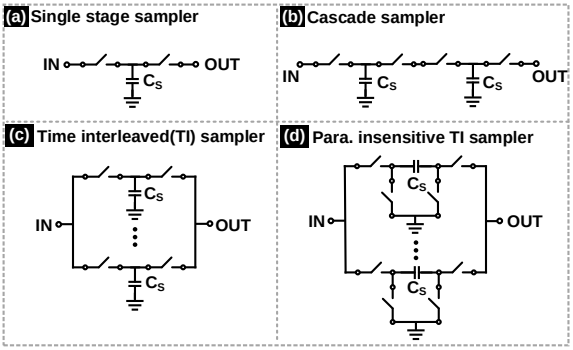

Fig. 3: Various approaches of time delay unit design using switched capacitor circuits

impedance, on-resistance, and sampling capacitor determines the input network time constant. More importantly, the input impedance and the switch on-resistance are connected in series, its magnitude need to be minimized. Second, similar to any sample-and-hold system, the switching behavior introduces the residual charge throwing back to the input signal. This undesired phenomenon also known as "kick-back", that need to be minimized. Thus, a source follower is usually adopted because of its high impedance, and low output impedance which is inversely proportional to the input transistor trans-conductance, thus posing a tradeoff with the power consumption.

The noise performance of the switched capacitor delay cell is determined by the thermal noise from the sampling capacitor. Thus, the design procedures can be summarized as the following:

1) Choose the sampling capacitor such that its thermal noise power level is less than quantization noise for a given resolution.
2) Size the switch on-resistance such that its time constant with the sampling capacitor in which the settling error (ϵ) is less than a certain level. For instance, for a 10-bit design with an ϵ less than 0.25LSB, the required time constant is required to be larger than 8.3X of the inverse of the bandwidth-of-interest.
3) Plug the initial value to the simulator to perform transistor-level simulation and adjust the values if needed.

As suggested, a larger sampling capacitor introduces less noise, but suffers from a reduced bandwidth. One may wonder if it's feasible to enlarge the transistor size to scale down the on-resistance. However, the associated junction capacitance starts to attribute nonlinear component, causing undesired distortion. The noise-bandwidth relationship indicates another tradeoff here.

After the signal at each of the channel got delayed properly, the summer plays a role in transferring the charges to the output stages through a capacitive feedback amplifier. Assume the N number of channels with a feedback capacitor of C_F, a feedback factor of $C_F/(C_F+NC_S)$ can be calculated. With a open loop bandwidth of BW_O, the closed-loop summer bandwidth will be its BW_O divided by its feedback factor. This important results indicates for a larger number of array size, the

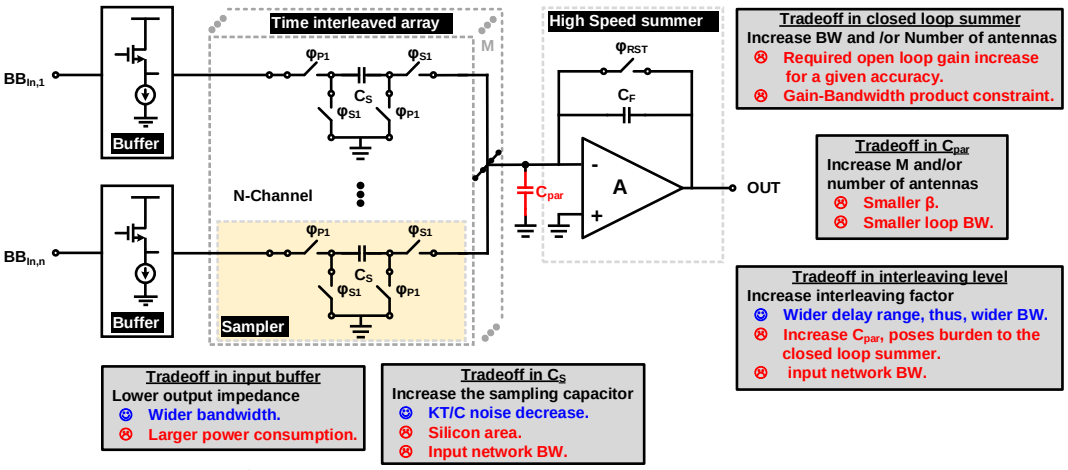

Fig. 4: Generic TTD SSP architecture and its design tradeoff

bandwidth requirement increases proportionally. Additionally, amplifier design in general falls into gain-bandwidth product constraint. To break this constraint, advanced techniques with extra power consumption and silicon area are required.

Care must be paid to minimize the parasitic capacitance C_{par} at the virtual node of the summer amplifier. The C_{par} is contributed by the summer input capacitor, switch junction capacitor, and routing. The latter one is more substantially when a large number of M (i.e., a longer achievable delay range) is implemented. A large C_{par} deteriorates the closed loop bandwidth, poses challenges for the summer design.

B. Prototype implementation

In this section, a 4-channel prototype is implemented considering the tradeoff in section-III-(A). The architecture for the proposed 4-element TTD SSP is shown in Fig. 5(a). To sum the aligned signals, a ring-amplifier is used for signal combining. An interleaving factor of 7 was chosen to cover a large delay range while meeting the Nyquist rate sampling requirements of a wideband signal. Figure 5(b) shows the simplified timing diagram. The delay compensation technique only requires digital logic, switches, and capacitors which can be well integrated in CMOS technology and benefit from process scaling. Each interleaved level has a conversion speed of roughly 228MHz (1.6GHz/7). The SCA uses 50fF sampling capacitor and sized transmission gates for the switches in each path due to the common mode voltage being at roughly half the supply. Interested readers can refer to [5] for more detailed circuit design description.

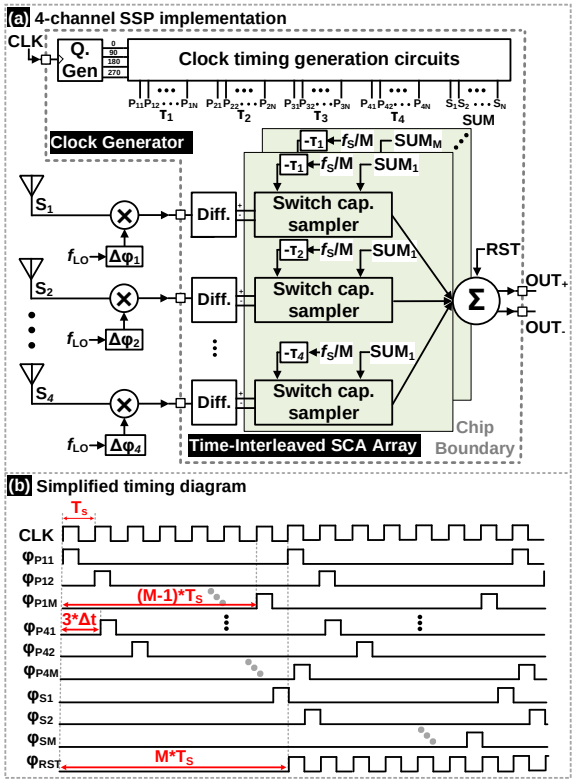

Fig. 5: (a) 4-channel SSP implementation and; (b) its timing diagram

IV. Measurement Results

The silicon implementation of the proposed SSP was fabricated in 65nm CMOS occupying 1.98mm^2 area including pads as shown in Fig. 6. Figure. 6 also shows the simplified test setup with the device-under-test (DUT) and the Xilinx FPGA. To prove the concept in [8], the input signals of TTD IC are generated by FPGA to emulate the OFDM symbols received by a critically spaced 60GHz linear array, followed by down-conversion to intermediate frequency at 491.32MHz. Fig. 7 presents the power spectral density (PSD) to 9 different incidence angles θ, indicating the unknown incident angle θ can be identified by analyzing the frequency response of the array upon receiving a wideband pilot symbol, thanks to the TTD frequency-dependent antenna weight vector. The procedure accelerate beam training by avoiding the sequential switching-measuring as required by conventional method.

Different testing methods are performed to characterize the SSP in the communication mode as shown in Fig. 8(a)-(d). Figure 8(a) shows a ∼12dB frequency-independent beamforming gain for a 720MHz wide bandwidth with four channels enabled demonstrating delay compensation with RAMP based signal combiner. The off-chip bandpass filter with 70MHz 3-dB high-pass corner attenuates the gain at lower frequencies. At higher frequencies, the observed gain roll-off is due to amplifiers in the ZCU216 RF-ADC. Error vector magnitude (EVM) measurement with 30.8Mb/s 4-QAM signal

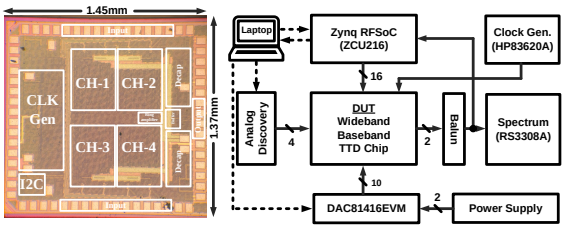

Fig. 6: Die photo and simplified test setup

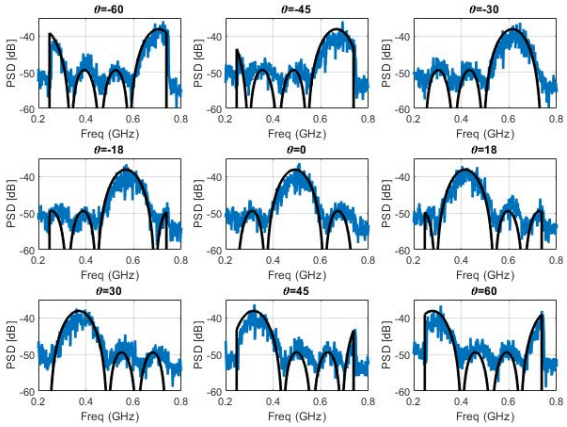

Fig. 7: Measured beam training power spectral density (PSD) against theoretical results.

and 614.4Mb/s 16-QAM signal are fed into the SSP for data communications performance evaluation. An EVM of 5.2% and 7.3% are obtained with four channels enabled as shown in Fig. 8(c)(d). The results can be further improved as the loss in the on-chip output buffer is decoupled. Table I summarizes the critical parameters for the proposed TTD SSP and compares with state-of-the-art. The proposed work has the ability to connect with different RF and mmWave front end downconverters relaxing the overall system design complexity for TTD arrays.

V. Conclusions

This paper analyzes the design considerations and tradeoff in implementing the TTD SSP. Base on the analysis, a prototype is fabricated in 65-nm CMOS process to demonstrate the fast beam-training algorithm for TTD arrays leveraging frequency-dependent search beams to sound all directions simultaneously which reduces beam training latency substantially. Furthermore, the proposed architecture supports wideband data communications for efficient signal combining in the baseband switched-capacitor array. A 3.8ns delay compensation across 800MHz bandwidth is demonstrated with EVM of $< 10\%$ supporting 16-QAM modulated signal.

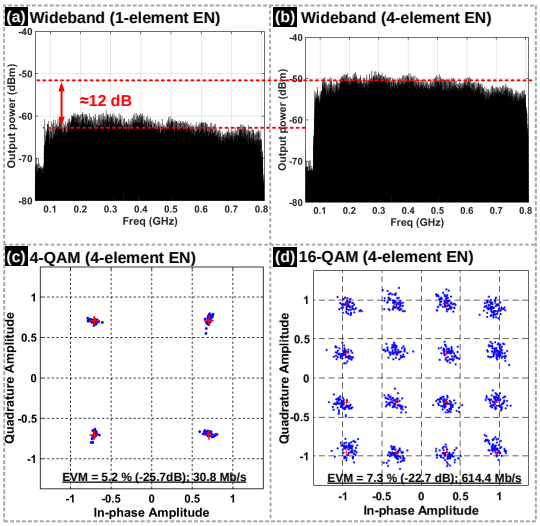

Fig. 8: Wideband signal measurement

TABLE I: Comparison to prior-art 4-element SSP.

Parameters	[9]	[3]	[7]	[10]	This work
Method	BB-TTD	BB-TTD	BB-TTD	RF-TTD	BB-TTD
# of Elements	4	4	4	4	4
Domain	Charge	Charge	Time	Charge	Charge
BW (MHz)	100	100	500	800	800
Delay range (ns)	10	15	1	5	3.8
Digital intensive	Yes	No	Yes	Yes	Yes
Beamtraining	No	No	No	No	Yes
Power(mW)	70*	52	40†	70	29§
Area (mm^2)	0.5*	0.82	0.9	1.2	1.98♯
Technology (nm)	65	65	65	28	65

*Baseband delay, mixers, and LO; †incl. ADC power; §excl. test buffers; ♯incl. vector modulator

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