A $2V_{pk\text{-}pk,diff}$ Input Range 1GS/s Voltage-to-Time Converter with Tunable Distortion Compensation

Chase Puglisi, Erfan Ghaderi, Shrestha Bansal, George Larue, and Subhanshu Gupta
School of Electrical Engineering and Computer Sciences
Washington State University
Pullman, United States
chase.puglisi@wsu.edu

***Abstract*—Next generation 5G standards operating at sub-6GHz and millimeter-wave frequencies place stringent requirements on the design of analog-to-digital converters (ADCs) via conversion speed, ENOB, and power consumption. The reduction of supply voltages through increasingly scaled CMOS process nodes further complicates the design process of these circuits. This work presents a 1GS/s sampling based voltage-to-time converter (VTC) in 65nm process with full $2V_{pk\text{-}pk,diff}$ input range at only 1mW power consumption. We propose a method for tunable distortion compensation across corners to realize a truly robust design. The proposed design has a low frequency figure-of-merit (FOM) of 3.8 fj/conv-step and a high frequency FOM of 2.46 fj/conv-step. The performance of VTC enables realization of time-to-digital converters (TDC) with high resolutions.**

Keywords— Voltage-to-time converter, VTC, time-to-digital converter, TDC, distortion compensation.

I. Introduction

Next generation wireless communication offers the potential of increased data rates harnessing larger bandwidths at sub-6GHz and millimeter-wave (mmWave) frequencies. However, resolving signals with large modulated bandwidths at the baseband requires the use of giga-bit-per-second ADCs. consuming minimal power while providing sufficiently linear multi-bit conversions. As supply voltages shrink in scaled CMOS process nodes, maintaining large dynamic range and hence achieve large signal-to-noise ratio (SNR) in the ADC have become increasingly more difficult. Reducing the available analog voltage headroom results in a loss of SNR which limits the achievable linearity of these ADCs. While analog design techniques are available to the designer to overcome these SNR limitations, such as gain-boosted op-amps and pole cancellation, they only increase the complexity of conventional designs resulting in increased power consumption and die area. Therefore, new design techniques should be considered.

Time-based circuits, on the other hand, benefit tremendously from short channel lengths via increased switching speeds and lower dynamic power consumption. These circuits have thus become increasingly more attractive with scaled CMOS process nodes. As shown in Fig. 1, the voltage-to-time-to-digital process is as follows. First, the analog signal is sampled. Then each sample is converted to a corresponding time pulse for the subsequent TDC to quantize with picosecond resolution [1]. To practically implement a time-based analog circuit, there is a need to first convert the analog voltage to a series of equivalent time pulses. This conversion is done though the voltage-to-time converter (VTC). The VTC is an important circuit block that should ideally be low power with large dynamic range to not limit the performance of subsequent circuits, such as the time-to-digital converter (TDC).

Input voltage range has proved to be a limitation in the design for recent VTC's in sub-micron CMOS processes. In [2]-[4], the input voltage range is limited due to biasing requirements of the current source along with input frequency limitations caused by variations at the input before a conversion is made. The gate of the current source transistor also serves as the signal input. This limits overall input voltage range to 240mV differential to ensure that the current source remains in saturation for the given bias voltage. In [5], the architecture is a sample-and-hold, NOR gate-based comparator. The input voltage has been increased to 1000mV peak-to-peak differential but exhibits linearity problems with low input voltage values due to the discharging current source falling out of saturation. The sample-and-hold configuration allows for relatively constant linearity over the entire input frequency range as well. While this method resolves issues that are present in the case of current-starved inverter based VTCs, it suffers from increased power consumption (8mW) due to static power consumption of the current source even when it is not being used for discharge.

This work presents an improved design inspired by sample-and-hold VTC in [5] to achieve reduced power consumption and with maximum input voltage range of $2V_{pk\text{-}pk,diff}$ without losing achievable linearity. We achieve this through non-linear, low power, initial voltage-to-time conversion where linearity lost in voltage-to-time conversion is recovered through a variable gain time-amplifier (TA) capable of optimizing achievable signal-to-noise-and-distortion (SNDR) ratio across corners. By minimizing the distortion in the time domain rather than at the input of the VTC, power is saved, and we are fully taking advantage of the benefits that digital circuits see in sub-micron processes.

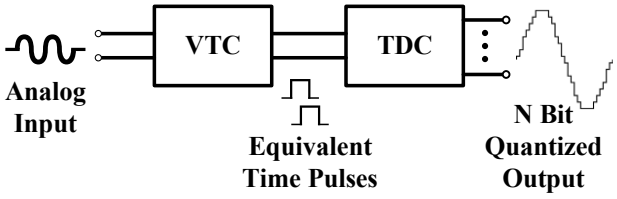

Fig. 1. Block diagram of a voltage-to-time-to-digital converter.

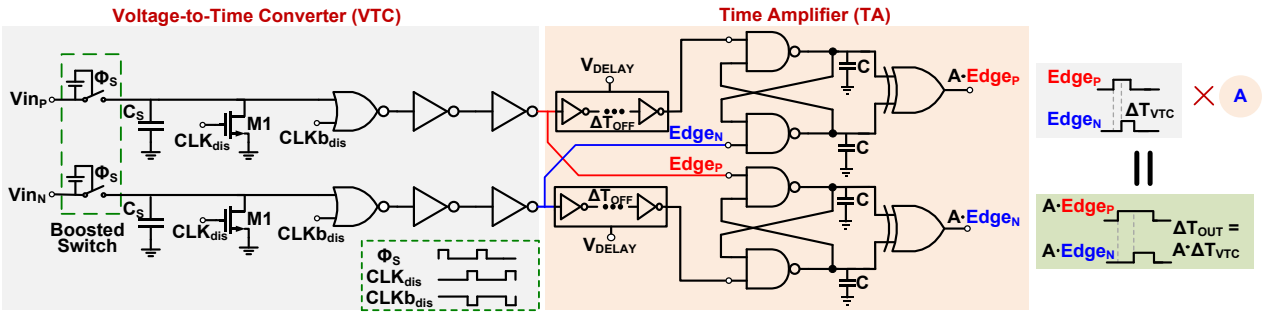

Fig. 2. Circuit diagram of the proposed VTC + TA. The initial conversion, ΔT_{VTC}, is then compensated through the TA by tuning ΔT_{OFF} to realize the final output delay ΔT_{OUT}. Gain is generated by introducing a delay of ΔT_{OFF} through a chain of current starved inverters with control voltage V_{DELAY}.

The remainder of the paper is as follows: Section II describes circuit design and analysis where the linearity recovery technique will be highlighted. Section III presents simulation results where the linearity compensation technique is validated. Section IV presents the conclusions.

II. Circuit Design and Analysis

A. Proposed VTC + TA Architecture

The proposed circuit design architecture is illustrated in Fig. 2. The architecture is a pseudo-differential configuration where each parallel path contains a bootstrapped sampling switch, capacitor, a discharge path, and a NOR gate based comparator. For a 1V supply, $Vin_{N/P}$ are biased at 500mV (V_{CM}) so the input can swing rail to rail. During the sample phase, Φ_S, input voltage $Vin_{P/N}$ is stored on the sample capacitor C_S. Then in the evaluation phase, CLK_{dis}, the sample capacitor is discharged through M_1 and a rising edge is triggered when the voltage reaches the switching threshold of the comparator to generate the respective $Edge_P$ and $Edge_N$ pulses. In [5], the large static current consumption of the current source in the sample phase resulted in poor energy efficiency with the VTC consuming 8mW while operating at 4GHz. By removing the current source, power can be saved, and input voltage swing can be maximized. However, removing the current source now requires M_1 to drive the sampled value to ground. This results in a large non-linear discharge current due to channel length modulation of the minimum length M_1 device leading to significant distortion in the output time pulses.

Each output pulse is then sent to an SR-Latch based TA described in [6] to compensate for the harmonic distortion that is introduced by the non-linear voltage-to-time conversion of the VTC.

B. Distortion Compensation

Before describing the method of compensation, it is useful to understand the cause of the non-linearity of the initial conversion. As previously mentioned, without a constant current source to discharge the sampled voltage, we must rely on M_1 to do so. Ideally, the time it takes to discharge the sampled voltage can be written as:

$$t_{discharge} = \frac{C_S V_{in}}{I_D} \tag{1}$$

where C_S is the sample capacitor, V_{IN} is the sampled voltage, and I_D drain current of M1. Once C_S discharges, a rising edge is triggered at the NOR gate comparator. Assuming the device in the positive path is in saturation region during discharge for large input voltage values, and the device in the negative path is in linear operation during discharge, the delay from the rising edge of CLK_{DIS} to the rising edge, $Edge_{P/N}$, can be modeled using the following equation:

$$Edge_P = \frac{C_S(V_{cm}+V_{in})}{I_{SAT}(1+\lambda(V_{cm}+V_{in}))} + 2t_{inv} \tag{2}$$

$$Edge_N = \frac{C_S(V_{cm}-V_{in})}{I_{LIN}} + 2t_{inv} \tag{3}$$

where I_{SAT} is the current when M1 is in saturation region, I_{LIN} is the current when M1 is in linear region, t_{inv} is the propagation delay of each inverter that follows the VTC, and λ is the channel length modulation parameter. Using (2) and (3) the overall differential output can be defined:

$$\Delta T_{VTC} = \frac{\frac{C_S}{I_{SAT}}(V_{in}+V_{cm}) - \frac{C_S}{I_{LIN}}(V_{cm}-V_{in})\psi}{\psi} \tag{4}$$

where $\psi = (1+\lambda(V_{cm}+V_{in}))$. From (4), assuming all values are constant except for V_{IN}, an equation of this form compresses for large values of V_{IN}. Using a Taylor Series expansion of (1) and negating even ordered terms due to a differential implementation, ΔT_{VTC} can be approximated as:

$$\Delta T_{VTC} \approx \frac{C_S}{I_D} V_{in} - \beta V_{in}^3 \tag{5}$$

where β is the third order non-linearity coefficient given from the Taylor Series equation. This approximation is illustrated in Fig. 3 by comparing both (4) and (5) for a given parameter set.

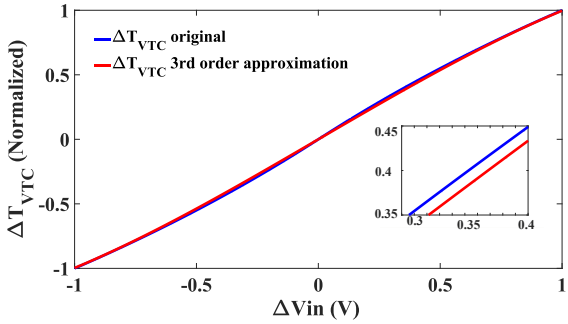

Fig. 3. Distortion modeling of equations (4) and (5) for the pseudo-differential VTC model.

One method to reduce the contribution of the third harmonic term is to compensate it with another circuit that exhibits an expansive characteristic for large input values. An expansive characteristic would include a positive signed third ordered term where in (5), it is negative. The time amplifier (TA) described in [6] has just this characteristic. When the TA is operating in its respective stable region, for large input time pulses, the output begins to expand. By properly controlling the severity of this expansion, the third order distortion introduced by the VTC can be compensated. To do so, some sort of controllability needed to be introduced into the TA. From [6] the small signal gain of the TA can be controlled through a delay line ΔT_{OFF}. By implementing a current starved inverter chain with control voltage, V_{DELAY}, prior to the TA (as shown in Fig. 2), direct access to controlling the small signal gain of the TA can be achieved. This gives direct control of the third-order coefficient of the TA which allows for minimization of the overall third-order component of the VTC + TA. Balancing the TA with the VTC to achieve minimal distortion was done through a circuit simulation-based approach. A visualization of this method can be seen in Fig. 4.

While this method increases the complexity of the overall VTC design, a sufficiently linear circuit can be realized without the need of a constant current source that consumes power even when it is not being used. This is beneficial in terms of power consumption, linearity, and input voltage range. By handling the linearity problem with a digital circuit rather than a constant current source in the voltage domain, power can be saved. This also benefits us because a point of controllability has been introduced to the circuit which allows for potential closed loop optimization schemes to be developed that are not present in any previous VTC works, bringing this circuit one step closer to being practical in the real world. However, the drawback of this method is that for a given value of ΔT_{OFF}, overall output time range of the converter has now been limited to the stable region of operation of the TA as described in [6].

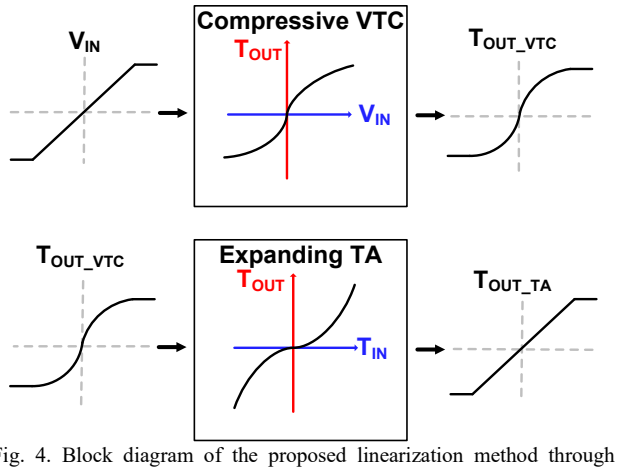

Fig. 4. Block diagram of the proposed linearization method through minimization of the third order distortion coefficient. By cascading the compressive characteristic of the VTC with the expanding characteristic of the TA, a linear transfer characteristic from V_{IN} to T_{OUT} can be

III. Simulation Results

The VTC and TA have been designed in the TSMC 65nm CMOS process. Both spectrum and transient analysis have been done using the edge cross method as described in [5].

A. Voltage Input Range

By removing the discharge current source, there is no limitation on input voltage range. Even when the sampled voltage is initially below the switching threshold of the comparator, a unique output delay is still present for input values all the way down to ground. This is due to a different initial output charging current of the comparator for a given voltage less than the switching threshold of the comparator. However, this introduces significant distortion at the output of the VTC. But, by tuning the gain of the TA through the control voltage, V_{DELAY}, output distortion can be suppressed significantly as shown in Fig. 5. Before compensation, the output spectrum contains every odd order harmonic with the third and fifth harmonic being the most prominent. However, after distortion compensation, the third harmonic is reduced by 34dB and the fifth harmonic by 13dB while higher order harmonics remained unchanged.

Fig. 6 offers insight into how the distortion compensation affects the overall transfer characteristic of the VTC + TA. By cascading the VTC and the TA, the overall transfer characteristic is shown to be linear over the entire available voltage compared to the individual transfer characteristics of each block.

B. Maximum Input Frequency

Bootstrapping the input sampling switch was utilized to maintain the linearity at high input frequencies. The current starved inverter based VTCs as previously mentioned do not utilize a sample-and-hold circuit which results in significant

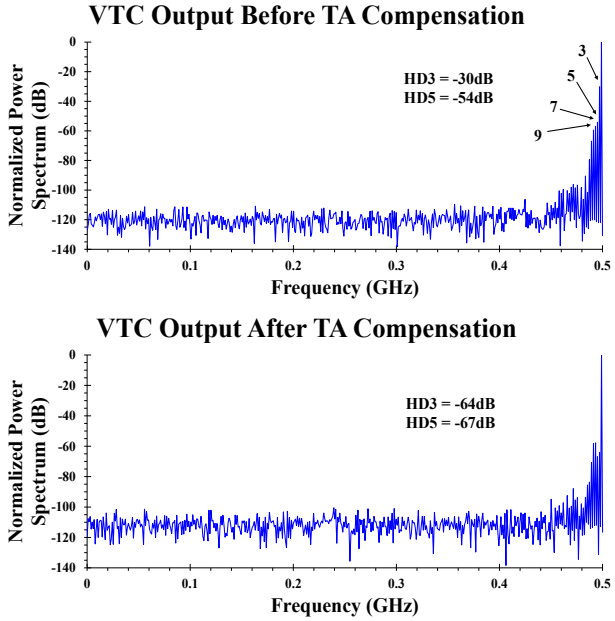

Fig. 5. Output spectrum of ΔT_{VTC} (top) prior to compensation and of ΔT_{OUT} (bottom) after distortion compensation in the typical corner. Nyquist input frequency (~500MHz) with full scale input of 2Vpk-pk differential.

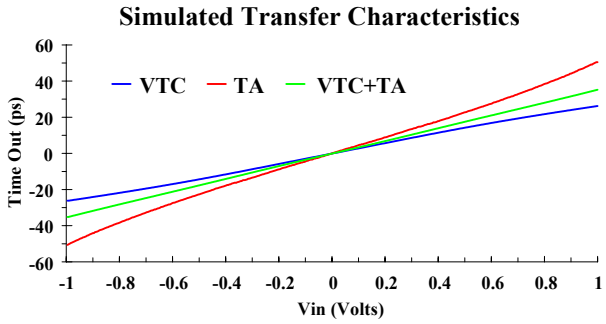

Fig. 6. Simulated transfer characteristic of the VTC (blue), TA (red), and the combined characteristic of the VTC + TA (green).

SFDR variation across input frequency. Fig. 7 shows the SNDR the gain of the TA via V_{DELAY}. For all cases, overall SNDR performance of the proposed VTC+TA is shown across corners. For each corner, the output of the VTC+TA was optimized through tuning the TA gain, resulting in better than 50dB SNDR from low frequency input all the way up to Nyquist. Additionally, the SNDR remains linear from low to high input frequency with less than 1.2dB of variation with respect to each corner.

Table I compares the proposed VTC + TA with the recent state-of-the-art. The VTC + TA implementation achieves full differential voltage input range of $2V_{pk\text{-}pk,diff}$ while only consuming 1.1mW of power. This maximizes overall signal-to-noise ratio, which benefits subsequent stages that would follow the VTC + TA, such as a TDC. The distortion compensation method achieves a final worst case ENOB of 8.2 bit with 34dB third harmonic suppression at the typical corner. Implementing the tunable delay chain comes at minimal area cost too, as only 4 additional inverters were required for each differential channel with a delay range from 25ps to 80ps over the available tuning voltage range of 500mV to 1V. Because this circuit is to be utilized in conjunction with a TDC, it is necessary to utilize the Walden figure-of-merit (FOM) for ADC performance. This results in an FOM of 3.8 fJ/conv-step at low frequency and 2.46 fJ/conv-step at high frequency input, which is comparable to state-of-the-art.

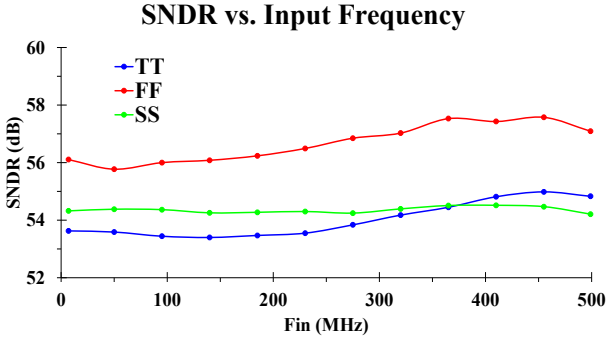

Fig. 7. SNDR across input frequency for each corner. Input voltage was help constant at 2V differential while the delay T_{OFF} was optimized for each corner.

TABLE I. COMPARISON WITH RECENT STATE-OF-THE-ART.

	[2]	[3]	[4]	[5]	This Work
Year	2016	2013	2017	2016	2019
Technology	130nm	NR[a]	65nm	65nm	65nm
Supply Voltage (V)	1	NR[a]	1.2	1V	1V
Input Range ($mV_{pk\text{-}pk}$)	240 (diff)	150	1000	1000 (diff)	2000 (diff)
Sample Rate (GS/s)	0.001	4	5	4	1
ENOB (bit)	NR[a]	6	NR[a]	7.6	8.2
Time Output Range (ps)	451* 10^3	23	102	126 (diff)	70 (diff)
Power (mW)	668* 10^{-6}	NR[a]	477* 10^{-3}	8	1.1
FOM @LF (fJ/conv-step)	NR[a]	NR[a]	NR[a]	NR[a]	3.88
FOM @HF (fJ/conv-step)	11.6* 10^3	NR[a]	52	10.3	2.46

[a]Not Reported

IV. CONCLUSIONS

In this paper, a low power, $2V_{pk\text{-}pk}$ input range VTC has been presented. By compensating the highly non-linear discharge current of the VTC with an SR-latch based TA, we have been able to reduce power consumption, recover the VTC linearity, and maximize input voltage range. The proposed design was shown to be robust across corners which has yet to be showcased in any known VTC works.

Not only is this design one of the most power efficient VTCs across the entire available input frequency range, this structure is also capable of future closed loop optimization schemes due to the controllability introduced in the TA, allowing room for future work to take place. The designed architecture is thus a step closer to practical implementation for high data rate next generation wireless communication.

REFERENCES

[1] S. Ziabakhsh, G. Gagnon, and G. W. Roberts, "A second-order bandpass delta-sigma time-to-digital converter with negative time-mode feedback," *IEEE Trans. on Cir. and Syst. – I : Regular Papers*, vol. 66, no. 4, pp. 1355–1368, Apr. 2019.

[2] A. H. Hassan, *et al*, "An ultra-low power voltage-to-time converter (VTC) circuit for low power and low speed applications," *IEEE International System-on-Chip Conf. (SOCC)*, Seattle, WA, USA, 2016, pp. 178–182.

[3] H. Mostafa and Y. I. Ismail, "Highly-linear voltage-to-time converter (VTC) circuit for time-based analog-to-digital converters (T-ADCs)," *IEEE Intl. Conf. on Elec., Cir., and Syst. (ICECS), Abu Dhabi, United Arab Emirates, 2013, pp. 149–152.*

[4] S. Jia *et al*, "A highly linear 5GS/s voltage-to-time converter for time-based analog-to-digital converters," *IEEE Asia Pac. Micro. Conf. (APMC)*, Kuala Lumpar, 2017, pp. 714-717.

[5] P. Osheroff, G. LaRue, and S. Gupta, "A highly linear 4GS/s uncalibrated voltage-to-time converter with wide input range," *IEEE Intl. Symp. on Cir. and Syst. (ISCAS)*, Montréal, QC, Canada, 2016, pp. 89–92.

[6] M. Lee and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse–fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. of Solid-State Cir.*, vol. 43, no. 4, pp. 769–777, Apr. 2008.