Zero-Power Feed-Forward Spur Cancelation for Supply-Regulated CMOS Ring PLLs

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***Abstract*— A new reference-spur cancelation technique is presented for supply-regulated ring-oscillator-based integer-N phase-locked loops (PLLs). A passive *RC* filter is used to implement a feed-forward (FF) spur-coupling path to perform spur cancelation at the PLL control signal. The proposed technique achieves a simulated spur cancelation of about 22 dB at the first spur harmonic. The simulated postcancelation spur value is −79 dBc for an oscillator gain of 0.1 GHz/V and −46 dBc for an oscillator gain of 6 GHz/V. Spur cancelation is also robust against large process, voltage, and temperature variations in the gain and bandwidth of the FF path. A 1-GHz integer-N PLL prototype in a 65-nm CMOS process has a measured cancelation of 19.5 and 13 dB at the first and the second spur harmonic, respectively, with 320 μW of total power consumption. The PLL prototype has an oscillator gain of 1.5 GHz/V, which results in a postcancelation spur of −53 dBc. The proposed zero-power technique is suitable for low-power PLLs as it achieves a large spur cancelation without requiring any additional power consumption or calibration.**

***Index Terms*— Band-reject filter, low power, low-dropout regulator (LDO), phase-locked loop (PLL), reference-spur cancelation.**

I. Introduction

MORE than 20 billion low-cost consumer devices are envisioned to have low data-rate wireless connectivity by 2020 [1] for monitoring, diagnostics, and corrections [2], i.e., a global expansion of the Internet of Things. The subgigahertz bands in the industrial, scientific, and medical category (e.g., 915 MHz in USA and 920 MHz in Japan) are an attractive choice for these low-rate applications using low-power communication standards, such as IEEE 802.15.4 [3].

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Phase-locked loops (PLLs) are used to synthesize the local oscillator (LO) signal in synchronized wireless transceivers for the up/down conversion of the modulated data. The spectral purity of a PLL output is quantified as the relative strength of the phase noise (PN) and the spurious tones (spurs) compared to the LO signal. The reference spurs degrade signal-to-noise ratio in wireless systems by down-converting interference over the desired signal band through reciprocal mixing. The reference spurs also increase PLL's output jitter (i.e., integrated noise).

Normally, the PLL bandwidth (BW) and the frequency tuning range (i.e., oscillator gain) are chosen according to the system requirements. For given PLL design parameters, the PLL PN can be reduced by increasing power consumption. For example, with a fixed PLL BW and oscillator gain, increasing oscillator power consumption reduces PLL's out-of-band PN, while increasing the charge-pump (CP) current may reduce the PLL's in-band PN [4]. However, the reference spurs are a strong function of the PLL BW and oscillator gain. Hence, the reference spurs may not reduce with a simple scaling of PLL power consumption. This has encouraged numerous methods for reducing the spurs [5]–[15].

We propose a feed-forward (FF) spur cancelation technique to minimize the reference spurs in supply-regulated ring PLLs. A high-frequency spur-coupling path is introduced within the PLL using a passive *RC* filter, which provides the replica spur signal for spur cancelation. The reference spurs are canceled just before they induce frequency modulation in the ring oscillator (RO). Consequently, the effect of several spur-causing PLL nonidealities is suppressed simultaneously. A large and robust reference spur cancelation is achieved over a wide range of spur values and various PLL design parameters. The proposed technique does not require any power consumption or complex calibration which makes it suitable for low-power PLL designs.

This paper is organized as follows. A brief introduction on PLL architecture, reference spurs in integer-N PLLs, and prior art is given in Section II. The proposed technique, its performance, and scalability are presented in Section III. The impact of the spur-coupling path on PLL stability and PN is analyzed in Section IV. The PLL design details are provided in Section V. Measurement results are shown in Section VI and the conclusions are summarized in Section VII.

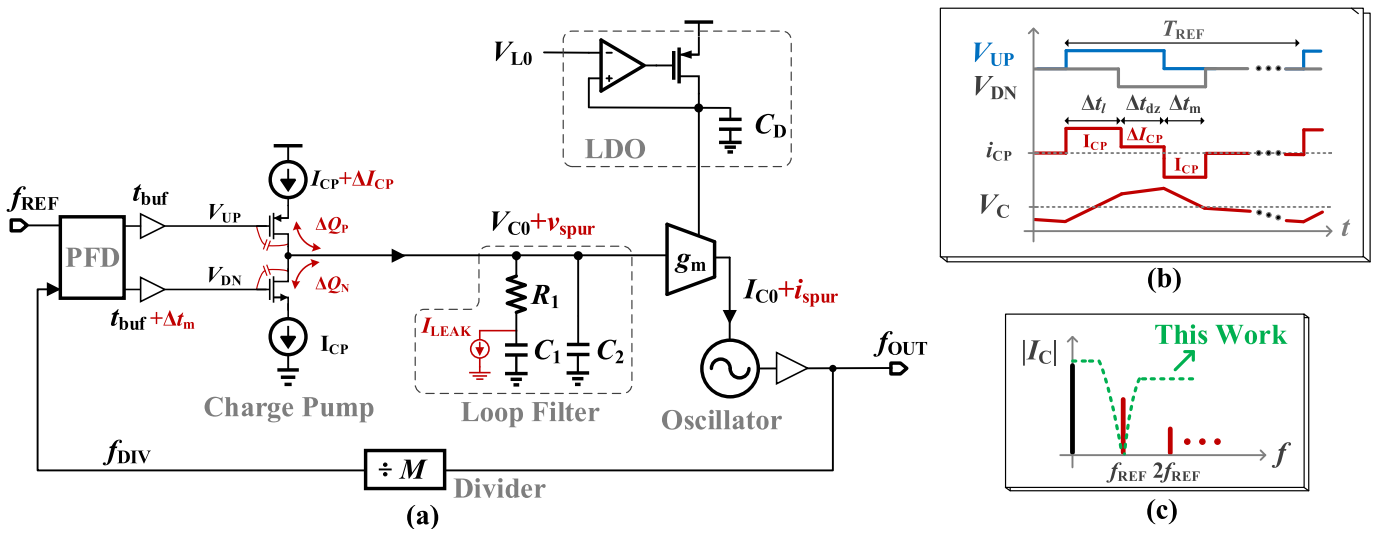

Fig. 1. (a) Integer-N PLL block diagram (key nonidealities that cause reference spurs are highlighted). (b) Time-domain waveforms at the PFD, charge-pump, and the loop-filter outputs. (c) Oscillator's frequency control current (I_C) in the frequency domain.

II. Reference Spurs in Integer-N PLLs

A. Supply-Regulated Ring PLL Architecture

A block diagram of a conventional integer-N PLL is shown in Fig. 1(a). With the very large-scale integration of digital and analog circuits on a common silicon substrate, the resulting large supply noise degrades the PLL PN [16]. The frequency modulation of supply noise by the RO is most detrimental to PLL noise performance, as ROs have a large oscillator gain due to their highly nonlinear frequency tuning characteristics. Furthermore, the control-voltage (V_C) range in a PLL operating from 1-V supply is usually limited from 0.3 to 0.7 V, to ensure that CP current sources operate in a deep saturation region. A smaller V_C range requires a higher oscillator gain to maintain the same frequency tuning range.

An RO's supply-noise immunity is improved by using a dedicated low-dropout regulator (LDO) [17]. The LDO can be used either within the PLL's negative-feedback loop by using a supply-voltage-tuned RO [18] or outside the loop by using a gate-voltage-tuned RO [19]. The LO buffers are used to provide a rail-to-rail voltage swing for the feedback divider, and to isolate the RO from variable output loading conditions. To maintain a constant swing at the PLL output, a supply-voltage-tuned RO requires an increasingly larger buffer gain with a decreasing supply voltage. Hence, the gate-voltage-tuned RO is used for lower power implementation, as shown in Fig. 1(a).

B. Reference Spurs: Cause and Strength

PLL operation in the lock state is described as follows. The phase-frequency detector (PFD) samples the input phase difference ($\Delta\Phi_{IN}$) between the reference (f_{REF}) and the feedback (f_{DIV}) signals with a T_{REF} period. The CP then converts $\Delta\Phi_{IN}$ into an equivalent charge injected in or withdrawn from the loop filter (LF). The key PLL nonidealities causing a periodic high-frequency spurious signal (v_{spur}) at the control voltage V_C are highlighted in Fig. 1(a), and briefly summarized as follows.

1) The timing mismatch (Δt_m) between the V_{UP} and the V_{DN} signal paths due to mismatches in the capacitive loading and during the single ended to differential conversion in the PFD.
2) The periodic charge sharing/injection into the LF by the CP switches during the ON/OFF transitions.
3) The signal feed through, i.e., capacitive coupling of the PFD's digital output signal to the LF through the gate–drain capacitance of the CP switches.
4) The minimum required pulsewidth (Δt_{dz}) for V_{UP} and V_{DN} signals for a complete steering of the CP currents to avoid the switching dead zone. The CP's UP and DN current mismatch (ΔI_{CP}) is injected into the LF for Δt_{dz} duration.
5) The LF capacitor (C_1) leakage current (I_{LEAK}) decreases V_C, which is compensated by injecting I_{CP} into the LF for an additional Δt_l duration. For example, an I_{LEAK} of 0.5 μA discharges C_1 of 150 pF by 0.35 mV in (a T_{REF} of) 100 ns.

The time-domain signal waveforms for the PFD, the CP, and the LF are depicted in Fig. 1(b), ignoring charge injection and signal feed through. The periodic disturbances at V_C are filtered by the loop. The resulting control current (I_C) at the output of the transconductance (g_m) is shown in Fig. 1(c) in the frequency domain. The spur components in I_C are frequency modulated to PLL output by the oscillator as reference spurs.

Using the narrowband frequency-modulation approximation, the output spur strength (A_{spur}) of the first reference harmonic at f_{REF} relative to the PLL output (A_{out}) is given as

$$\left.\frac{A_{spur}}{A_{out}}\right|_{@\,f_{REF}} = \left.\frac{g_m K_C}{2f_{REF}} v_{spur}\right|_{@\,f_{REF}} \approx \left.\frac{g_m K_C}{2f_{REF}} \frac{f_2}{f_{REF}} R_1 i_{CP}\right|_{@\,f_{REF}} \quad (1)$$

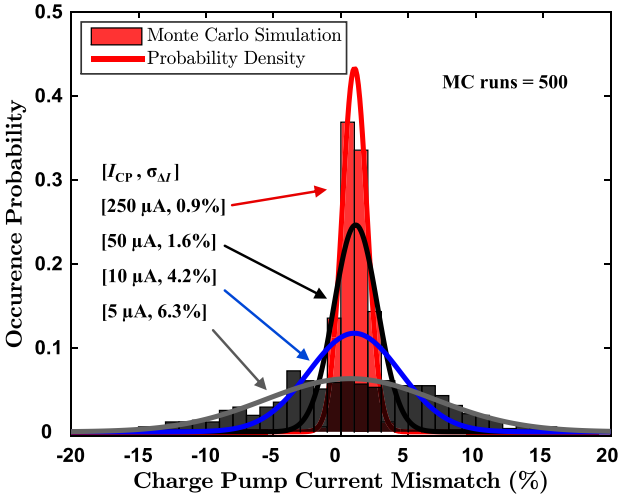

Fig. 2. Monte Carlo simulation results for the CP current mismatch for 500 runs. The histogram is shown for an I_{CP} of 5 and 250 μA.

where i_{CP} is the current injected by the CP into the LF. The K_C is the oscillator gain (Hz/A), which results in a net oscillator gain of $g_m K_C$ (Hz/V). The zero and pole by the second-order LF are ω_1 $(= 1/C_1R_1)$ and ω_2 $(= 1/C_2R_1)$, respectively. Equation (1) shows that for a given PLL BW and f_2, the spur value scales in proportion to the oscillator gain. For example, approximating v_{spur} as a saw-tooth waveform of 0.5-mV amplitude, with f_{REF} of 10 MHz, a $g_m K_C$ of 1.5, and 0.1 GHz/V results in a spur of -35 and -58.5 dBc, respectively.

The PLL power consumption can be lowered by reducing the power consumption of the oscillator, CP, and its bias circuit. The oscillator gain may not necessarily change with its power consumption. The PLL's open-loop gain transfer function (TF), $G_{OL}(s)$, is

$$G_{OL}(s) = \frac{I_{CP}}{2\pi} \frac{\left(1+\frac{s}{\omega_1}\right)}{sC_1\left(1+\frac{s}{\omega_2}\right)} \frac{g_m K_C}{s} \frac{1}{M} \tag{2}$$

where the feedback division ratio is M, and $I_{CP}/2\pi$ (A/rad) is the combined gain of the PFD and the CP. A lower I_{CP} requires a proportionally smaller LF capacitor C_1.[1] A smaller C_1 requires a proportionally larger LF resistor R_1 to maintain ω_1, i.e., the PLL BW and PM.

The histogram for the mismatch between the CP's UP and DN currents is shown in Fig. 2. For simplicity, the MOSFET gate bias and gate length are kept fixed while the device width is scaled to scale the CP current. The standard deviation $(\sigma_{\Delta I})$ of the percentage current mismatch increases with a decrease in the CP current as the MOSFET device area is reduced [21]. Overall, reducing the CP current increases the ripple $i_{CP}R_1$ on the control voltage due to a proportionally larger R_1 and a higher current mismatch. For example, an I_{CP} of 10 μA with $3\sigma_{\Delta I}$ mismatch between UP and DN currents results in a calculated spur value of -32.3 dBc (1) [22], using R_1 of 14 kΩ, $g_m K_c$ of 1.5 GHz/V, Δt_{dz} of 400 ps, and f_2 of 22.7 MHz.

[1]Note that the CP bias-circuit power consumption also scales with I_{CP} for a fixed percentage contribution by the bias-circuit noise to the total CP noise.

Similarly, designing a lower power PFD requires smaller device sizes. The smaller PFD device sizes may result in a larger mismatch between the UP and DN signal paths, which increases the timing mismatch Δt_m. A larger Δt_m results in higher reference spur. Therefore, low-power ring PLLs with large oscillator gain are inherently prone to large spurs.

C. Prior Art of Spur Reduction

The reference spur can be suppressed by simply using a smaller PLL BW, which results in a higher noise contribution from the RO and a longer settling time. Subblock level spur-cause mitigation techniques, such as the PFD calibration [5], minimization of the ΔI_{CP} [6], [15], the charge injection [20], and the I_{LEAK} [8], [9], have been proposed to reduce spurs.

A holistic approach can minimize the cumulative effect of multiple PLL nonidealities simultaneously. The PLL corrects the input phase difference at each rising/falling reference edges. The spur periodicity is broken by randomizing the correction time instant using pulse position modulation [12] or random clock generator [21], which spreads the spur as broadband noise. If the period at which the loop corrects the error is reduced from T_{REF}, the (now) higher frequency spurs experience higher filtering by the loop. The period is decreased by eight times using edge interpolators in [7] which suppresses the fundamental spur by 16 dB, but requires 5.8 mW for only the edge interpolators.

As shown in Fig. 1(c), use of a band-reject filter at the oscillator control signal reduces the spurs. A power-hungry digital filter is realized in [11] by adding a digital correction signal (ideally equal to $-v_{spur}$) to V_C, which achieves on average 13.3 dB of spur suppression. A direct down-conversion receiver is used for an analog cancelation in [10], which achieves 12.5 dB of noise and spur reduction while consuming an additional 4.5 mW. In [14], an active-L-based LC-filter is used at the control node to shunt the spurs to the ground, which reduces the spur by 18 dB after calibration and consumes 250 μW. In comparison, the proposed method employs a passive RC filter to achieve 19.5 dB of measured spur cancelation without any additional power consumption or calibration.

III. Feed-Forward Spur Cancelation Technique

A. Proposed Concept

The PLL block diagram with the proposed FF uses a passive high-pass filter $H_{HF}(s)$ to couple the high-spur-coupling path is shown in Fig. 3(a). The proposed design frequency spur signals to the LDO input. The spur signal then travels to the RO's supply node (V_L) with an additional low-pass filtering by the LDO closed-loop TF $H_{LDO}(s)$. Consequently, the FF path TF FF(s) has a bandpass frequency response. The FF(s) is depicted in the bode-plot diagram of Fig. 3(b), with f_{LDO} as the closed-loop 3-dB BW of the LDO.

The MOSFET drain current in saturation region is a function of the difference of its gate and source voltages $(V_G - V_S)$. Hence, the M_P's V_{GS} is the effective control voltage for the RO. The LDO output voltage V_L is given as

$$V_L = V_{L0} + \text{FF}(s)v_{spur} \tag{3}$$

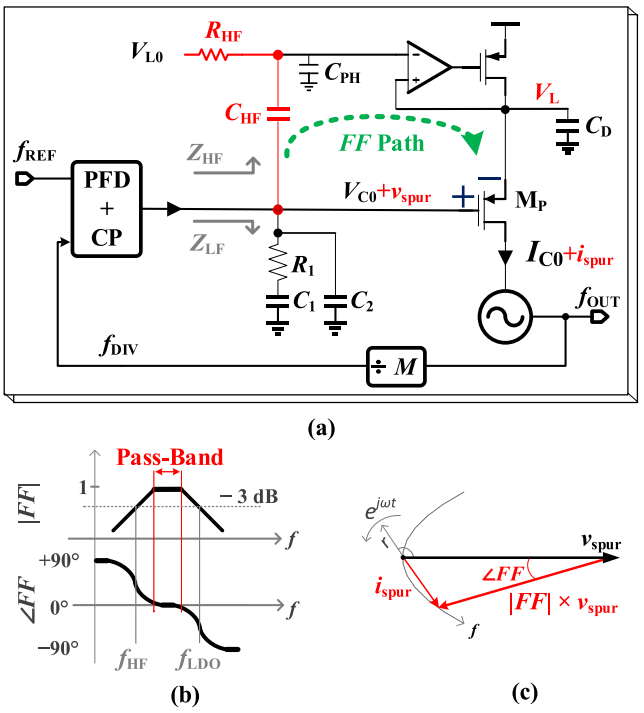

Fig. 3. (a) Proposed PLL architecture with the FF path. (b) Bode plot of the FF TF, FF(s). (c) Phasor diagram representation of the FF reference-spur cancelation by the M_P.

where V_{L0} is LDO's input reference voltage. The M_P's drain current (i.e., oscillator control current) I_C is given as

$$\begin{aligned} I_C &= (V_{L0} - V_{C0}) - (1 - \mathrm{FF}(s))g_m v_{\mathrm{spur}} \\ &= I_{C0} - R(s)g_m v_{\mathrm{spur}}. \end{aligned} \tag{4}$$

The high-frequency spur components (i_{spur}) of I_C that fall within the FF(s) passband are filtered by an equivalent band-reject filter $R(s)$ due to the V_{GS} cancelation by the M_P. The spur cancelation phasor diagram is shown in Fig. 3(c). The highest spur cancelation is achieved at the $R(s)$ center frequency f_R, where ideally the FF(s) magnitude (|FF|) is 1 and phase shift (∠FF) is 0°. With a wideband FF path and finite gain roll-off of the FF(s), the higher spur harmonics are also feed-forwarded and canceled by the M_P.

B. Feed-Forward Design and Implementation

The FF path TF FF(s) is given as

$$\mathrm{FF}(s) = H_{\mathrm{HF}}(s)H_{\mathrm{LDO}}(s) \tag{5}$$

$$H_{\mathrm{HF}}(s) = \frac{s}{\omega_{\mathrm{HF}}} \frac{\beta}{\left(1 + \frac{s}{\omega_{\mathrm{HF}}}\right)} \tag{6}$$

$$H_{\mathrm{LDO}}(s) = \frac{H_L(s)}{1 + H_L(s)} \tag{7}$$

where $\beta = C_{\mathrm{HF}}/(C_{\mathrm{HF}} + C_{\mathrm{PHF}})$, $\omega_{\mathrm{HF}} = 1/(C_{\mathrm{HF}}R_{\mathrm{HF}})$, and $H_L(s)$ is the LDO open-loop TF. The FF path impedance Z_{HF} introduces a pole–zero pair in the effective loop-filter impedance Z_{ELF} (= $Z_{\mathrm{HF}}||Z_{\mathrm{LF}}$), which affects the PLL phase margin (PM). Here, Z_{LF} is the second-order LF impedance as shown in Fig. 3(a). The BW of $H_{\mathrm{HF}}(s)$ should be much higher than the PLL BW to avoid a considerable degradation of the PLL PM. The optimum f_{HF} is calculated by solving for ∠FF($j\omega_R$) = 0° (i.e., maximum spur cancelation at f_R), which results in

$$f_R^2 = f_{\mathrm{HF}} f_{\mathrm{LDO}}. \tag{8}$$

For an f_{LDO} of 70 MHz in this paper, f_{HF} is chosen as 1.5 MHz for an f_R of 10 MHz (= f_{REF}).

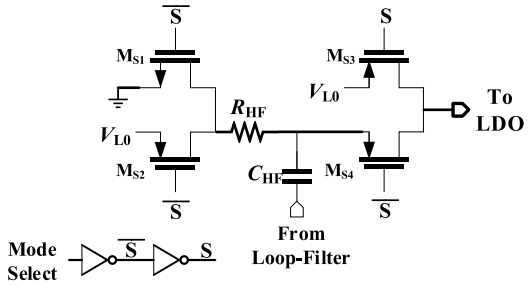

Fig. 4. Schematic of the switch network used for controlling the FF path between ON and OFF modes, only for comparing PLL performance.

A switch (SW) network is used to switch the FF path between the ON mode and the OFF mode, only for comparative measurement capability. The switch network schematic is shown in Fig. 4. The resistance R_{HF} is grounded in the OFF mode, for an equal loop-filter impedance in both ON and OFF modes. The channel resistance of M_{S1-2} is included in R_{HF}, and the parasitic capacitance due to M_{S3-4} is included in C_{PHF} as shown in Fig. 3(a). Hereafter, the PLL shown in Fig. 3(a) is referred to as the conventional PLL (Conv PLL) with the FF path OFF and as the FF PLL with the FF path ON.

C. Spur Cancelation Performance and Scalability

The PLL shown in Fig. 3(a) is designed using a 65-nm CMOS process with an f_{REF} of 10 MHz. The PLL is simulated using transistor-level circuits for a range of $g_m K_C$ values to ascertain the performance of proposed spur cancelation technique. The RO is implemented using VerilogA only for these simulations. PLL design details are provided in Section V. The I_{CP} in (2) is scaled in inverse proportion to $g_m K_C$ to maintain PLL characteristics during comparisons.

The simulated first reference-spur harmonic strength (in dBc) is shown in Fig. 5. An oscillator gain of 1.5 and 0.1 GHz/V results in a reference spur of −35 and −57.5 dBc, respectively, in the Conv PLL. The spur strength scales with the oscillator gain for a fixed PLL BW, as shown in (1). The FF PLL achieves a spur of −79 dBc for an oscillator gain of 0.1 GHz/V. The fundamental spur harmonic is canceled by an average of 22 dB using the proposed technique across the precancelation spur values of −23 to −57.5 dBc.

The FF(s) design parameters, such as gain and frequency response, may vary with process, voltage, and temperature (PVT) variations and thus affect the spur cancelation performance. The proposed band-reject filter's magnitude at f_{REF} ($|R(j\omega_{\mathrm{REF}})|$) is shown in Fig. 6 against PVT variations in the FF path gain ($|\mathrm{FF}(j\omega_{\mathrm{REF}})|$) and LDO's dominant

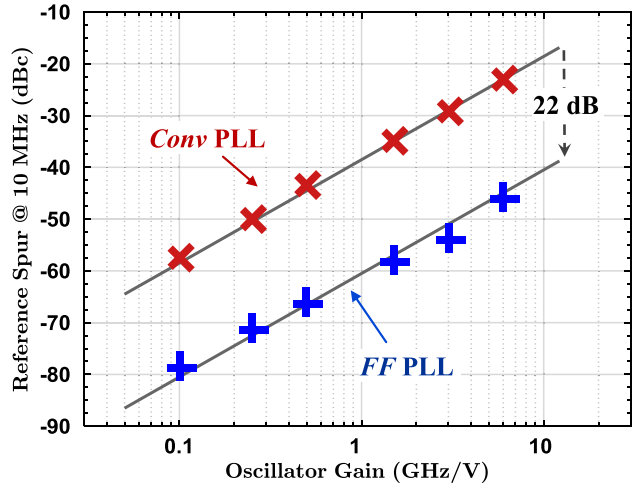

Fig. 5. Spur strength in a PLL using transistor-level circuit simulations. Only the ring oscillator is implemented using VerilogA. The $f_{\rm OUT}$ is 1 GHz, and $f_{\rm REF}$ is 10 MHz. The proposed method achieves a spur cancelation of 22 dB.

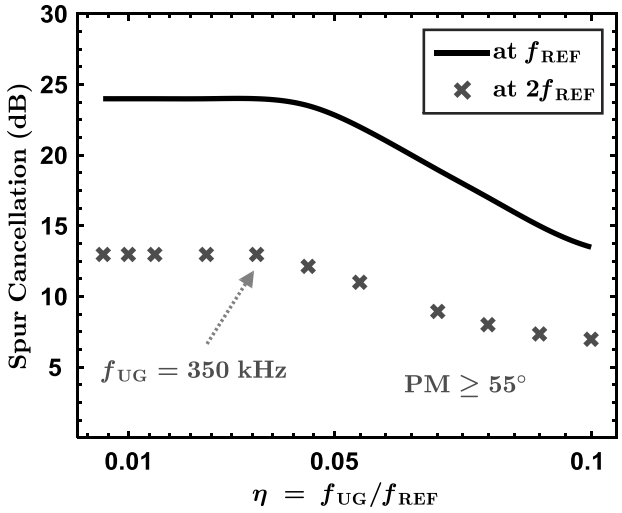

Fig. 7. Calculated spur cancelation against PLL BW with a minimum FF PLL PM of 55°. The $f_{\rm OUT}$ is 1 GHz, $f_{\rm REF}$ is 10 MHz, and $g_m K_C$ is 1.5 GHz/V.

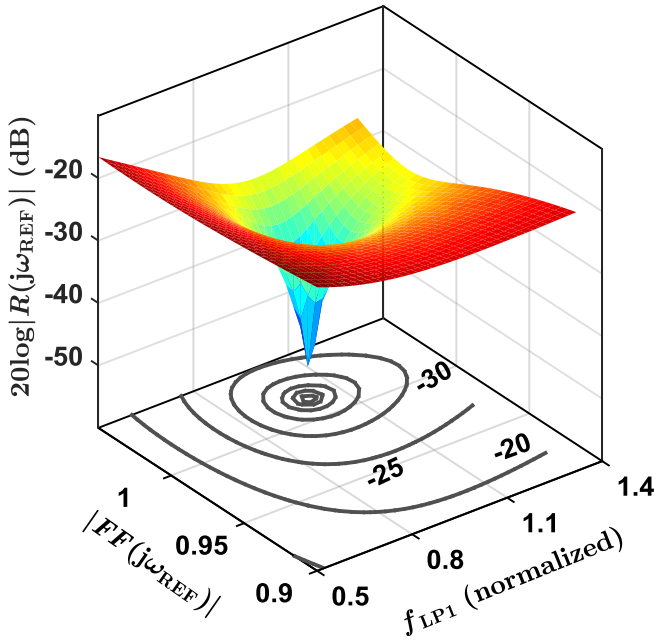

Fig. 6. Calculated $R(s)$ magnitude at $f_{\rm REF}$ against PVT-induced variations in the gain of FF(s). The $f_{\rm OUT}$ is 1 GHz, $f_{\rm REF}$ is 10 MHz, and $g_m K_C$ is 1.5 GHz/V.

open-loop pole $f_{\rm LP1}$.[2] In practice, $\angle{\rm FF}(j\omega_{\rm REF})$ is not equal to 0° due to higher order parasitic poles and zeros. Consequently, the theoretical maximum spur cancelation is 55 dB at an $|{\rm FF}(j\omega_{\rm REF})|$ of 1.015. Moreover, $|{\rm FF}(j\omega_{\rm REF})|$ is less than 1 due to a finite LDO open-loop gain, and passive implementation of the $H_{\rm HF}(s)$ which causes a β of less than 1, as shown in (6). The simulated $|{\rm FF}(j\omega_{\rm REF})|$ is 0.95 in this paper, which results in a spur cancelation of 24 dB for an optimum $f_{\rm LP1}$. As shown in Fig. 6, the proposed technique achieves a robust spur cancelation of more than 20 dB against 16% variation in $|{\rm FF}(j\omega_{\rm REF})|$ and 30% variation in $f_{\rm LP1}$.

[2]The effect of $f_{\rm HF}$ on $R(s)$ is similar to that of the $f_{\rm LP1}$ (i.e., $f_{\rm LDO}$). However, due to passive implementation, $f_{\rm HF}$ is much less sensitive to variations compared to the LDO frequency response.

The spur cancelation is also simulated against PLL BWs to investigate the applicability of the proposed method to the PLLs designed for different applications.[3] A minimum FF PLL PM of 55° is maintained during these simulations. The $f_{\rm HF}$ is kept as 1.5 MHz for $f_{\rm UG}/f_{\rm REF}$ $(\eta) \leq 0.05$, since the resulting PLL PM is greater than 55°. The $f_{\rm HF}$ is increased for $\eta > 0.05$ values to maintain the PM. As shown in Fig. 7, a spur cancelation of 24 and 13 dB is achieved at $f_{\rm REF}$ and $2f_{\rm REF}$, respectively, for $\eta \leq 0.05$. The f_R increases with $f_{\rm HF}$, as shown in (8), which reduces spur cancelation for $\eta > 0.05$ values. A minimum cancelation of 13 dB is achieved at $f_{\rm REF}$ for a maximum η of 0.1. An optimized PLL design can increase spur cancelation for large values of η.

IV. PLL Analysis and Design

A. Loop Stability

FF PLL open-loop gain TF $G_{\rm OLFF}(s)$ and the $Z_{\rm ELF}$ are given as

$$G_{\rm OLFF}(s) = \frac{I_{\rm CP}}{2\pi} Z_{\rm ELF} R(s) \frac{g_m K_C}{s} \frac{1}{M} \tag{9}$$

$$Z_{\rm ELF} = Z_{LF} || Z_{\rm HF} = \frac{\left(1+\frac{s}{\omega_1}\right)}{s(C_1+C_{\rm HF})\left(1+\frac{s}{\omega_2}\right)} \frac{\left(1+\frac{s}{\omega_{\rm HF}}\right)}{\left(1+\frac{s}{\omega_T}\right)} \tag{10}$$

where $\omega_T = 1/[(C_{\rm HF}||C_1)(R_{\rm HF}+R_1)]$. The calculated pole and zero values are: $f_1 = 76$ kHz, $f_2 = 22$ MHz, $f_{\rm HF} = 1.5$ MHz, and $f_T = 0.96$ MHz. The bode plots of the PLL open-loop gain are shown in Fig. 8 for the FF PLL, the Conv PLL with $Z_{\rm ELF}$ as the loop-filter impedance (i.e., FF path in OFF mode), and the Conv PLL with $Z_{\rm LF}$ as the loop-filter impedance [as shown in Fig. 1(a)]. With FF path in ON mode, the fundamental and the second spur harmonics are canceled by 24 and 13 dB, respectively, compared to when the FF

[3]For PLLs using a variable reference frequency, the $H_{\rm HF}(s)$ can be reconfigured (for example, by implementing $C_{\rm HF}$ using a capacitor bank) to realign the $R(s)$ center frequency f_R with that of the reference frequency (8). Then, spur cancelation is determined by the ratio η, as shown in Fig. 7.

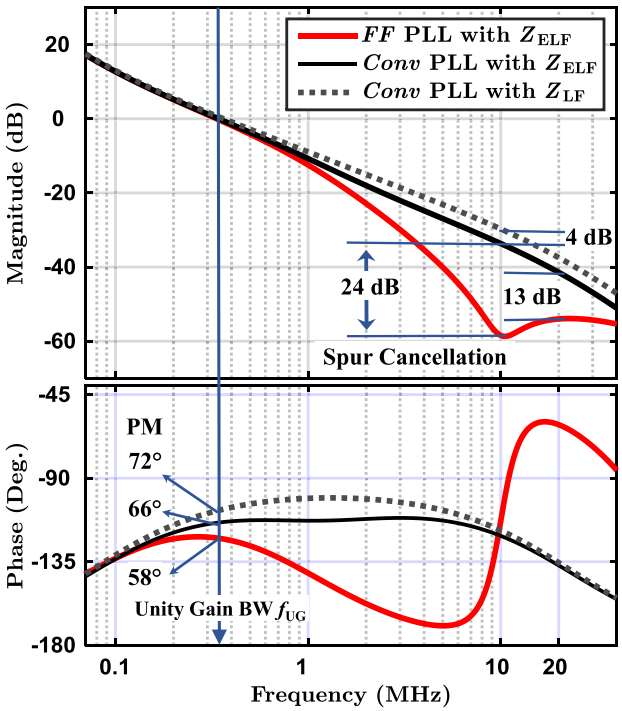

Fig. 8. Bode plots of the PLL open-loop gain TF for the FF PLL, the Conv PLL with Z_{ELF}, and the Conv PLL with Z_{LF}.

path is in OFF mode.[4] The PLL unity-gain frequency (f_{UG}) is about 350 kHz for all three cases. The Conv PLL PM is 72° with Z_{LF}, which reduces to 66° with Z_{ELF}. With an equal LF impedance Z_{ELF}, the PLL PM reduces by 8° due to $R(s)$ when FF path is ON compared to when FF path is OFF.[5]

B. Design Details

A D flip-flop (DFF)-based tri-state PFD is used. The schematics of the PFD and the DFF with reset are shown in Fig. 9. The operation of the DFF is as follows. With clock (CLK) and reset (RST) signal as 0, the X and Y nodes are precharged to 1 and 0, respectively. Transistor P_1 disables inverter 1 (INV_1). With CLK = 1, the arrival of PFD's RST signal enables the N_2 to discharge the node X to 0, which charges the node Y to 1 through the INV_1. Setting $Y = 1$ SWs OFF P_3, thus holding X at 0 utill the CLK falling edge precharges Y to 0 through N_1. Assuming a zero phase difference at the PFD input, the timing diagram for the DFF is shown in Fig. 9.

A cascode current-mirror-based CP is used with an I_{CP} of 10 μA. A current-mirror ratio of 4:1 is used in the CP to suppress the bias noise contribution by 16 times. The bias circuit is shared by the CP and the LDO. The loop-filter values

[4]Reference spurs can also be reduced by using a third-order LF [15]. The additional LF pole f_P increases spur filtering by the loop at the cost of a lower PLL PM. For example, an additional pole f_P of 1.4 MHz reduces the PLL PM by $\tan^{-1}(f_{UG}/f_P) = 14°$ and the spur at f_{REF} by $20\times\log_{10}(f_{REF}/f_P) = 17$ dB compared to the *Conv* PLL with Z_{LF}. In comparison, the proposed FF PLL reduces PM by 14° and spur by 28 dB compared to the Conv PLL with Z_{LF}, as shown in Fig. 8.

[5]A unity-gain amplifier with BW greater than the LDO BW can restore PM by isolating impedance Z_{HF} from the LF.

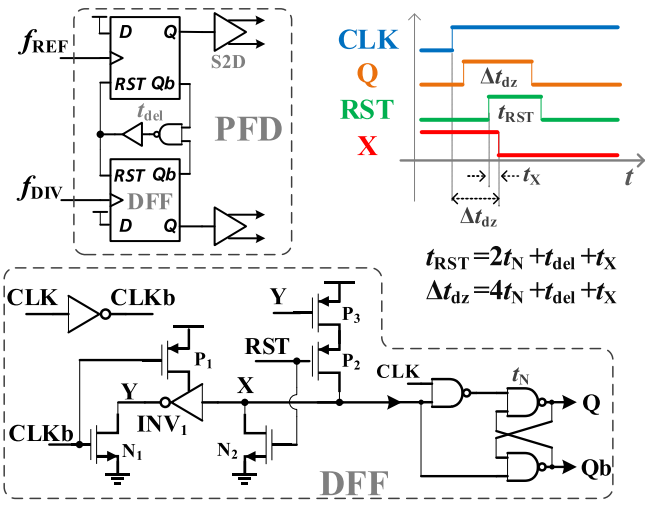

Fig. 9. PFD schematic and the timing diagram of the edge-triggered DFF with reset pulse generator.

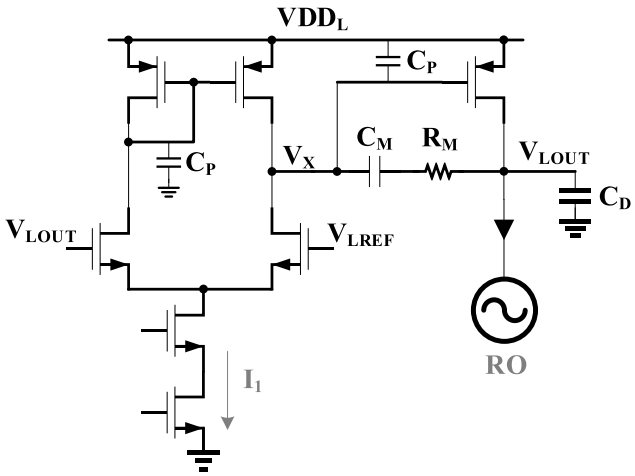

Fig. 10. LDO schematic using Miller compensation for stability.

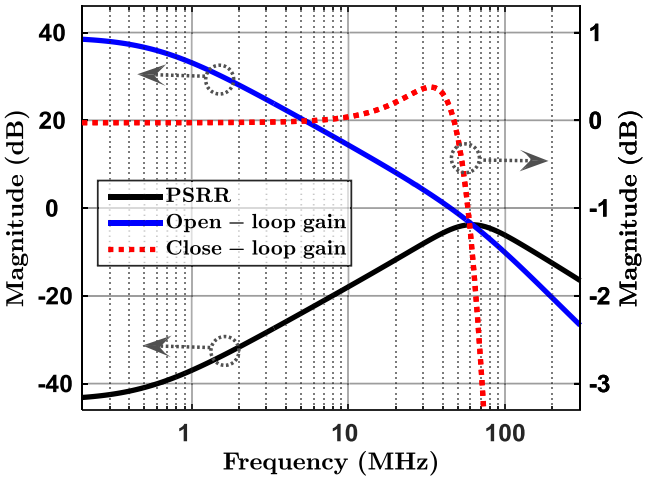

Fig. 11. LDO TFs using transistor-level circuit simulations.

are $C_1 = 150$ pF, $R_1 = 14$ kΩ, $C_2 = 0.5$ pF, $R_{HF} = 24$ kΩ, and $C_{HF} = 4.5$ pF. The RO is composed of three-stage current-starved single-ended inverters. The M_P's bulk and source

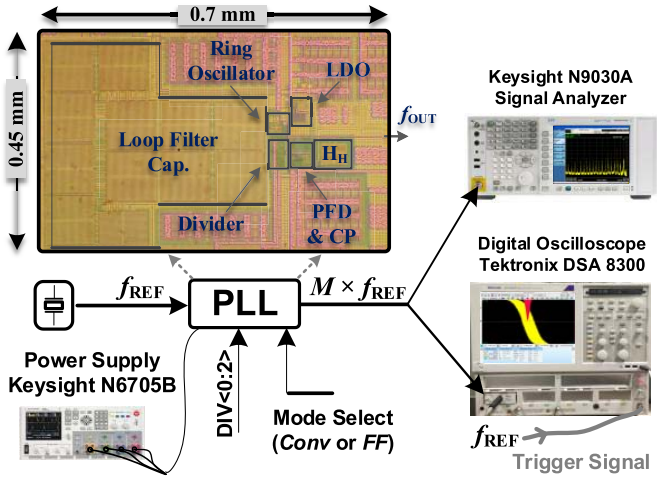

Fig. 12. PLL chip micrograph and measurement setup for the time- and frequency-domain characterization.

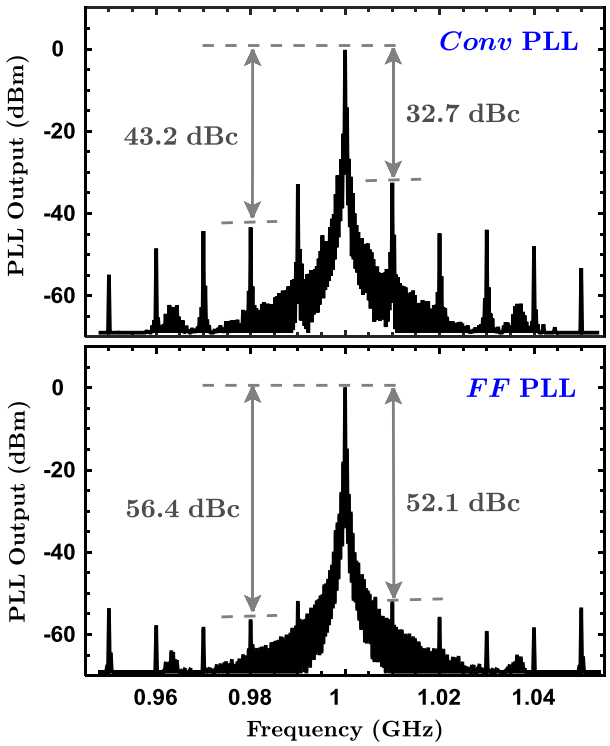

Fig. 13. Measured PLL output spectrum at 1-GHz output frequency in FF and Conv modes. RBW = 10 kHz and VBW = 1 kHz.

nodes are shorted to nullify its bulk transconductance. The RO has a tuning range of 0.6–1.7 GHz and an oscillator gain of 1.5 GHz/V.

PLL output is divided by two before feeding to the prescaler in the feedback divider. Feedback divider ranges from 44 to 51. PLL output frequency tuning range is 880 MHz–1.02 GHz, which is limited by the divider in this demonstration. To minimize spur leakage through the substrate, PLL blocks are isolated by placing each block in an independent deep n-well that is surrounded by a single layer of deep-trench wall [23].

The LDO schematic is shown in Fig. 10. The Miller compensation technique with zero placement is used to stabilize

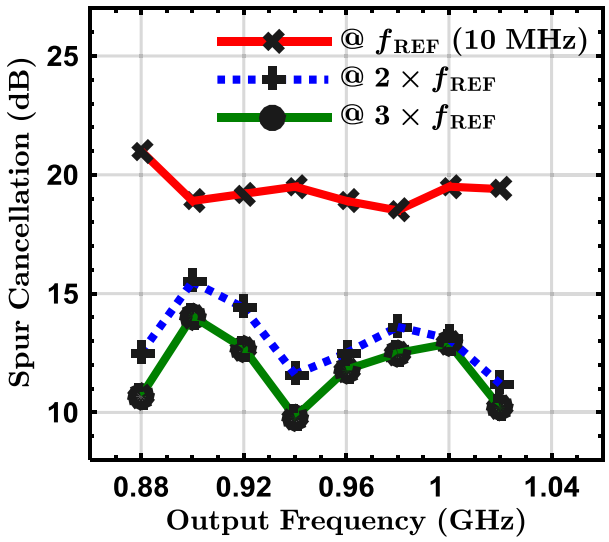

Fig. 14. Measured spur cancelation for various reference harmonics across the PLL frequency tuning range.

TABLE I
FF PLL PERFORMANCE SUMMARY

Technology	65 nm CMOS
Supply voltage	1 V and 1.5 V
Output frequency	1 GHz
Reference frequency	10 MHz
Loop bandwidth	0.35 MHz
Oscillator gain	1.5 GHz/V
Reference spur at f_{REF}	−52.1 dBc
Spur cancellation at f_{REF}	19.5 dB
Total power consumption	320 μW
Phase noise at 100 KHz	−62 dBc/Hz
Die area	0.32 mm^2

the LDO by using capacitor C_M and resistor R_M, as shown in Fig. 10. The bode-magnitude plot for the LDO's power-supply rejection ratio (PSRR), open-loop gain, and the closed-loop gain are shown in Fig. 11. A 1.8-V-thick gate-oxide pMOS device regulates a 1.5- to 1-V supply voltage for the RO. The design parameters for the LDO are: $C_M = 0.2$ pF, $R_M = 3$ kΩ, $C_D = 57$ pF, and $I_1 = 25$ μA. The simulated LDO open-loop poles and zeros are at {0.6, 70, 190} and 190 MHz, respectively. The PSRR is more than 35 dB below 1 MHz. The $H_L(s)$ has a peaking of <0.8 dB and phase margin of > 50° across process and temperature variations.

V. EXPERIMENTAL RESULTS

An integer-N PLL prototype is fabricated in a 65-nm bulk CMOS process. The PLL chip micrograph and measurement setup are shown in Fig. 12. The FF path adds an area overhead of less than 2% of the total area. The PLL operates from 1- to 1.5-V supplies and consumes a total of 320 μW, excluding output buffers.

The measured PLL output spectrum at 1 GHz is compared in Fig. 13 for both PLL modes. A spur cancelation of 19.4 and

TABLE II
COMPARISON OF PROPOSED ZERO-POWER FF SPUR CANCELATION WITH PLLS USING SPUR SUPPRESSION AND OPERATING AT SIMILAR FREQUENCY

	This Work	[21] TVLSI'13	[14] JSSC'16	[7] TVLSI'12	[15] RFIC'15	[13] JSSC'08
Output frequency [GHz]	**1**	2.6	2.4	1	2.4	2.4
Reference frequency f_{REF} [MHz]	**10**	5	22.6	13	1	12
f_{UG}/f_{REF}	**1/29**	1/100	1/2.3†	1/44	1/25	1/12
Oscillator gain [GHz/V]	**1.5**	0.33	1.5	0.05	0.09	0.06
1st Spur harmonic [dBc]	**−53**	−72	−65	−57	−50	−70
Spur suppression* [dB]	**19.5**	19	18	16	15	12
Power overhead for Spur cancellation? (%)	**No (0%)**	Yes (N/A)	Yes (6.3%)	Yes (20%)	No (0%)	Yes (N/A)

†Type-I PLL. 1st spur harmonic post-cancellation or suppression.

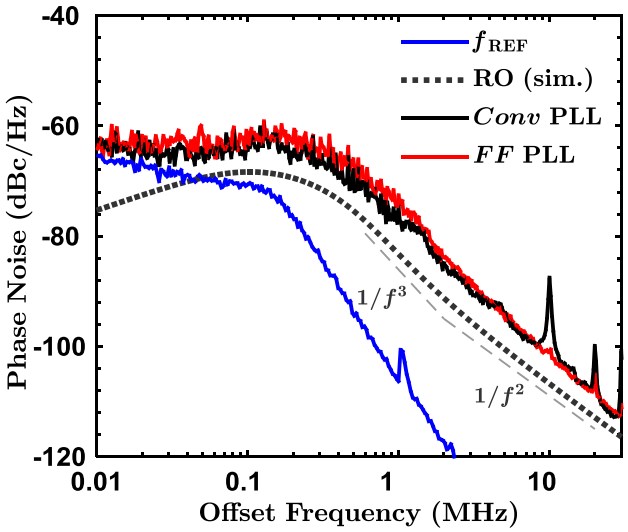

Fig. 15. Measured PLL PN at 1 GHz in FF and Conv modes. Contribution of the reference signal (measured) and the RO (simulated) to PLL's PN is also shown.

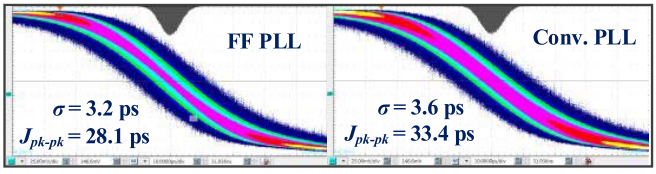

Fig. 16. Measured jitter histogram of PLL at 880-MHz output in FF and Conv modes using 100-K waveform samples.

13 dB is measured at the first and the second spur harmonics, respectively. The measured spur cancelation across the PLL frequency tuning range for up to the third spur harmonic is shown in Fig. 14. An average spur rejection of 19.5, 13, and 11.8 dB is achieved at the first, second, and third spur harmonics, respectively. Spur cancelation increases at higher harmonics and decreases at the first harmonic as f_R is shifted to higher frequency.

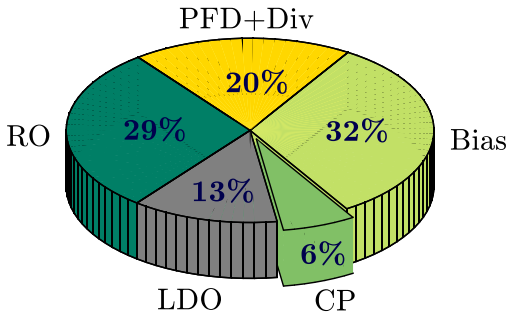

Fig. 17. Power consumption breakdown of the PLL at 1 GHz.

PLL PN for a 1-GHz output frequency is shown in Fig. 15 for both modes of the FF path. The (measured) XTAL oscillator and the (simulated) RO PN contribution to the PLL's PN are also shown in Fig. 15. The PLL in-band PN is –63 and –62.1 dBc/Hz at a 100-kHz offset for the Conv and the FF modes, respectively. The presence of a pole–zero pair in the effective loop-filter impedance Z_{ELF} due to the FF path, as shown in (10), causes peaking in the PLL's noise TF. This noise transfer peaking increases the PN by about 1 dB near the f_{UG}. PLL jitter histograms are shown in Fig. 16. The spur cancelation reduces the integrated noise, which reduces peak-to-peak jitter ($J_{pk\text{-}pk}$) and the jitter variance (σ_t) by more than 14% and 10%, respectively, across the PLL output frequency tuning range.

PLL power consumption breakdown at 1-GHz output frequency is shown in Fig. 17. PLL performance is summarized in Table I. The proposed technique is compared with the state-of-the-art spur suppression methods in Table II. The proposed method suppresses the first spur harmonic by 19.5 dB without consuming any power. Despite a large oscillator gain of 1.5 GHz/V, the PLL prototype has a postcancelation spur of −53 dBc. In comparison, [21] suppresses the first spur harmonic by an average of 19 dB using power hungry and complex active circuits. The spurs in [15] are dominated by

the charge sharing between the CP switches and the LF, which is suppressed by 15 dB at the first spur harmonic using fixed voltage CP biasing. However, this method has limited benefits as it cannot reduce the spur if it is dominated by other PLL nonidealities, as discussed in Section II-B. In summary, the proposed low-complexity technique achieves among the highest spur suppression without requiring any calibration and zero-power consumption.

VI. Conclusion

This paper presents a novel FF spur cancelation technique for supply-regulated ring PLLs. Up to the third spur harmonics are canceled significantly by introducing a passive high-pass filter-based FF spur-coupling path. The proposed method achieves simulated postcancelation spur values of -46 to -79 dBc (depending on the oscillator gain), and is applicable to a wide range of PLL designs with any loop BW. Spur cancelation performance is robust against large PVT variations, which avoids the need of calibration schemes. An integer-N PLL prototype in 65-nm CMOS process achieves a spur cancelation of 19.5, 13, and 11.8 dB at the first, second, and third spur harmonics, respectively. The proposed technique has low complexity and zero power consumption, which makes it suitable for the design of low-power PLLs for low-cost applications.

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