26.4 A 28GHz 41%-PAE Linear CMOS Power Amplifier Using a Transformer-Based AM-PM Distortion-Correction Technique for 5G Phased Arrays

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To fulfill the insatiable demand for high data-rates, the millimeter-wave (mmW) 5G communication standard will extensively use high-order complex-modulation schemes (e.g., QAM) with high peak-to-average power ratios (PAPRs) and large RF bandwidths. High-efficiency integrated CMOS power amplifiers (PA) are highly desirable for portable devices for improved battery life, reduced form factor, and low cost. To meet simultaneous requirements for high efficiency and reasonable linearity, PAs intended for use with complex modulation are often operated in Class-AB mode [1,2]. For small input amplitude in Class-AB, the device is turned-on and has an input capacitance (C_{gs}) of ~(2/3)WLC_{ox}. As the input amplitude becomes large, the device turns-off for part of the RF cycle, thus reducing its effective input capacitance. This input capacitance-modulation effect creates an input-amplitude-dependent phase shift in Class-AB mode resulting in an amplitude-modulation to phase-modulation (AM-PM) distortion [2]. Consequently, it degrades linearity metrics (e.g., error vector magnitude (EVM), adjacent channel power ratio (ACPR)) in complex-modulation systems. External linearization techniques (e.g., digital pre-distortion) are often used in transmitters to meet linearity requirements, but they are complex in nature and expensive to implement. Apart from these, few works at low-GHz frequencies are reported to improve the PA's intrinsic linearity using a varactor- or PMOS-based AM-PM correction methods [1,2]. These works reduce the design overhead of external linearization systems; however, the inclusion of additional capacitive element to correct AM-PM degrades gain and efficiency, which is not optimal for mmW frequencies [1,2].

To address linearity, without degrading performance or introducing dramatic design complexity, we propose a 2-stage linear PA architecture where a compensation transformer is integrated into the amplifier chain to correct AM-PM distortion while maintaining high power efficiency. Figure 26.4.1 shows the conceptual architecture and waveforms of the proposed technique. The 1st and 2nd amplifiers are driver (DA) and power (PA) stage, respectively, and both are biased at Class-AB. A harmonically tuned, continuous Class-F load network is used in the 2nd-stage for high efficiency [3]. The transformer (T_C) acts as an analog pre-distortion network, which is used to compensate for the AM-PM phase shift from the 2-stage amplifier. The proposed T_C samples the RF signal from the input of the DA and generates a nonlinear phase response of θ_C. The magnitude response of the θ_C is designed to be larger than the inherent phase response of the DA, θ_{DA} (i.e. $|\theta_C| > |\theta_{DA}|$). The 2nd stage has a phase response of θ_{PA}, and the design conditions (such as device size, bias level etc.) of this stage are set such that $\theta_{PA}=-\theta_{S1}$, where $\theta_{S1}=\theta_C+\theta_{DA}$. Thus, the net AM-PM distortion is reduced.

Figure 26.4.2 shows the complete schematic of the proposed architecture. The primary coil of the transformer is connected at the input signal path, while the secondary coil of the transformer is connected to an NMOS switch (M_{sw}). The gate terminal of the M_{sw} taps into the gate of the DA's device (M_1), while the drain and source nodes are connected to a large-resistor for well-defined dc bias. As the input power (P_{in}) rises in magnitude (large-signal), the net impedance of T_C primary coil creates an inverse characteristic in comparison to the net impedance created by C_{gs1} in the DA. By appropriately selecting the size of T_C and thereby controlling the net impedance change across P_{in}, a desired phase shift of θ_{S1} can be generated at the output of DA. The layout and the equivalent circuit of the transformer for M_{sw} on and off are shown in Fig. 26.4.2. If M_{sw} is off, there is no current flow in the secondary coil of T_C; therefore, the net inductance in primary coil remains unchanged (i.e. $L_{eq,off} = L_{cp}$). Conversely, when M_{sw} is on, the secondary coil develops an opposing net current of i_{cs}, which reduces the net inductance to a lower value in primary coil, $L_{eq,on} = L_{cp}(1-k_c^2)$. The net impedance waveform for a large signal is shown in Fig. 26.4.2 for both T_C and C_{gs1} across P_{in}.

The proposed AM-PM correction technique offers three key benefits for enhancing PA large-signal performance. First, the control signal of the transformer is directly tapped from the input of the DA's gate terminal, thus there is no need to implement any additional control circuitry. Since the tapped signal is in RF domain the correction process is instantaneous and synchronized with the DA's large-signal behavior, unlike the phase adjusting method in [2] limited to baseband operation. Second, designers can allow lower quiescent bias current in the DA thus generating higher efficiency in contrast to typically designed low-efficiency Class-A DA. Finally, due to the inductive linearization, the net capacitive impedance at the input of the DA reduces; hence, high gain and efficiency can be achieved in the DA compared to other capacitive-based linearization methods as in [1].

To demonstrate the proposed technique, a PA prototype is fabricated in a 65nm CMOS process. Deeply scaled CMOS process used in moderate-to-high $P_{o,sat}$ (e.g., >10dBm) levels pose stability concerns due to an increased Miller effect from a large gate-drain capacitance (C_{gd}). Hence, PAs often need to operate at compromised performance levels. To cope with this adverse effect, we integrate a tunable gate-drain transformer (T_{N1} and T_{N2}) feedback neutralization network as implemented in [4], in both stages using a switched-substrate-shield layout (SSL) technique [5]. The continuous Class-F output matching network is designed using a multi-order tuned network consisting of 3rd-order harmonic matching [3]. Furthermore, a tunable inductor (L_{int}) using the SSL technique is integrated into the inter-stage matching network. These tunable components (T_{N1}, T_{N2}, and L_{int}) provide flexibility to compensate PVT variations and mismatch, ensuring high performance.

Results of the AM-PM phase distortion at the 1st (DA), 2nd (PA), and 2-stage amplifier are shown in Fig. 26.4.3. Less than 0.7° measured phase distortion is achieved at P_{1dB} for the 2-stage amplifier at 28GHz. The distortion is about 1.3° near P_{sat} at 28GHz, enabling amplification of large PAPR signals like 64/256-QAM with low EVM. The PA achieves <1° measured phase distortion at P_{1dB} across 27 to 31GHz. The large-signal performance for 1-tone signals are presented in Fig. 26.4.4. A PAE_{sat} of 41% at 28GHz for $P_{o,sat}$ of 15.6dBm is achieved. The PAE_{sat} varies between 38 and 41% from 26 to 29GHz while maintaining P_{sat}>15dBm. The PA is tested under 64/256/512-QAM signals with 340/50/20MSym/s data-rate with measurement results summarized in Fig. 26.4.5. Due to the low AM-PM distortion at P_{1dB} to P_{sat} level, the PA shows high average power-efficiency for high-order-QAM signals without any external phase pre-distortion, while maintaining excellent EVM and ACPR results. The proposed technique dramatically improves the PA large-signal performance while reducing the complexity and implementation cost as compared with traditional works.

Figure 26.4.6 summarizes recently reported silicon PAs intended for 5G band. At 28GHz, the proposed linear PA amplifies a 340MSym/s 64-QAM signal with –26.4dB EVM and –30dBc ACPR while achieving PAE of 18.2% at +9.8dBm of $P_{o,avg}$. Figure 26.4.7 shows the die micrograph of the PA with an active area of only 0.24mm^2.

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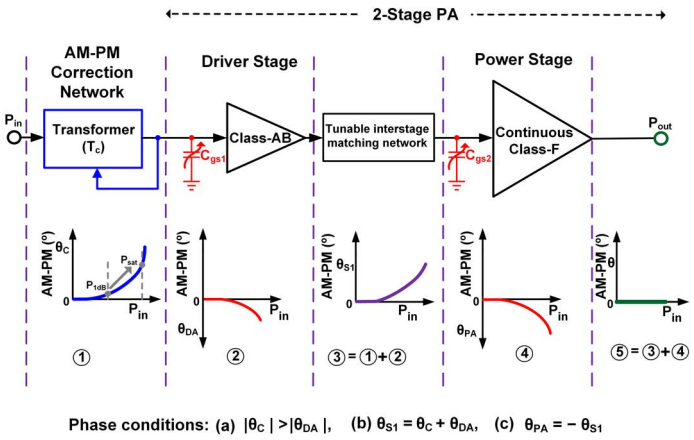

Figure 26.4.1: Architecture of the proposed AM-PM-distortion correction technique for mmW CMOS PA.

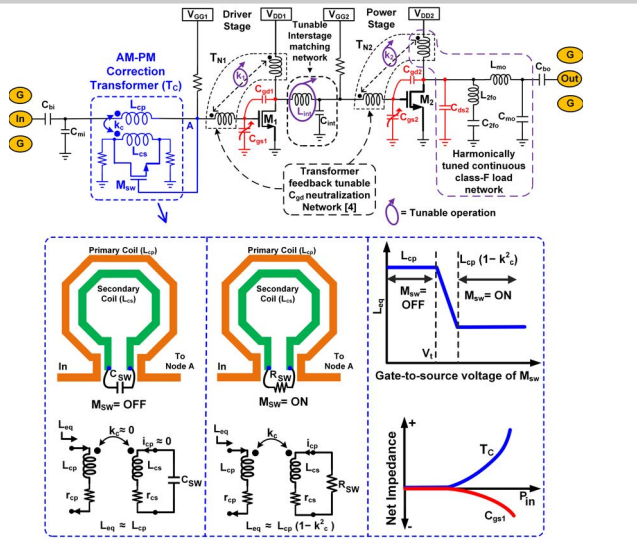

Figure 26.4.2: Schematic of the proposed 2-stage linear PA network incorporating a transformer based AM-PM-distortion correction network.

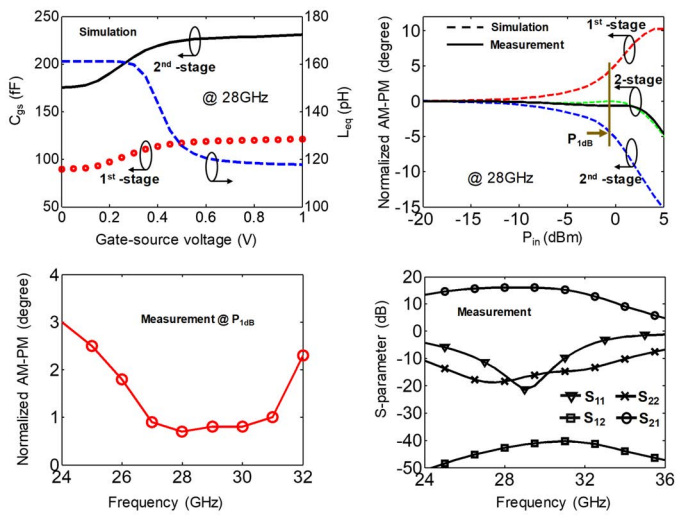

Figure 26.4.3: Results of C_{gs}, L_{eq}, AM-PM, and small-signal S-parameters.

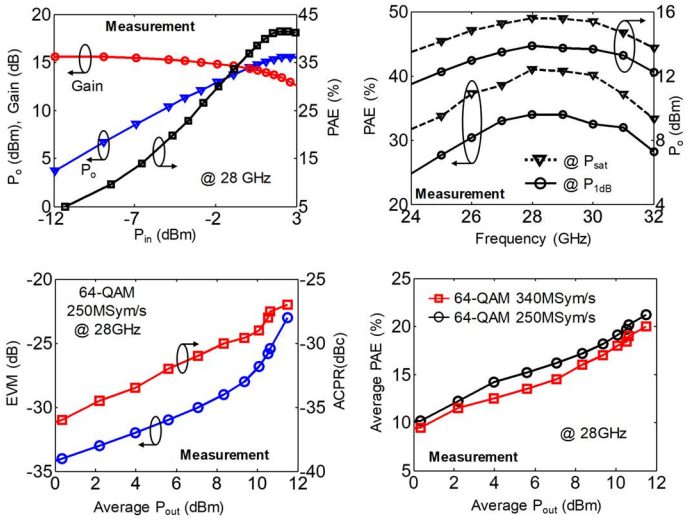

Figure 26.4.4: Measurement results of large-signal and linearity metrics.

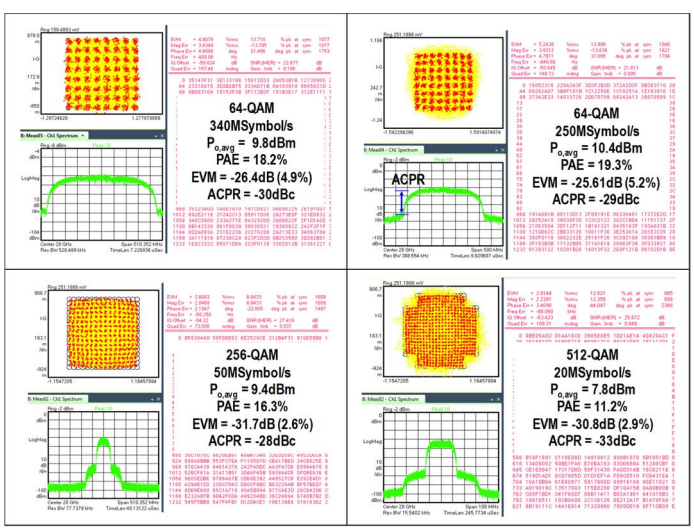

Figure 26.4.5: Measurement results of demodulated signals at 28GHz.

Ref.	This Work	JSSC'16 [6]	ISSCC'17 [7]	TMTT'16 [8]	RFIC'17 [9]
Tech.	65nm CMOS	28nm CMOS	130nm SiGe	28 nm CMOS	28nm CMOS
Freq. (GHz)	28	30	28	28	34
V_{DD} (V)	1.1	1.0	1.5	1.1	0.9
Gain (dB)	15.8	15.7	18.2	10	20.8
$P_{o,1dB}$ (dBm)	14	13.2	15.2	14	13.4
$P_{o,sat}$ (dBm)	15.6	14	16.8	14.8	16.6
PAE_{1dB} (%)	34.7	34.3	19.5	35.2	12.6
PAE_{max} (%)	41	35.5	20.3	36.5	24.2
AM-PM (deg.) @P_{1dB}	0.7	NA*	NA	NA	1.1#
Modulated Signal Measurement Results	64-QAM 340Msym/s +9.8dBm -26.4dB EVM -30dBc ACPR 18.2%PAE	64-QAM 250Msym/s +4.2dBm -25dB EVM -26.4dBc ACPR 9%PAE	64-QAM 500Msym/s +9.2dBm -27dB EVM -28.4dBc ACPR NA	64-QAM 80Msym/s +6.8dBm -27.4dB EVM -34dBc ACPR 16.5% PAE	64-QAM 337Msym/s +10.1dBm -25dB EVM -32.1dBc ACPR 5.8% PAE
	256-QAM 50Msym/s +9.4dBm -31.7dB EVM -28dBc ACPR 16.3%PAE	NA	NA	NA	NA
Active Area (mm^2)	0.24	0.16	1.76**	0.28	0.16
Topology	Transformer based AM-PM correction	Inductive source degeneration	Doherty	2nd harmonic short, common-source	PMOS varactor based AM-PM compensation

*Including pads (total area). *Not available. #Estimated from graph

Figure 26.4.6: Comparison with mmW silicon PAs.

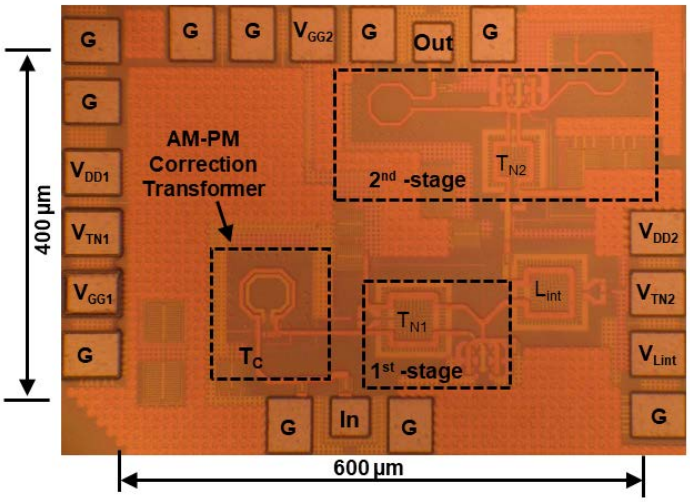

Figure 26.4.7: Die micrograph in a 65nm CMOS technology.

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