Frequency-channelized Mismatch-shaped Quadrature Data Converters for Carrier Aggregation in MU-MIMO LTE-A

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***Abstract*—Emerging wireless standards aggregate information by selecting combinations of contiguous or non-contiguous channels, thereby enabling wider transmission bandwidths, and hence, higher data rates. Frequency-interleaved analog-to-digital conversion (FI-ADC) is an attractive emerging technique for carrier aggregation receivers because it facilitates an efficient way to dynamically vary the receiver bandwidth in order to address the many possible channel combinations. Compared to their time-interleaved counterparts, the specifications of the samplers in the parallel channels in FI-ADCs are significantly relaxed, thereby resulting in lower overall power consumption in the receiver. This work extends the FI-ADC concept to the quadrature frequency-interleaved oversampled data converter (QFI-ADC) to achieve greater aggregate data rates. Previously, digital-to-analog converter (DAC) and other inter-channel mismatches have limited the performance of QFI-ADCs. In this paper, we propose a low-complexity element rotation algorithm (ERA) to mitigate DAC mismatches. The ERA is synthesized from the corresponding mismatch transfer function using a rigorous mathematical procedure which is shown to be applicable generally to low-pass, high-pass, band-pass and quadrature ERAs. Simulations confirm that the resulting low-complexity quadrature ERAs have advantages over previously proposed approaches in both performance and hardware complexity. An additional gain calibration technique alleviates image folding due to gain and timing mismatches between the quadrature DAC elements, which yields higher SNDR.**

***Index Terms*—Quadrature mismatch shaping, sigma-delta ADC, dynamic element matching, element rotation algorithm, gain calibration.**

I. Introduction

Cloud technologies, the internet-of-things (IoT) and emerging multi-user multi-input multi-output (MU-MIMO) standards, such as *LTE-A* and *IEEE 802.16m*, have increased data rate demands, which exacerbates crowding of the radio spectrum and complicates physical layer design. Spectrum usage efficiency has improved, but this alone cannot provide the targeted data rates. Carrier aggregation (CA) is proposed to overcome this limitation; it enables the simultaneous use of more than one carrier frequency (i.e., more than one channel), which increases the overall bandwidth. The channels may be selected from among contiguous or non-contiguous intra- or inter-band options. Current state-of-the-art implementations require multiple transceivers, which adds cost and complexity, particularly to user terminals where space and power dissipation are key considerations.

Wide-band ADCs have been identified as the primary performance limiters, especially in non-contiguous inter-band scenarios. Parallel channel sampling based on the generalized sampling theory is an effective method for high-speed A/D conversion. Parallel architectures including time-interleaved ADCs (TI-ADC) [1]-[6], quadrature mirror filter bank (QMFB) [7] and hybrid filter bank (HFB) structures [8]-[10], and hybrid frequency conversion architectures [11], have demonstrated impressive performance because of their simplicity in achieving parallelism and equalization. Many of these architectures (e.g., Fig. 1(a)) require high-speed sample-and-hold (S/H) stages, wherein gain and offset mismatches between parallel time-interleaved channels cause distortion products, which necessitate spectral reconstruction using digital calibration techniques [12], [13].

A frequency-interleaved analog-to-digital converter (FI-ADC) relaxes the requirements on each S/H stage by sampling the wideband input signal after it is decomposed into sub-bands [8], [11], [14] (Fig. 1 (a)). This approach increases flexibility in the frequency domain and reduces sensitivity to timing mismatches between parallel S/H stages. In the time-interleaved approach, the Nyquist-rate ADCs must exhibit maximum precision at all frequencies even though it is required at only the highest signal frequency. On the other hand, noise-shaping Σ-Δ converters feature an inherent trade-off between sampling frequency and resolution, which enables energy optimization of sampling rate versus quantization accuracy; i.e., only the frequencies of interest have suppressed quantization noise [15], [16]. A quadrature Σ-Δ modulator enables digitization of the in-phase and quadrature-phase components using two identical ADCs. The resulting complex converter architecture features several performance advantages over its real counterpart including immunity to DC offsets and flicker noise [17]-[19]. A parallel bank of quadrature ADCs enables the frequency-agile reception of narrowband signals in adjacent (or non-contiguous) concurrent bands (Fig. 1(a)) [8], [11], [14]. A drawback of complex-valued signal processing is *I/Q* imbalance caused by coefficient mismatches between the in-phase and quadrature-phase channels. This imbalance causes

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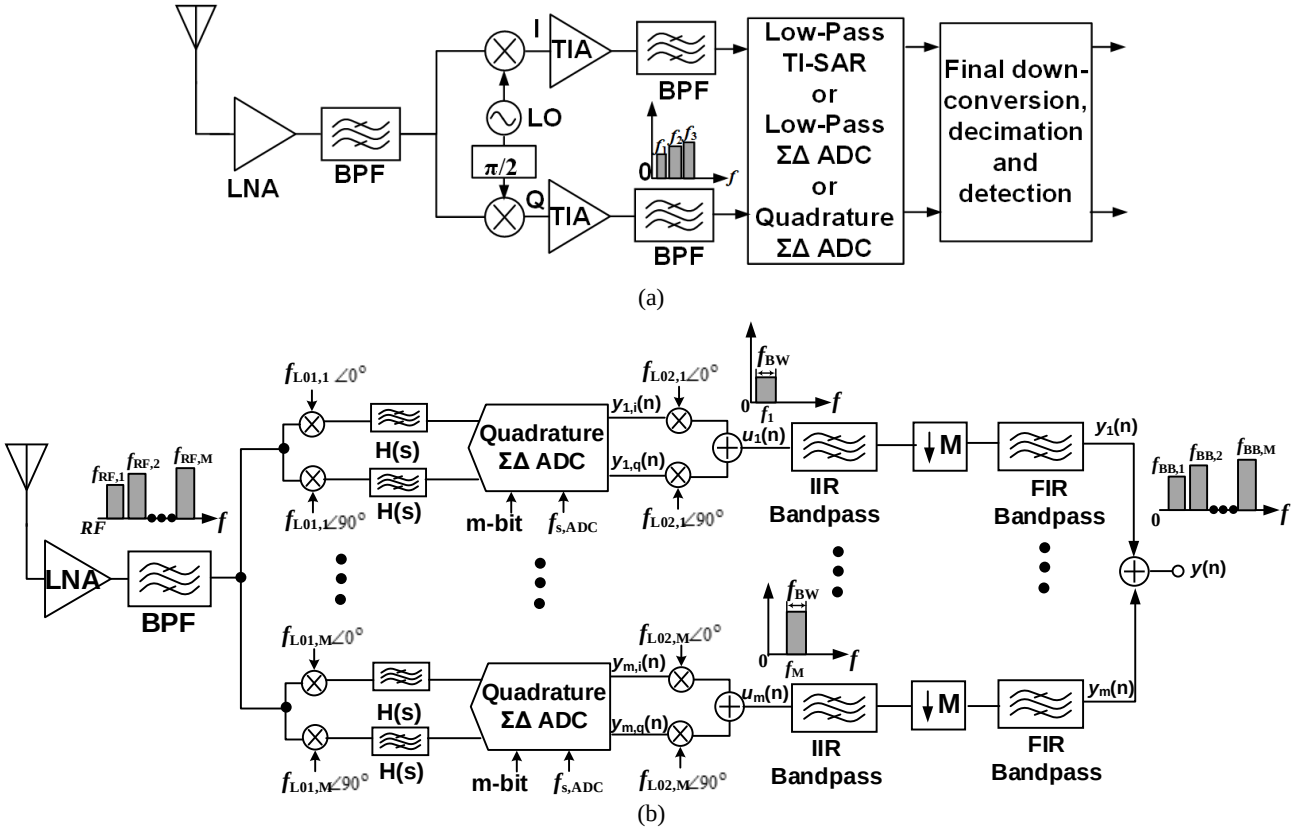


Fig. 1. (a) Possible quadrature frequency-channelized receiver signal paths, and (b) the proposed M-channel quadrature frequency-interleaved ADC (QFI-ADC) architecture with mismatch shaping and *m*-bit feedback for gain calibration.

in-band image-frequency interference which degrades the overall signal-to-noise ratio (SNR) of the receiver. In addition, process, voltage, and temperature (PVT) variations between the analog and the digital filter coefficients of the QFI-ADC limit the reconstruction accuracy, which introduces aliasing artifacts and reduces its advantages over TI-ADC architectures. Recent works have described a digital post-compensation scheme to mitigate mirror-frequency interference and gain/offset mismatches for the synthesis filter bank for quadrature ADCs [11], [20]. Although impressive results are achieved, digital calibration is necessary and the higher throughput rates foreseen for wideband next-generation architectures may require high-f_T CMOS processes. In this paper, a low-latency mismatch-shaping algorithm and a low-power multi-rate least-mean-squares (LMS) digital calibration scheme [21] are combined to achieve greater efficiency. The mismatch-shaping algorithm, which features low hardware complexity, is embedded in the quadrature ADC to mitigate gain and offset *I/Q* mismatches as well as the intra- and inter-channel mismatches between frequency-interleaved channels. The low-power LMS-based digital calibration scheme alleviates aliasing effects from the mirror frequencies.

II. Frequency Channelization Architecture And Quadrature Band-pass Σ-Δ ADC

A quadrature frequency-channelized receiver with several ADC options is shown in Fig. 1(a). This work aims at reducing the effects of mismatches on the QFI-ADC of Fig. 1(b), wherein a wideband signal is input to M = 4 channels centered symmetrically about f_{IF}. Thus, the aggregate input bandwidth, Ω_B, is the sum of the individual channel bandwidths.

Each of the four channels comprises two paths that frequency translate the input signal centered at carrier frequency f_1, f_2, f_3, or f_4 to corresponding in-phase and quadrature-phase components. The quadrature signals are analog band-pass filtered by *H(s)* and digitized using a quadrature Σ-Δ converter. The oversampled digital outputs are down converted to baseband, bandpass filtered, decimated by *M*, and recombined to reconstruct a digital representation of the wideband analog input signal.

When fully deployed, the system functions as an ADC digitizing a wideband signal of bandwidth Ω_B; alternatively, some of the parallel channels may be turned off when less carrier aggregation is used. The *M*-channel architecture of Fig. 1(b) has *2M* identical band-pass filters and *M* identical quadrature band-pass oversampled Σ-Δ converters. Each converter operates at a sampling frequency of $2OSR(\Omega_B/M)$, where *OSR* is the oversampling ratio.

The analysis of complex data converters was treated by Tang, et al. [18] wherein a third-order complex band-pass modulator Fig. 2(a)) was synthesized from a third-order real band-pass modulator with each real integrator, $H_N(z)=z^{-1}/(1-z^{-1})$ replaced by its complex counterpart, $H_C(z)=Pz^{-1}/(1-Pz^{-1})$, with $P = \exp(2\pi f_{IF}/f_s)$ as shown. Thus,

$$\begin{aligned} Y &= Y_I + jY_Q \\ &= \left(X_I + jX_Q\right)z^{-3} + \left(1-Pz^{-1}\right)^3\left(Q_I + jQ_Q\right) \end{aligned} \tag{1}$$

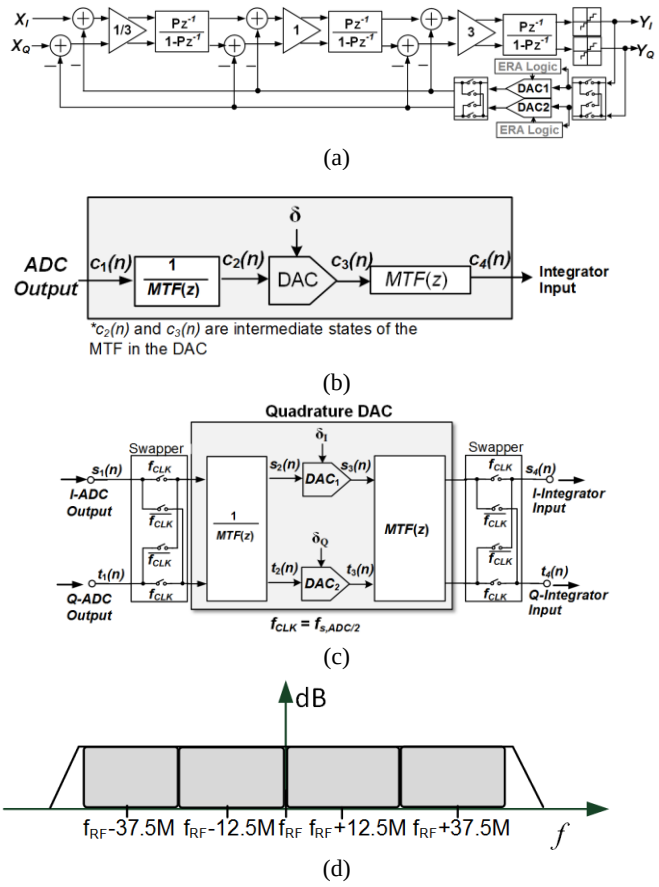


Fig. 2. (a) The third-order ΣΔ modulator used in this work, and (b) a conceptual and (c) a detailed realization of the mismatch-shaping ERA; (d) spectral distribution before down conversion.

has a real signal transfer function, $STF = 1$, and a complex noise transfer function, $NTF = N_r + jN_i = \left(1 - Pz^{-1}\right)^3$.

The performance of complex modulators is sensitive to *I*/*Q* mismatches [18], which introduce differential-mode errors in the signal and noise transfer functions, which, in turn, corrupt the signal band and degrade SNR. Although SNR degradation can be reduced using a DSP solution [22], the concomitant folding of quantization noise into the signal band is problematic. This effect is mitigated by cascading an oversampled complex modulator in the first stage with a Nyquist-rate pipeline converter in the second stage followed by adaptive noise cancellation digital logic [18].

This paper demonstrates techniques that shape DAC integral non-linearity errors similarly as the NTF of a Σ-Δ loop shapes quantization errors [23]-[27]. The mismatch transfer function (MTF) is made similar to the NTF to maximize SNR. One mismatch shaping method is the element rotation algorithm (ERA), implemented conceptually in Fig. 2(b). Other algorithms for high-order mismatch shaping are vector-based [26], [28] and tree-structured/butterfly-shuffler DAC-based methods [23], [27], [29], [30]. The hardware requirements for some of these techniques are compared below.

Section III gives a brief survey of mismatch shaping techniques for quadrature band-pass and frequency-interleaved ADCs. Section IV introduces a general approach for deriving an ERA, and extends it to quadrature applications. Section V describes mismatch shaping in an FI-ADC. Simulation results for a single-channel quadrature ADC and a two-channel FI-ADC are presented in Section VI, and hardware versus performance trade-offs for state-of-the-art ERAs versus the proposed algorithm are given in Section VII. Section VIII considers the inverse objective of finding the MTF for a given ERA, and Section IX concludes this contribution.

III. Mismatch Shaping

The proposed MTF is evaluated first for a single-channel quadrature band-pass Σ-Δ converter [19] and then for a dual-channel FI-ADC. A conceptual model of the mismatch-shaping ERA is depicted in Fig. 2(b). The ADC output, $c_1(n)$, is pre-filtered by the inverse of MTF with digital output, $c_2(n)$. The DAC output, $c_3(n)$, is then post filtered by MTF, with analog output, $c_4(n)$. Ideally, the input signal is unaltered, but errors introduced by the DAC, δ, are shaped by the MTF. A literal implementation of Fig. 2(b) is problematic because the input to the DAC, $c_2(n)$, may grow without bound for certain MTFs.

Several approaches are functionally equivalent to the conceptual implementation including ERAs for low-pass [31], [32], real band-pass [33] and quadrature modulators [34], [35]-[36]. Maurino and Papavassiliou [35] used quadrature mixers to frequency translate the input/output signals into low-pass mismatch shaping DACs with good results. But, that approach exhibits high latency and is relatively complex. Prior-art quadrature ERAs require less hardware but do not faithfully represent the quadrature MTF [34], [36].

The systematic derivation of an ERA for a desired MTF starting from Fig. 2(b), or from given knowledge, has not been developed for advanced architectures such as a quadrature FI-ADC. This paper extends the approach in [19] to synthesize an optimum quadrature ERA with less hardware than more general mismatch shaping schemes [24]. Behavioral simulations confirm the advantages of the proposed ERA over the previous implementations used for single- or multi-channel frequency-channelized quadrature receivers [20], [34]. The general approach is also applicable to low-pass, high-pass and real band-pass architectures [19].

Energy efficiency is increased using a gain calibration technique that works with the multi-band quadrature ERA to mitigate image-frequency interference; specifically, a multi-rate implementation of a sign-sign LMS algorithm is employed [21]. The extra DSP circuitry adds latency in the Σ-Δ loop, which reduces the available amplifier settling time. The additional switches in the unit cells reduce the bandwidth and increase layout challenges. These issues are critical in the design of high-speed wideband multi-band Σ-Δ converters for LTE-Advanced and other future WiFi standards. The combination of analog mismatch shaping and digital calibration enables complex quadrature receivers with relatively low hardware complexity.

IV. Element Rotation Algorithms

A. General Approach

An $MTF(z) = 1 + bz^{-k}$, where k is an integer and $b \in \{\pm 1, \pm j\}$, is chosen so that the DAC can be realized using two-level elements. The output in Fig. 2(b) is [19]:

Table I: Quadrature ERA calculation: Step 1

Cycle	$s_1 + jt_1$	$c_3 = s_3 + jt_3$
n		$U + jV$
n+1	$u_1 + jv_1$	$-(V - u_1) + j(U + v_1)$
n+2	$u_2 + jv_2$	$-(U + v_1 - u_2) - j(V - u_1 - v_2)$
n+3	$u_3 + jv_3$	$(V - u_1 - v_2 + u_3) - j(U + v_1 - u_2 - v_3)$
n+4	$u_4 + jv_4$	$(U + v_1 - u_2 - v_3 + u_4) + j(V - u_1 - v_2 + u_3 + v_4)$

Quadrature ERA calculation: Step 2

s_4	t_4
$-\sum_{i=1}^{V-u_1}(1+\delta_{1i})+\sum_{i=1}^{V}(1+\delta_{2i}) = u_1 + \sum_{i=V-u_1+1}^{V}\delta_{1i}$ DAC1-index moves from V to $V-u_1+1$; i.e. ←	$\sum_{i=1}^{U+v_1}(1+\delta_{2i})-\sum_{i=1}^{U}(1+\delta_{1i}) = v_1 + \sum_{i=U+1}^{U+v_1}\delta_{2i}$ DAC2-index moves from $U+1$ to $U+v_1$; i.e. →
$-\sum_{i=1}^{U+v_1-u_2}(1+\delta_{1i})+\sum_{i=1}^{U+v_1}(1+\delta_{2i}) = u_2 + \sum_{i=U+v_1-u_2+1}^{U+v_1}\delta_{2i}$ DAC2-index moves from $U+v_1$ to $U+v_1-u_2+1$; i.e. ←	$-\sum_{i=1}^{V-u_1-v_2}(1+\delta_{2i})+\sum_{i=1}^{V-u_1}(1+\delta_{1i}) = v_2 + \sum_{i=V-u_1-v_2+1}^{V-u_1}\delta_{1i}$ DAC1-index moves from $V-u_1$ to $V-u_1-v_2+1$; i.e. ←
$\sum_{i=1}^{V-u_1-v_2+u_3}(1+\delta_{1i})-\sum_{i=1}^{V-u_1-v_2}(1+\delta_{2i}) = u_3 + \sum_{i=V-u_1-v_2+1}^{V-u_1-v_2+u_3}\delta_{1i}$ DAC1-index moves from $V-u_1-v_2+1$ to $V-u_1-v_2+u_3$; →	$-\sum_{i=1}^{U+v_1-u_2-v_3}(1+\delta_{2i})+\sum_{i=1}^{U+v_1-u_2}(1+\delta_{1i}) = v_3 + \sum_{i=U+v_1-u_2-v_3+1}^{U+v_1-u_2}\delta_{2i}$ DAC2-index moves from $U+v_1-u_2$ to $U+v_1-u_2-v_3+1$; i.e. ←
$\sum_{i=1}^{U+v_1-u_2-v_3+u_4}(1+\delta_{1i})-\sum_{i=1}^{U+v_1-u_2-v_3}(1+\delta_{2i}) = u_4 + \sum_{i=U+v_1-u_2-v_3+1}^{U+v_1-u_2-v_3+u_4}\delta_{2i}$ DAC2-index moves from $U+v_1-u_2-v_3+1$ to $U+v_1-u_2-v_3+u_4$; i.e. →	$\sum_{i=1}^{V-u_1-v_2+u_3+v_4}(1+\delta_{2i})-\sum_{i=1}^{V-u_1-v_2+u_3}(1+\delta_{1i}) = v_4 + \sum_{i=V-u_1-v_2+u_3+1}^{V-u_1-v_2+u_3+v_4}\delta_{1i}$ DAC1-index moves from $V-u_1-v_2+u_3+1$ to $V-u_1-v_2+u_3+v_4$; i.e. →

$$c_4(n) = mtf(n) * c_3(n) = c_3(n) + bc_3(n-k) \quad (2)$$

A corresponding ERA is deduced using a two-step process:

- Step 1: Ideally, $c_4(n)$ is equal to $c_1(n)$. Thus, (2) is solved for $c_3(n)$ terms of the input sequence:

$$c_3(n) = c_4(n) - bc_3(n-k) \rightarrow c_1(n) - bc_3(n-k) \quad (3)$$

- Step 2: Eqn. (3) is used to calculate the pointer, $c_3(n)$, at each time step using the input values, c_1. Assume an initial value of $c_3(n) = U$. Based on the value of $c_1(n)$ (e.g., u_1), the selected DAC elements start from $U \pm u_1$ where each selected cell adds ± 1 to the output for the $(n+1)^{st}$ time step. Assuming a random deviation, δ_i, from the ideal for each cell, an additional error term, $+\mathrm{sgn}(u_1)(\delta_i)$, is also added which eventually limits the performance of the mismatch-shaping algorithm. By evaluating (2) for several time steps, the usage pattern of the DAC elements is determined, which yields the element *usage algorithm*. The rotational part of the ERA arises from realizing the linear array in a circular form with a limited number of DAC cells. After the element usage is determined, (2) is used to find the error introduced by DAC mismatches at each time step.

B. Mismatch-shaping ERA for Quadrature Band-pass ADC

The approach described above is now extended to an ERA for the quadrature $MTF(z) = 1 - jz^{-1}$ which has a zero only at $+f_s/4$ (and not at $-f_s/4$). Eqns. (2) and (3) are re-written for the quadrature case of Fig. 2(c) as [19]:

$$\begin{aligned} s_4(n) &= s_3(n) + t_3(n-1) \\ t_4(n) &= t_3(n) - s_3(n-1) \end{aligned} \quad (4)$$

$$\begin{aligned} s_3(n) &= s_4(n) - t_3(n-1) \rightarrow s_1(n) - t_3(n-1) \\ t_3(n) &= t_4(n) + s_3(n-1) \rightarrow t_1(n) + s_3(n-1) \end{aligned} \quad (5)$$

where $c_1 = s_1 + jt_1$, $c_3 = s_3 + jt_3$ *and* $c_4 = s_4 + jt_4$.

- Step 1: Values of the complex-valued pointer, $c_3 = s_3 + jt_3$, are calculated using (5) for the complex-valued inputs, $c_1 = s_1 + jt_1$ (Table 1).
- Step 2: The real and imaginary parts of $c_4(n)$ are first evaluated using Table 1 and then (5) to sum the contributions of the DAC elements using the indices given by s_3 and t_3. Note that there are two DACs (DAC_1 and DAC_2), and, hence, two different sets of unit cells with mismatches, δ_{1i} and δ_{2i}. An additional assumption, $\delta_{1i} = \delta_{2i}$ (for all i), has been made in Step 2 in Table 1. This assumption states that the DAC_1 and DAC_2 paths are identical and only inter-element mismatches within each DAC are addressed by the quadrature ERA. This assumption is necessary to avoid contention—the simultaneous use of a single DAC element by both DAC_1 and DAC_2. It is essential to note that this assumption is needed only to derive the proposed quadrature ERA; it also works in realistic cases where $\delta_{1i} \neq \delta_{2i}$ so long as digital calibration is added to equalize the random DAC gain mismatches. This issue is addressed later.

Step 2 in Table 1 yields the required element usage patterns as exemplified in Fig. 3(a). Note that the DAC indices are assumed to be increasing (decreasing) to the right (left). For example, when the DAC_1 index moves from V in cycle n to $V-u_1+1$ in the next cycle, the index moves to the left (since $V-u_1+1 \leq V$) as indicated by the left-pointing arrow.

Two essential aspects of the proposed ERA should be emphasized: The element usage in each DAC changes direction after every two cycles, and, thus repeats after four cycles. And, there is a one cycle time difference (i.e., a 90° phase difference), between the direction changes in the two DACs. This is a key difference from previous quadrature ERAs [35]-[36]. Another key aspect of this ERA is the per-cycle DAC swapping; i.e., if DAC_1 (DAC_2) is used in the I-path (Q-path) in the current cycle,

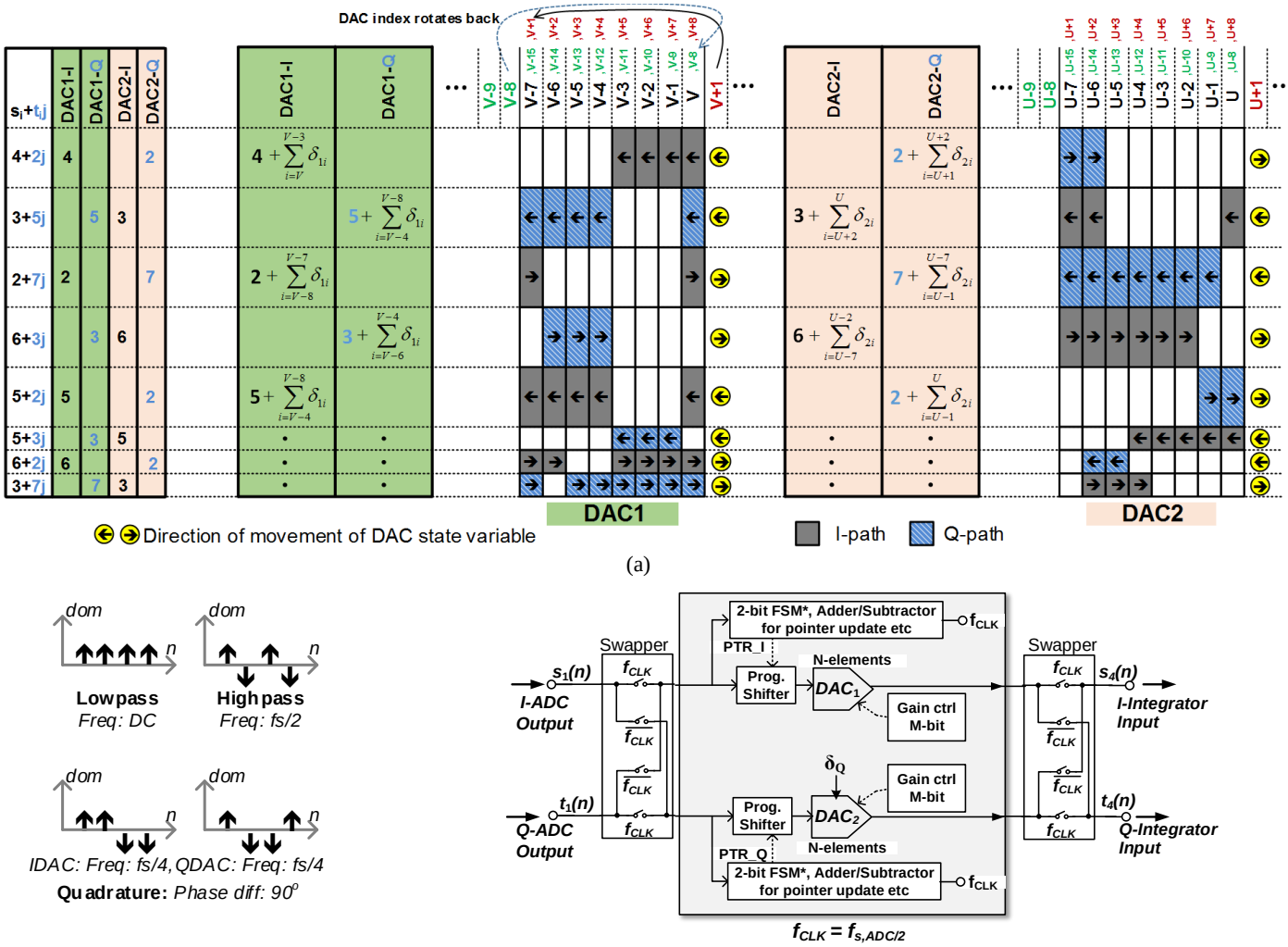


Fig. 3 (a) Proposed quadrature ERA details, demonstrated with numerical example using equations from Step2 of Table I, (b) Direction of movement (*dom*) summary for different ERAs, and (c) Implementation of the proposed ERA with m-bit gain calibration through LMS algorithm.

DAC_2 (DAC_1) will be used in the *I*-path (*Q*-path) in the next cycle. Further insight is gained from Fig. 3(b) where a critical frequency is identified from the DAC cell selection direction of movement for two traditional ERAs and the proposed quadrature ERA. Specifically, a low-pass ERA has a zero at DC (no direction changes in *dom*) and a high-pass ERA has a zero at $f_s/2$ (*dom* changes every clock cycle). In the proposed ERA algorithm, *dom* alternates after every two clock cycles which corresponds to a zero in the MTF at $f_s/4$.

C. *Proposed Mismatch Shaping ERA for FI-ADC*

The quadrature ERA algorithm is now extended to FI-ADCs. Analog mismatch shaping mitigates intra-channel mismatches because the ERA swaps the roles of the DACs from one cycle to the next. However, this creates a cycle-to-cycle gain mismatch; i.e., if G_{DAC1} and G_{DAC2} are the DAC gains with $G_{DAC1} \neq G_{DAC2}$, then $G_{DAC1} + jG_{DAC2}$ in one cycle is not equal to $G_{DAC2} + jG_{DAC1}$ in the next. Thus, LMS digital gain calibration is used so that $G_{DAC1} \approx G_{DAC2}$.

For a multi-channel FI-ADC, it is necessary to extend these techniques for more than two DACs. For example, in a two-channel implementation (at F_{C1} and F_{C2}), there are four DACs with independent mismatches; i.e., $G_{DAC1,Fc1} \neq G_{DAC2,Fc1} \neq G_{DAC1,Fc2} \neq G_{DAC2,Fc2}$. The proposed ERA shapes these intra-DAC mismatches for both channels with an MTF = $(1 - jz^{-1})$.

As a consequence of the extended ERA, and before digital calibration, the two-channel FI-ADC has different DAC gains in alternate odd/even cycles (Table II). Digital LMS gain calibration makes $G_{DAC1,Fc1} \approx G_{DAC2,Fc1} \approx G_{DAC1,Fc2} \approx G_{DAC2,Fc2}$.

Table II. Two-channel FI-DAC Gains with Mismatches

Clock Cycle	Effective Gain
Even	$G_{DAC1,Fc1} + jG_{DAC2,Fc1}$ $G_{DAC1,Fc2} + jG_{DAC2,Fc2}$
Odd	$G_{DAC2,Fc1} + jG_{DAC1,Fc1}$ $G_{DAC2,Fc2} + jG_{DAC1,Fc2}$

V. Clock Jitter and Inter-Channel Mismatches

All of the frequency-interleaved channels are sampled using clock signals derived from the same reference; thus, there is less sensitivity to clock jitter than in a TI-ADC [11]. However, the local oscillator used to perform the down-conversion (Fig. 1(b))

must generate multi-band quadrature clock signals with low jitter. Such LO jitter can be modeled as sinusoidal tones as described by Ding, et al. [37]

$$LO_k(t) = e^{-j\left(2\pi k \frac{t}{T_i} + jitter_K(t)\right)} \quad (6)$$

An analysis of the effects of jitter for square-wave-like LO generators used with harmonic-reject mixers in frequency-channelized receivers is detailed by Forbes and Gharpurey [38].

The mismatch noise shaping due to the odd/even cycle swapping of the DACs along with the digital LMS gain calibration techniques described above also can be used to correct input *I*/*Q* timing errors. That is, the effects of mismatches at the inputs to the quadrature ADC are analyzed with the same mismatch errors moved into the feedback DACs.

Suppose the even samples (*I*-phase) in Fig. 1(b) occur at the correct times while the odd samples (*Q*-phase) have a timing error, θ. Begin the analysis of the effects of this timing error when multiplexing the even and odd streams by considering an input signal sampled at f_0:

$$S(nT_s) = \cos(2\pi n\, f_0 / f_s) \quad \text{where } f_s = 1/T_s \quad (7)$$

Next, extract the odd and even components of (7) and up sample both by 2X. Only the terms between 0 and 2π are considered in the extracted terms assuming $f_0 < f_s/2$; it is important to note that two of the terms are due to aliasing. With the assumed phase error between even and odd samples, θ, where $\theta = 2\pi f_o \Delta t$, the even and odd parts are

$$S_e(nT_s) = 0.5\cdot[e^{(j2\pi n f_0/f_s)} + e^{(j2\pi n(f_s/2-f_0)/f_s)}] \quad (8)$$

$$S_o(nT_s) = 0.5\cdot[e^{(j2\pi n f_0/f_s + 2\pi f_0/f_s + \theta)} + e^{(j2\pi n(f_s/2-f_0)/f_s - 2\pi f_0/f_s - \theta)}]$$

Thus, the image terms are aliases of the desired signal. Given $S_o[(n-1/2)T_s] = S_0[(n-1)T_s]$, the equivalent sampled output at t = nT_s is

$$S(nT_s) = S_e(nT_s) + S_o[(n-1)T_s]$$

where

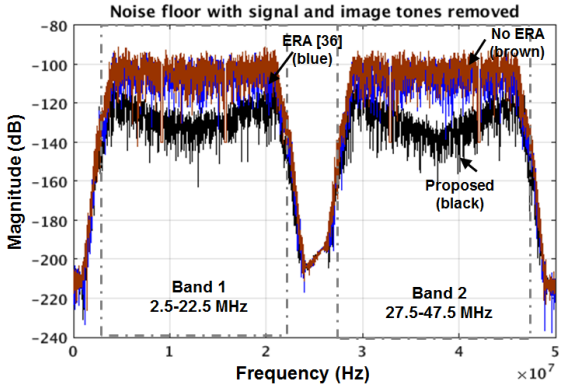
$$S_0[(n-1)T_s] = 0.5\cdot\begin{bmatrix} e^{(j2\pi n f_0/f_s - 2\pi f_0/f_s + 2\pi f_0/f_s + \theta)} \\ + e^{(j2\pi n(f_s/2-f_0)/f_s - 2\pi f_0/f_s - \theta)} \end{bmatrix}$$

$$= 0.5\cdot[e^{(j2\pi n f_0/f_s + \theta)} + e^{(j2\pi n(f_s/2-f_0)/f_s)} - \pi + \theta]$$

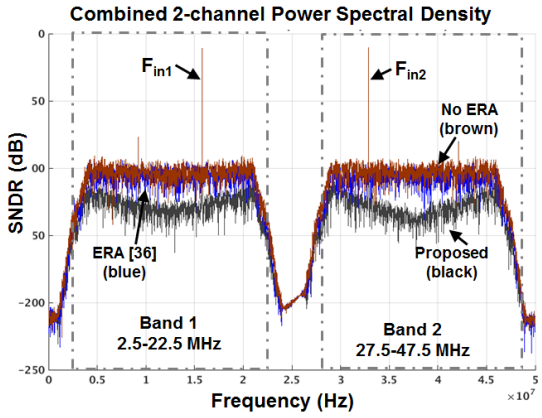
Combining $S_e(nT_s)$ and $S_o((n-1)T_s)$ with $e^{j\theta} \sim (1+j\theta)$ (for small θ) yields

$$S(nT_s) = 0.5\cdot e^{(j2\pi n f_0/f_s)}[2 + j\theta] + 0.5\cdot e^{(j2\pi n(f_s/2-f_0)/f_s)}[j\theta] \quad (9)$$

The second term in (9) dominates the image signal error owing to the phase mismatch between the even and odd sampling instants. The resulting total distortion is $\theta\cdot 0.5 = \pi\cdot f_0\cdot\Delta t$. Also note that the image is rotated by π/2 relative to the image present in the odd-even sequences. Thus, this error can be corrected using either a narrow-band *I*/*Q* digital calibration technique [11], [20], or the same digital LMS gain calibration as shown above in Section VI.B.



(a)



(b)

Fig. 4. (a) Comparison of the reconstructed noise floors: no ERA (brown), ERA [36] (blue), and proposed ERA (black); (b) combined output of the two-channel FI-ADC with 0.5% mismatch. An 8192-point FFT was performed to capture the entire baseband bandwidth of 50 MHz.

VI. Simulation Results

Experimental results are obtained using *Matlab/Simulink*® simulations with the proposed ERA applied to the 3rd-order, 4-bit, quadrature band-pass Σ-Δ ADC of Fig. 2(a). The same architecture is then extended to a two-channel FI-ADC as in Fig. 1(b). Detailed simulations are performed to illustrate the effects of *I*/*Q* gain and phase mismatches along with the improved performance obtained using digital gain calibration. An example frequency allocation of intra-band contiguous channels is shown in Fig. 2(d). For this work, f_{c1} and f_{c2} represent the center frequencies of two adjacent 25 MHz bands at the output of the first RF down-conversion mixer. Two CW tones are chosen at arbitrary frequencies within these bands given by $f_{in} = (k/2^N)f_s$ where *N* is the *N*-point Fast Fourier Transform (FFT), and *k* is chosen to be a prime number (where $k < 2^{N-1}$) to avoid repetitive patterns in the output, and f_s is the ADC sampling frequency.

A. Proposed ERA for Two-channel Quadrature ADC

Behavioral simulations for the 3rd-order 4-bit two-channel FI-ADC based on the architecture in Fig. 1(b) are shown in Fig. 4. The digital reconstruction comprises digital multipliers, adders, up-samplers and FIR filters. Selecting the FI-ADC

center frequency as $f_s/4$ enables multiplication coefficients for the the digital mixers of either 0 or ±1. Thus, no multipliers are required for the digital mixers. Quadrature bandpass filters are the main source of implementation complexity in the digital block. An 8th-order infinite-impulse-response reconstruction filter is used for power-efficiency in *MATLAB*'s Filter Design Analysis and automatic synthesis tools.

For simulations, two contiguous 20 MHz bands with an aggregate bandwidth of 40 MHz and a transition band of 5 MHz were chosen. The chosen sub-bands are centered at f_1 = 212.5 MHz and f_2 = 237.5 MHz. Again, the third-order quadrature band-pass Σ-Δ modulator of Fig. 2(a) is used. Each 20 MHz input band is mixed down to the same IF frequency, f_{IF} =100 MHz, which enables the use of the same quadrature converter design for each. Fourth-order band-pass channel-select filters are used to provide > 40 dB adjacent channel attenuation to negate any in-band image artifacts. Note that a mirror image implementation would allow even lower filter orders due to the intrinsic band-pass nature of its signal transfer function as shown by Schreier and Temes [28].

The power spectral density (PSD) plots show the simulated noise floor (Fig. 4(a)) and the reconstructed output of the two-channel QFI-ADC (Fig. 4(b)). The image frequencies are intentionally notched out by the DSP to allow comparison of the noise floors for the three cases: no ERA, ERA in [36] and the proposed ERA. It can be seen that for the same mismatch (1%), the noise floor after decimation for the proposed ERA has a marked improvement over the other techniques.

A significant decrease in the noise floor and a corresponding increase in *SNDR* is achieved using the proposed ERA for a quadrature band-pass Σ-Δ ADC assuming equal inter-element mismatches (i.e., $\delta_{1i} = \delta_{2i}$ for all i). The *SNDR* improvement is maintained for a wide range of *OSR* values [19]. With $\delta_{1i} \neq \delta_{2i}$ for all i, an image tone appears at $|f_s/4 - f_{in}|$ due to the DAC_1/DAC_2 swapping. Its magnitude depends on the gain imbalance, so it can degrade the overall *SNDR* even though it and the noise floor are substantially reduced using the proposed ERA along with the digital LMS gain calibration presented in the next section. Note that this image tone also appears in a similar manner in previous ERAs [35]-[36]. Herein, mismatch alters the effective gains of DAC_1 and DAC_2 as highlighted by the analysis in the previous section.

Based on the results of Fig. 4(b), it is important to use layout techniques that maximize the matching of the DACs in an FI-ADC; such techniques are highlighted by Kundu, et al. [19]. Perfect matching is statistically impossible so the resulting residual image tone is removed using auxiliary *m*-bit DACs to equalize the gains of DAC_1 and DAC_2, as shown schematically in Fig. 3(c). The implementation of the LMS algorithm based on a multi-rate polyphase filter for Σ-Δ converters is presented in [21].

B. Gain Mismatch Calibration

For a multi-channel FI-ADC, it is necessary to calibrate the gains of each DAC against a common value to maximize overall *SNDR* and reduce/eliminate image tones from the signal bands. It is important to note that the calibration method mentioned here also corrects for *I/Q* phase mismatch (Eqn. (9)) and intra- and inter-channel mismatches in the signal path in addition to DAC gain mismatches by applying a gain correction only to the feedback DACs. However, for simplicity, we will refer to all of these mismatches collectively as "DAC gain mismatches" in this section since they all produce a tone at the same image frequency. An offline version of the gain calibration is implemented here, while an online version is equally feasible albeit with more hardware.

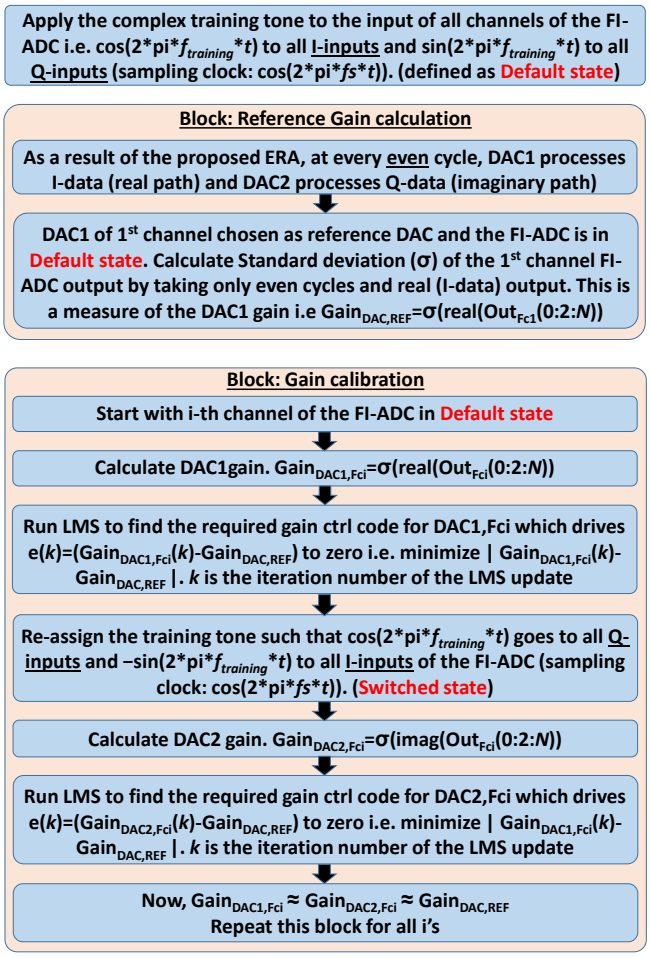


Fig. 5. Proposed gain calibration algorithm steps.

The calibration method requires choosing any one DAC as a reference DAC (DAC_{REF}) from among all of the 2*M* DACs available in the *M* FI-ADC channels. The calibration method sets the gains of all the other DACs equal to that of the reference DAC; i.e., $G_{DACx,Fci} \approx G_{DAC,REF}$ for x = 1:2 and I = 1:M. Without loss of generality, $DAC1_{Fc1}$ is chosen as the reference DAC. The calibration steps are outlined in Fig. 5.

The calibration method is demonstrated first through the simulation of a one-channel FI-ADC. Fig. 6(a) shows how $|Gain_{DAC1,Fci}(k) - Gain_{DAC,REF}|$ varies with $G_{CORR,DAC1}(k)$ where $G_{CORR,DAC1}(k)$ is the gain correction applied to DAC1 and k denotes the LMS iteration number. It also shows the settling behaviors of the gain correction and the error terms. Next, $G_{CORR,DAC1}$ is fixed at 0.999654, the optimum value found, and the calibration continues to determine the optimum value for $G_{CORR,DAC2}$. As $G_{CORR,DAC2}$ moves towards its optimum value, the *SNR*(single channel) of the *i*-th channel increases as the image tone decreases. This behavior is illustrated in Fig. 6(b).

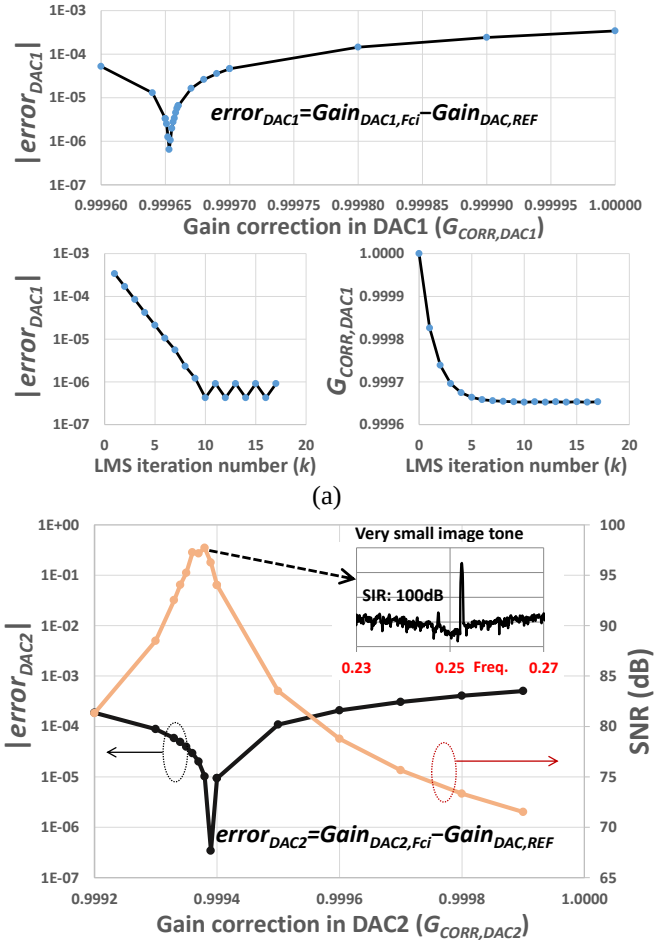


Fig. 6. (a) Variation of $|Gain_{DAC1,Fci}(k) - Gain_{DAC,REF}|$ with $G_{CORR,DAC1}(k)$ and its LMS convergence; (b) optimized *SNR* after calibration with *OSR* = 32 for a 3rd-order 4-bit ADC.

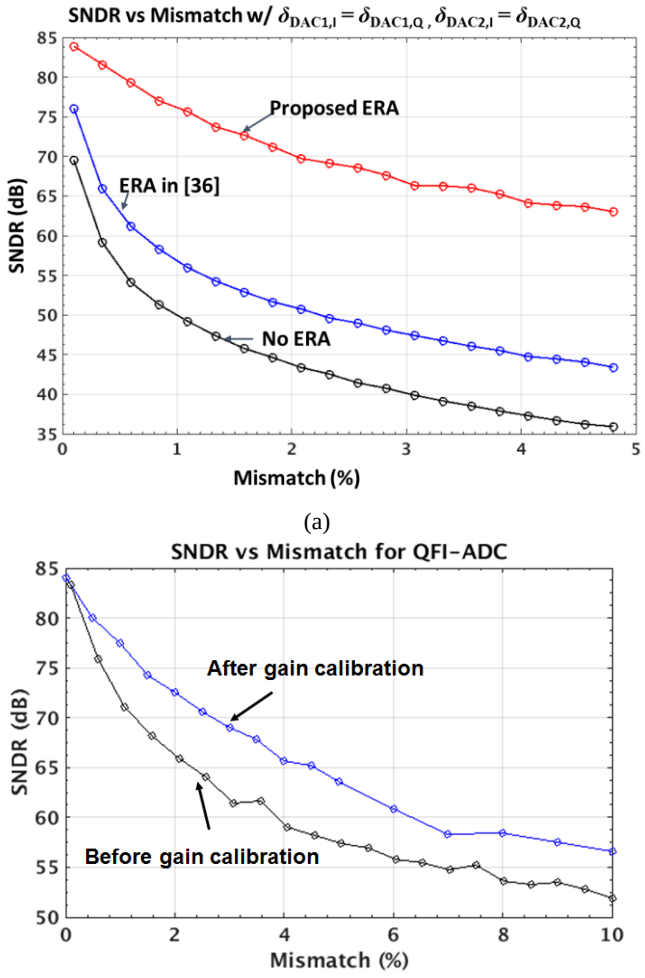


Fig. 7. (a) Reconstructed two-channel *SQNR* versus inter-element *I*/*Q* mismatches (prior to back-end DSP) for different ERA schemes (image tones are notched out); (b) Gain coefficient correction enables up to a 2-bit performance improvement for the case with unequal DAC mismatches.

The LMS-optimized *SNR* (96.27 dB at OSR = 32) is close to the single-channel maximum *SNR* (97.71 dB) as determined by sweeping $G_{CORR,DAC2}$ (Fig. 6(b)), which verifies the efficacy of the proposed approach.

Fig. 7(a) shows simulated *SQNR* in the presence of intra-DAC (DAC_I/DAC_Q) mismatches for a two-channel FI-ADC. The effect of the image due to mismatch is studied for the three ERA cases as shown; generally, the proposed ERA performs better showing about a 15 dB increase in *SQNR*. For large mismatches, the *SQNR* is only 8 bits, but an extra bit is recovered using the digital LMS gain calibration algorithm as shown in Fig. 7(b). The proposed scheme operates with mismatches up to 10% but the increase in the quantization noise floor and incomplete image cancellation limits the *SQNR* with digital calibration at higher mismatches. Techniques for improvement are under investigation including the use of a multi-rate LMS algorithm to correct mismatches between the analysis and synthesis filters [20].

VII. Hardware Overhead vs. Performance

The extra digital signal processing in the DAC adds latency in the Σ-Δ loop, which reduces the available settling time. Also, the additional switches within the DAC unit cells required in a complex DAC reduce bandwidth and create layout difficulties. These issues are critical in high-speed Σ-Δ converters [39].

Table III compares the proposed ERA for a 4-bit Σ-Δ ADC (including calibration hardware with M = 8) to a first-order reduced-complexity butterfly shuffler and a first-order tree-structured complex DAC [23], [30]. Note that hardware reduction techniques [40] have been applied to the latter, where appropriate, in order to make a fair comparison. The proposed scheme is superior in terms of hardware complexity, and, therefore, better suited to high-speed modulators while achieving similar first-order mismatch shaping performance. [35]-[36] have similar hardware complexity and latency, but their performance is inferior to the proposed scheme. Although it employs digital calibration to mitigate mismatches between the *I* and *Q* path gains, the significant performance advantages outweigh the additional hardware in many practical cases.

VIII. Reverse Problem: Deducing MTF From ERA

The significance of the previous systematic approach is enhanced by solving the reverse problem; i.e., deriving the *MTF* from a given ERA. Note that it is not always possible to obtain

Table III. Performance versus Hardware Overhead

	Digital Transistor count	Digital Latency (FO4 inv. delays)	Additional Analog Complexity	Relative Analog Bandwidth
This work	2592T (1X)	9 (1X)	Two 8-bit gain calibration DACs	1X
Butterfly [23]	9472T (3.6X)	18 (2X)	Two additional switches in each DAC unit cell[a]	~0.5X[b]
Tree-structured [23]	6992T (2.7X)	20 (2.2X)	Two additional switches in each DAC unit cell[a]	~0.5X[b]

[a] For a capacitive DAC, individual capacitors can no longer abut because the top plate is not a common node. To reduce cross element parasitic capacitance, they are spaced apart in the layout. For a current mode DAC, headroom is an issue because of the additional series switches.

[b] Due to another series switch in the main charging path, plus additional poles.

a closed-form expression from a given ERA. The approach is applied here to the quadrature ERA of Kurosawa, et al. [36] to derive its *MTF*, which shows its sub-optimal nature compared to the quadrature ERA proposed herein.

By retracing the two-step process in reverse, one set of difference equations for every alternate step can be written for the quadrature ERA of [36]:

$$\begin{aligned} s_4(n) &= s_3(n) + t_3(n-1) \\ t_4(n) &= t_3(n) - s_3(n-1) \end{aligned} \tag{10}$$

$$\begin{aligned} s_4(n) &= s_3(n) - t_3(n-1) + 1 \\ t_4(n) &= t_3(n) + s_3(n-1) - 1 \end{aligned} \tag{11}$$

Eqn. (10) represents $MTF = 1 - jz^{-1}$ (like (4)) whereas (11) approximates $MTF = 1 + jz^{-1}$. Since the ERA uses the *MTFs* on alternate cycles, it apparently realizes a real band-pass *MTF* (i.e., product of the two) albeit sub-optimally as shown by the results in Fig. 8; *SNDR* for an ADC with $NTF = (1 - jz^{-1})^3$ is about equal to that with $NTF = (1 + jz^{-1})^3$. However, the proposed ERA truly implements $MTF = 1 - jz^{-1}$ (i.e., with a zero at $+f_s/4$) to achieve an increase of almost 25 dB in *SNDR*. However, it does not perform well, as shown, when used with $NTF = (1 + jz^{-1})^3$ (i.e., with a zero at $-f_s/4$).

IX. Conclusions And Future Work

This paper describes mathematical procedures for deriving DAC element rotation algorithms from given general mismatch transfer functions for quadrature Σ-Δ data converters in frequency channelized receivers. An optimal quadrature ERA is derived and applied in multi-channel frequency-channelized data converters for wide-bandwidth applications such as LTE-Advanced. Gain mismatches between *I* and *Q* DACs are mitigated by combining analog mismatch shaping and digital LMS gain calibration algorithms with minimal hardware overhead. The proposed system shows significant *SNDR* improvements over earlier approaches for both intra- and inter-DAC element mismatches. Future work will investigate reducing the image artifacts, executing the calibration loops with separate localized coefficients for each channel, the impact of convergence of the LMS calibration loops on the overall

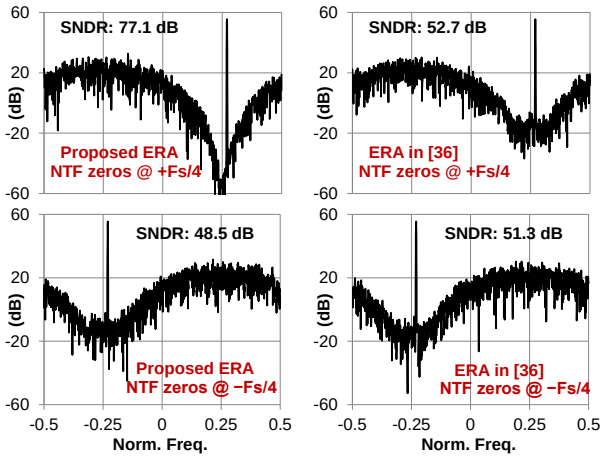


Fig. 8. The proposed quadrature ERA implements a zero at +fs/4 in the MTF; as opposed to [36], SNDR improves considerably when the NTF and MTF zeros are accurately aligned. (Simulations for 8 bit Gaussian mismatches, 3rd-order Σ-Δ ADC, OSR = 16, 4 physical bits).

SNDR using the proposed approach and implementation in silicon. A detailed comparison of the hardware and performance trade-offs compared to conventional approaches confirms the reduced area and latency advantages that are attractive for wide-bandwidth low-latency closed-loop architectures.

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