TDDB Chip Reliability in Copper Interconnects

Muhammad Bashir, Dae Hyun Kim, Sung Kyu Lim and Linda Milor
School of Electrical and Computer Engineering, Georgia Institute of Technology
Atlanta, GA, 30332
404-840-3147; e-mail: mbashir@gatech.edu

ABSTRACT

Backend time dependent dielectric breakdown (TDDB) degrades the reliability of circuits with copper interconnects. We use test data to develop a methodology to evaluate chip lifetimes, because of backend TDDB, from layout statistics. We identify features in a layout that are critical to backend reliability, present a model to incorporate those features in determining chip lifetimes, and study the effect of different layout optimizations on chip lifetime.

INTRODUCTION AND MOTIVATION

The performance advantage offered by Copper/low-k interconnects is accompanied by issues critical to reliable circuit and system operation. Copper (Cu) interconnects are especially vulnerable to failure due to time-dependent dielectric breakdown (TDDB) of low-k dielectrics. TDDB lifetime for different low-k dielectrics and conductor geometries is determined by using appropriate test structures. Lifetimes at use conditions are determined by scaling. To determine the lifetime of a chip, a correction is also needed to account for the difference between the vulnerable area of the product and the test structure. However, there is no literature on the method to find the vulnerable area for a chip for backend dielectric breakdown, except for the statement that the vulnerable area is "the total length of such [minimum spaced] lines within a product" [1].

The purpose of this paper is to clearly specify the vulnerable area of a chip for backend TDDB and to develop the link between data collected from test structures and chip lifetime due to backend dielectric breakdown. Our methodology accounts for more than minimum spaced lines and includes all layers of a chip, which can have different vulnerable areas.

This paper starts with a brief background on models for low-k dielectric breakdown and an overview of our approach in Section 2. In Section 3, we give an overview of our test structures and test results. In Section 4, we present our methodology. In Section 5, we present the results of applying our methodology to example circuits. In Section 6, as a stepping stone for a tool to optimize layouts for reliability, we present our observations regarding the effect of layout on reliability. Section 7 concludes the paper.

BACKGROUND AND OUR APPROACH

The time-to-failure (TF) of backend dielectrics is related to material characteristics and operating conditions. Relationships between the breakdown electric field (E) and TF have been the focus of most of the work done in backend TDDB. The E model [2], [3] and the $\sqrt{E}$ model [4], [5] describe the relationship between E and TF. The temperature dependence of TF is modeled with an Arrhenius relationship.

We focus on backend TDDB. However, we develop our methodology in a way that other reliability limiting mechanisms can be integrated with our methodology. We use test structure data to identify sensitivities of backend low-k TDDB to identifiable geometric features. We then use these geometric features to extract the vulnerable area of chips and to characterize failure rates. This work is not explicitly concerned with methods to account for details of the fabrication methods. Instead, we assume that the conductors in the chip are fabricated with the conductors in the test structure, a reasonable assumption given the simplicity of test structures.

TEST STRUCTURE DESIGN AND RESULTS

We categorize test structure as "area" and "linewidth" test structures to quantify the impact of dielectric area and Cu linewidth on backend TDDB. The area test structures are formed using test structures with areas that are multiples of a minimum area test structure [6]. Similarly, linewidth test structure are formed using test structures with linewidths that are multiple of a minimum linewidth test structure [7]. Fig. 1(a) shows our test structures.

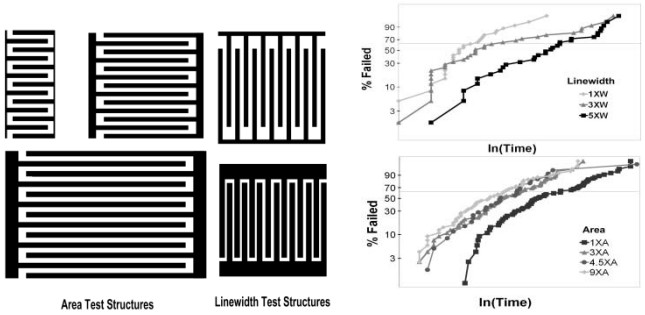

Fig. 1: Test structures to study the effect of dielectric area and Cu linewidth on low-k TDDB: (a) top view of the test structures and (b) data.

These test structures have been manufactured with an industrial 45nm CMOS process. We conducted constant voltage accelerated lifetime tests at $150^{\circ}C$. Breakdown was considered as the point of onset of a leakage current greater than greater than $100\mu A$. The sample size was 30. Fig. 1(b) shows the test results. Test results indicated a strong impact of area. Failure rate curves showed die-to-die linewidth variation that resulted in curvature in distributions [6]. Test results also showed a strong impact of linewidth on backend TDDB. Reasons for this particular behavior were investigated and modeled in [7]. In summary, time-to-failure (TF) decreased with increasing area and increased with increasing linewidth [6],[7]. Fig. 1(b) shows our test results. Fig. 2 shows the effect of dielectric area and linespace simultaneously on the Weibull characteristic lifetime η.

978-1-4244-8524-6/10/$26.00 ©2010 IEEE

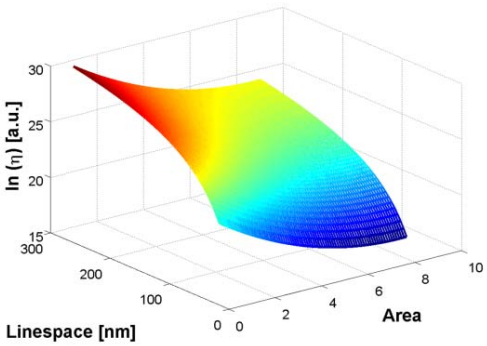

Fig. 2: The effect of dielectric area and linespace on Weibull characteristic lifetime (η). The model is based on data taken from test structures, where linespace is determined by linewidth, since the pitch is constant.

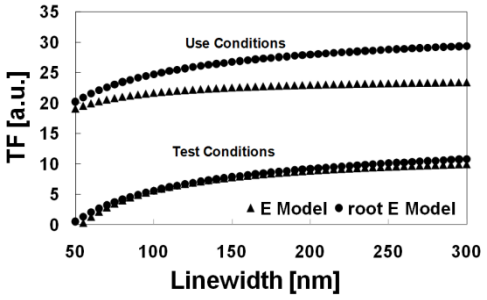

Fig. 3: Test results scaled to use conditions.

Electric field and temperature affect the scaling from test conditions to use conditions. In the case of backend TDDB, the choice of model also has a bearing on scaling to use conditions. Adjustments are made to find TF under AC stress [8], or pulsed DC, by incorporating a signal activity factor. Fig. 3 shows results from our test structures scaled to typical use conditions for 45nm technology.

LIFETIME FROM CHIP LAYOUT

Vulnerable Sites

Based on the information that can be extracted from a layout (GDSII), we determine the sites that are vulnerable to low-k TDDB, thus the vulnerable area. A vulnerable area is a two dimensional block of dielectric, with a horizontal (linespace) and a vertical dimension (length). The feature that is extracted from layout is the vulnerable length (L) between two lines associated with a linespace (S), which is a function of the two adjacent linewidths (W_L , W_R) [7]. If the different areas in the layout have different average on-chip temperatures, then the layout can be partitioned into sectors according to the temperature. Our studies show little or no impact of vias [6].

Methodology

TF for a Single Layer

We extract pairs ($S_i(W_L,W_R),L_i$) for each layer, i.e. the vulnerable length associated with each linespace in a layout. We assume a Poisson model for the defect distribution over an area and the Weibull failure distribution

$$P = 1-\exp(-\lambda(t)A) = 1-\exp\left(-\left(\frac{TF}{\eta}\right)^{\beta}\right), \qquad (1)$$

where $\lambda(t)$ is the defect density at failure and A is the vulnerable area. η is the Weibull characteristic lifetime and β is the Weibull slope. The characteristic lifetime of all features in the chip layout in a layer corresponding to linespace S_f is [9]

$$\eta_f = \eta_{test}\left(\frac{L_{test}}{L_f}\right)^{\beta}, \qquad (2)$$

where S_{test} is the linespace of the test structure that has a length L_{test} and η_{test} is the experimentally determined characteristic lifetime associated with it. For a layout with a variety of linespaces , S_f , it is necessary to combine the failure rates of all of these linespaces. We compute a defect count $d_f = (TF/\eta)^{\beta}$ for each linespace in the layer. The total defect count is the sum of defect counts of all linespaces present in a layer. We use this cumulative defect count to find the characteristic lifetime of the layer (η_{layer}) as [9]

$$\eta_{layer} = \left(\sum_f \frac{1}{\eta_f^{\beta}}\right)^{-1/\beta}. \qquad (3)$$

TF for a Chip

Let d_l be the defect density for each layer, where $d_l = \sum_f d_f$. Then, the defect density for the chip will be $d_{chip} = \sum_l d_l$. However, unlike for a single layer, multiple layers of a chip may have different process details. Therefore, data would need to be collected from test structures for each layer separately, i.e., L_{test} , η_{test} , and $\beta(l)$ are unique to each layer. If β were common to all layers, then it is possible to solve for the characteristic lifetime of the chip, η_{chip} , [9]

$$\eta_{chip} = \left(\sum_l \sum_f \frac{1}{\eta_f^{\beta}}\right)^{-1/\beta}. \qquad (4)$$

Otherwise η_{chip} is implicitly defined [9]:

$$1 = \sum_l \sum_f \left(\frac{\eta_{chip}}{\eta_f}\right)^{\beta(l)}. \qquad (5)$$

Summary

We extract pairs $(S_i(W_L,W_R),L_i)$ for each layer to show the vulnerable length associated with each line space in a layout and find the associated characteristic lifetime, using (2), by comparing the length of those linespaces with the length of the linespace in the test structure. We then solve (5) to find the characteristic lifetime for the chip.

LOW-K TDDB CHIP RELIABILITY

Assumptions

Since this study is about lifetimes, we assume the presence of an electric field in the dielectric between two neighboring lines throughout the duration of the operation of the chip. We have only collected data from one layer, so we assume that chemical-mechanical-polishing (CMP), etching and photolithography impact all the layers in the same way.

Circuits

We have used the NCSU 45nm technology library [10]. The process has ten metal layers. The minimum linespace is equal to the minimum linewidth for all the metal layers. The minimum linespace and minimum linewidth is 65 nm for Metal 1, 70 nm for Metal 2 and Metal 3, 140 nm for Metal 4 through Metal 6, 400 nm for Metal 7 and Metal 8, and 800 nm for Metal 9 and Metal 10.

We synthesized radix-2 pipelined, 256 and 512 points, 8 precision, fast fourier transform (FFT) HDL source code [11]. The 256 point circuit has 324k gates and 329k nets. The 512 point circuit has 708k gates and 712k nets. Synopsys Design Compiler was used for synthesis [12], and Cadence SOC Encounter was used for placement, clock tree synthesis, routing, optimization and RC extraction [13]. Synopsys PrimeTime was used for timing analysis [14].

We used seven different instantiations of the 256 point circuit and four different instantiations of the 512 point circuit. Our performance metrics were the number of layers in a circuit and its timing performance. Table 1 gives the details of the circuits. Table 1 shows the timing performance, the total wirelength, and the percentage of total wirelength in each layer (wire density). Names of the instantiations of the 256 point circuits start with f1 and that of 512 point start with f2. Circuits with M in their name are used to study the impact of the number of layers on lifetime. Circuits with RT in their names are used to analyze the impact of timing performance on lifetime.

Results

Fig. 4(a) shows characteristic lifetime for Metal1-Metal6 for the circuits used in the study and for the chip according to the $\sqrt{E}$ Model. η for chips are more pessimistic than η for the individual layers. There is no observable trend relating reliability and timing performance in Fig. 4, although it shows that decreasing wirelength increases reliability. Fig. 4(b) also shows characteristic lifetime for the circuits being studied according to both the E Model and the $\sqrt{E}$ Model.

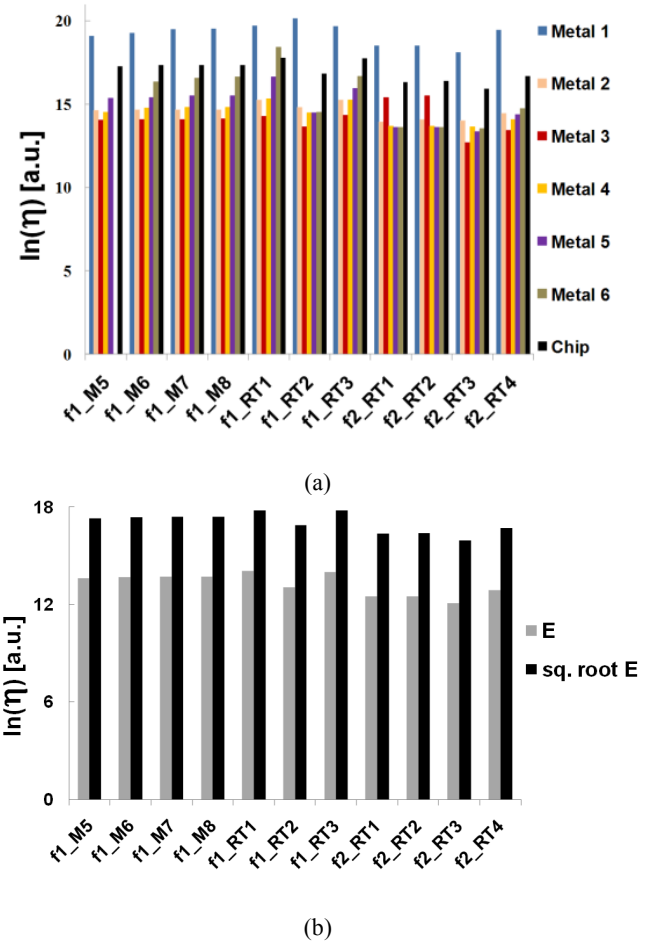

Fig. 4: (a) Characteristic lifetime for each layer and the chip using the $\sqrt{E}$ model. (b) Characteristic lifetime for circuits according to the E Model and the $\sqrt{E}$ Model.

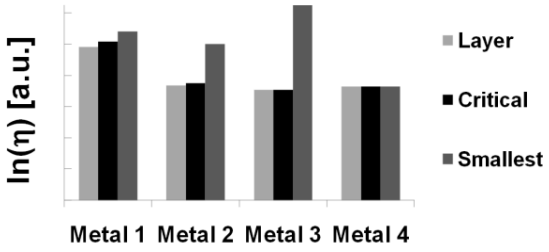

Fig. 5: Characteristic lifetimes, η, for Metal1-Metal4 of f1_M5, for the critical linespace group in each layer and the smallest linespace in each layer. The critical linespace group is the most frequent linespace in the layer.

IMPACT OF LAYOUT ON TDDB RELIABILITY

Using more metal layers generally results in a decrease in congestion. This leads to less coupling capacitances between the wires. Critical path delays are proportional to coupling capacitances. However, the wires can be spread out in a number of layers to improve coupling capacitances and consequently reliability. Table 1 shows that critical path delay (CPD) decreases when the number of layers is increased. But this is accompanied by a marginal improvement in reliability. It must be noted that the layer most critical to reliability statistics, Metal 3, remains the same, i.e. the layer with the highest wire-density. Moreover, even when the number of layers is increased, the additional layers route less than 8% of the total wirelength.

If we were to determine the characteristic lifetime based on the minimum linespace alone, we only need to determine the minimum linespace in each layer, the area formed by that linespace and the associated characteristic lifetime. In fact, if such an approach is followed, then we only need to determine the minimum linespace in the complete chip. Such an approach is inaccurate, as illustrated in Fig. 5. In fact, the critical linespace was larger than the smallest linespace for all the layers of all the circuits studied.

TABLE 1: PERCENTAGE OF WIRING IN EACH LAYER (LABELED METAL 1 – METAL 8), TOTAL WIRELENGTH (WL) AND CRITICAL PATH DELAY (CPD)

Layer	Design										
	f1_M5	f1_M6	f1_M7	f1_M8	f1_RT1	f1_RT2	f1_RT3	f2_RT1	f2_RT2	f2_RT3	f2_RT4
Metal1	1.4	1.4	1.4	1.4	2.6	0.8	2.2	0.6	0.6	0.6	1.2
Metal2	18.8	18	18.1	18.1	22.6	14.1	19.5	12.5	12.5	13.1	15.8
Metal3	33.9	33.1	33.1	33.1	38.4	25.8	32	23.2	23.2	26.2	27.9
Metal4	29.5	25.7	25.7	25.6	24.9	18.9	23.1	17.4	17.4	18.4	22.7
Metal5	16.2	16.1	15.4	15.3	9.52	19.9	15.5	19.5	19.4	23.1	19.8
Metal6		5.4	5.07	5.03	1.86	15.9	7	17.2	17.2	18.4	12.53
Metal7			0.9	1	0.05	4.6	0.7	5.14	5.14		
Metal8				0.1		0.01		4.38	4.38		
Total WL [m]	8.06	8.05	7.99	7.99	6.28	13.56	7.52	34.71	34.71	33.79	21.09
CPD [ns]	3.51	3.51	3.33	3.29	3.16	2.9	2.86	3.86	3.86	3.1	2.98

Figure 4(a) and Table 1 show that there is a strong correlation between wire density and lifetime. Such a correlation is expected because higher wire density results in higher field density and field intensity, and leads to poor reliability. Also, as expected, reliability increases with a decrease in wirelength.

We have previously shown that linewidth affects lifetime because of its interaction with the manufacturing process [7]. However, we found that wider lines, which improved the lifetime of test structures, increased the congestion in circuits and reduced reliability [9].

Timing optimization can be achieved in a number of ways: buffer insertion, gate re-placement, and gate sizing. Timing optimization can lead to densely routed areas. But, densely routed areas increase coupling capacitances and degrade reliability. These issues are addressed by re-routing or resizing nets. Timing optimization is also achieved through buffer insertion, although this strategy results in an increase in total wirelength.

Finally, we did not observe any correlation between timing and reliability. A possible reason for this could be the use of heuristic algorithms for timing optimization, instead of deterministic algorithms. However, there was an observable correlation between the coverage in a given layer by the critical linespace group and characteristic lifetime. For instance, for circuits f1_RT1, f1_RT2, and f1_RT3, 99% of the lines have two different linespaces between them, 120 nm and 310 nm. The lifetime was primarily determined by the 120 nm linespace group.

CONCLUSIONS

A methodology was proposed to evaluate low-k TDDB lifetime of chips. Test data was collected and relevant layout features were identified. The methodology links the test structures and chips via analysis of vulnerable area. Several case studies were presented to determine the effect of different layout optimization metrics on lifetime. We considered the impact of the number of layers, the minimum linespace, wire density, wirelength, and timing optimization was observed.

ACKNOWLEDGMENT

The authors would like to thank the National Science Foundation for their financial support under Award 0901576.

REFERENCES

[1] T. Pompl, *et al.*, "Practical aspects of reliability analysis for IC designs," in *Proc. Design Automation Conf.*, 2006, pp. 193-198.
[2] G. S. Haase and J. W. McPherson, "Modeling of interconnect dielectric lifetime under stress conditions and new extrapolation methodologies for time-dependent dielectric breakdown," in *Proc. Int. Reliability Physics Symp.*, 2007, pp. 390-398.
[3] J. Kim, *et al.*, "Time dependent dielectric breakdown characteristics of low-k dielectric {(SiOC)} over a wide range of test areas and electric fields," in *Proc. Int. Reliability Physics Symp.*, 2007, pp. 399-404.
[4] F. Chen, *et al.*, "A comprehensive study of low-k SiCOH TDDB phenomena and its reliability lifetime model development," in *Proc. Int. Reliability Physics Symp.,* 2006, pp. 46-53.
[5] F. Chen, *et al.*, "Cu/low-k dielectric TDDB reliability issues for advanced CMOS technologies," *Microelectronics Reliability,* vol. 48, pp. 1375-1383, 2008.
[6] M. Bashir and L. Milor, "A methodology to extract failure rates for low-k dielectric breakdown with multiple geometries and in the presence of die-to-die linewidth variation," *Microelectronics Reliability,* vol. 49, pp. 1096-102, 2009.
[7] M. Bashir and L. Milor, "Analysis of the Impact of linewidth variation on low-k dielectric breakdown," in *Proc. Int. Reliability Physiscs Symp.*, 2010, pp. 895-902.
[8] J. Sung-Yup, *et al.*, "The characteristics of Cu-drift induced dielectric breakdown under alternating polarity bias temperature stress," in *Proc. Int. Reliability Physics Symp.*, 2009, pp. 825-827.
[9] M. Bashir, *et al.,* "Methodology to determinethe impact of linewidth variation on chip scale copper/low-k backend dielectric breakdown," *Microelectronics Reliability,* vol. 50, pp. 1341-1346, 2010.
[10] N. EDA. *NCSU FreePDK45*. Available: http://www.eda.ncsu.edu/wiki/FreePDK
[11] *Launchbird Design Systems, Inc., CF FFT*.
[12] I. Synopsys. *Design Compiler*. Available: http://www.synopsys.com
[13] I. Cadence Design Systems. *Soc Encounter RTL-to-GDSII System 8.1*. Available: http://www.cadence.com
[14] I. Synopsys. *PrimeTime*. Available: http://www.synopsys.com