Analysis of TSV-to-TSV Coupling with High-Impedance Termination in 3D ICs

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Abstract—It is widely-known that coupling exists between adjacent through-silicon vias (TSVs) in 3D ICs. Since this TSV-to-TSV coupling is not negligible, it is highly likely that TSV-to-TSV coupling affects crosstalk significantly. Although a few works have already analyzed coupling in 3D ICs, they used S-parameter-based methods under the assumption that all ports in their simulation structures are under 50-Ω termination condition. However, this 50-Ω termination condition does not occur at ports (pins) of gates inside a 3D IC. In this paper, therefore, we analyze TSV-to-TSV coupling in 3D ICs based on a lumped circuit model with a realistic high-impedance termination condition. We also analyze how channel affect TSV-to-TSV coupling differently in different frequency ranges. Based on our results, we propose a technique to reduce TSV-to-TSV coupling in 3D ICs.

Index Terms—Coupling; Crosstalk; Through-Silicon Via (TSV); 3D IC; High impedance termination; Capacitive termination;

I. INTRODUCTION

Today's integrated circuits (ICs) need very wide bandwidth to meet ever-increasing computational requirements, small form factor to reduce cost, and high-speed chip-to-chip communication to boost performance [1]. Three-dimensional (3D) ICs are emerging as a promising technology to meet all these needs. In 3D ICs, dies are stacked vertically, and gates in different dies are connected by through-silicon vias (TSVs). TSVs are much smaller than off-chip wires, thereby enabling very wide bandwidth and high-speed communication between stacked dies. However, there exist several problems such as heat, TSV defects, and power delivery in 3D ICs [2], [3]. These problems need to be resolved to build reliable 3D ICs.

Crosstalk in 3D ICs is becoming one of the biggest reliability issues in 3D ICs. In 2D ICs, two adjacent metal wires form a parallel capacitor, and this capacitive coupling is the source of the crosstalk between the two wires. In 3D ICs, however, two adjacent TSVs have a coupling network between them due to the silicon substrate and silicon dioxide insulator. This TSV-to-TSV coupling could be very problematic in 3D ICs because TSVs are big and tall so that the coupling between two adjacent TSVs can be huge. These TSVs are connected
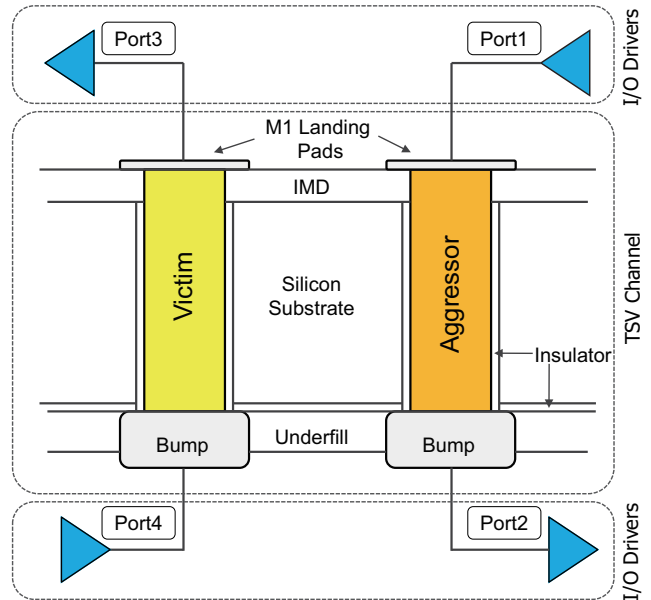
Fig. 1. A simplified model of TSVs and I/Os in 3D IC.

to metal wires, so the total coupling of two signal paths can cause serious crosstalk problems in 3D ICs.

Authors of [4], [5], [6] showed S-parameter-based coupling analysis assuming that all ports are under 50-Ω termination condition. However, it is not possible nor practical to create 50-Ω termination condition inside a digital IC. In this paper, therefore, we apply a lumped circuit model with a realistic high-impedance termination condition to analyze TSV-to-TSV coupling in 3D ICs. Then, we compare the S-parameter-based coupling analysis with the lumped-circuit-model-based coupling analysis. The result shows that our circuit-model-based analysis is highly accurate and that the difference between different termination conditions is huge. It also shows that the channel affect differently to TSV coupling in different frequency ranges. Finally, we propose a technique to reduce coupling in 3D ICs based on the analysis result.
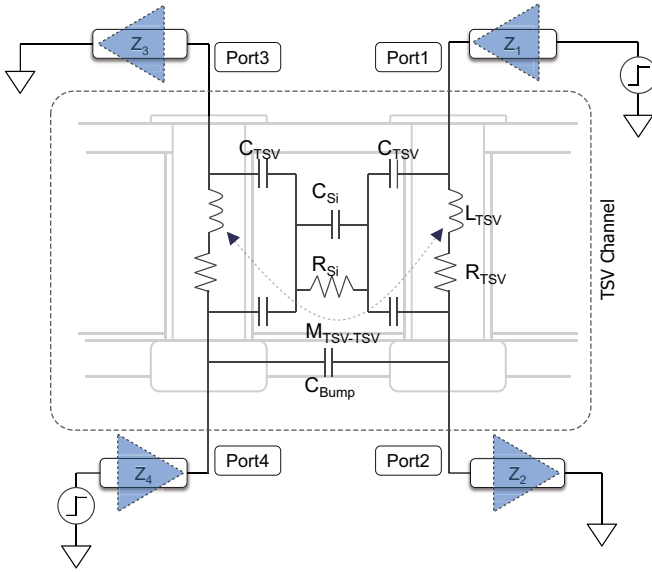
Fig. 2.   Equivalent lumped circuit model for the TSV channel.

II. Electrical Model of TSVs

TSV-to-TSV crosstalk analysis needs electrical models for a physical structure that consists of TSVs, insulator, silicon substrate, bumps, and I/O drivers. In this section, therefore, we show the physical structure and its electrical model, and validate it using a commercial simulator.

Figure 1 shows a simplified model for a TSV channel, and Figure 2 shows its equivalent lumped circuit model. The TSV at the right side is the aggressor, which is driven by Port1. The TSV to the left is the victim. The lumped circuit modeling can be used because the elements we are modeling are smaller than 100um, which are all shorter than the $1/20\lambda$ wavelength of 20GHz. The electrical parameters and process technology nodes used in this model are presented in Table I. Since TSVs are made of conducting material such as copper or tungsten, a TSV is modeled as a series connection of a resistor (R_{TSV}) and an inductor (L_{TSV}). Silicon dioxide insulator between TSV and silicon substrate is modeled as a capacitor (C_{TSV}). On the other hand, silicon substrate can be modeled as a capacitor (C_{si}) in parallel with a resistor (R_{si}) as shown in Figure 2. There exists mutual inductance between two TSVs, which also has to be modeled ($M_{\mathrm{TSV-TSV}}$). In order to compute the capacitances and the resistances, we use the following equations presented in [5]:

$$C_{\mathrm{TSV}} = \frac{1}{4} \frac{2\pi\epsilon_0\epsilon_{\mathrm{r}}}{\ln\left(\frac{r_{\mathrm{TSV}}+t_{\mathrm{ox}}}{r_{\mathrm{TSV}}}\right)} \cdot l_{\mathrm{TSV}} \tag{1}$$

$$C_{\mathrm{si}} = \epsilon_0\epsilon_{\mathrm{si}} \frac{2(r_{\mathrm{TSV}}+t_{\mathrm{ox}})+\alpha}{d} \cdot l_{\mathrm{TSV}} \tag{2}$$

$$R_{\mathrm{si}} = \rho_{\mathrm{si}} \cdot \frac{d}{2(r_{\mathrm{TSV}}+t_{\mathrm{ox}})+\alpha} \cdot \frac{1}{l_{\mathrm{TSV}}} \tag{3}$$

$$C_{\mathrm{Bump}} = \frac{\epsilon_0\epsilon_{\mathrm{r}}}{d-2r_{\mathrm{Bump}}} \cdot \pi \cdot r_{\mathrm{Bump}} \cdot l_{\mathrm{Bump}} \tag{4}$$

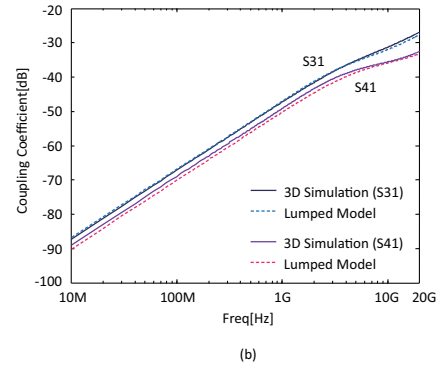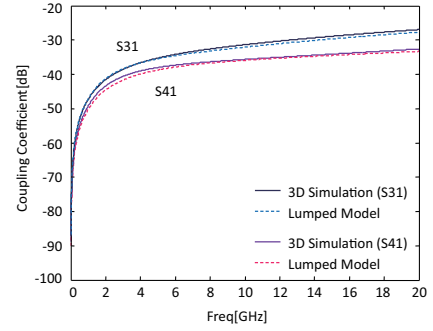| Parameter	Value
TSV diameter	$2.5\mu m$
TSV height	$75\mu m$
Insulator thickness	$0.5\mu m$
Bump pad diameter	$5.0\mu m$
Bump height	$10\mu m$
Dielectric constant of liner	4
Dielectric constant of underfill	4
Process technology	Nangate $45nm$
Supply voltage	$1.2V$

Fig. 3.   Coupling coefficients obtained from a 3D simulator model and our lumped circuit model when the TSV-to-TSV distance is $10\mu m$. (a) Linear scale, (b) Log Scale

where r_{TSV} is the TSV radius, l_{TSV} is the TSV height, t_{ox} is the thickness of the insulator, d is the pitch between two TSVs, r_{Bump} is the radius of a bump, and l_{Bump} is the height of a bump.

Regarding equation(2) and (3), many papers [5], [7] have mentioned this as the electromagnetic formula of capacitance between two parallel pillars. This may be effective in cases where no other TSVs are interfering inside the fields that are generated between the two pillars. However, in such cases this assumption may not be valid. Therefore we propose a formula regarding the silicon substrate as a parallel plate capacitor that considers the effective volume of the silicon substrate between two TSVs. In equations (2), and (3), we use scaling factors (α) which has the value of $24\mu m$.

Figure 3 shows the coupling coefficients (s_{31}) obtained from a commercial 3D electromagnetic simulator (Ansoft HFSS) and our lumped circuit model when the distance between two
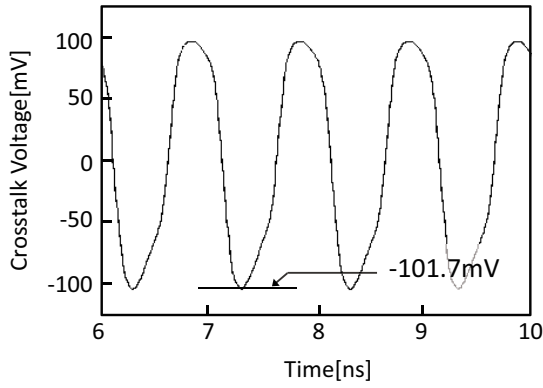
Fig. 4. Crosstalk voltage observed at port3 when 1.2V, 1GHz digital signal inserted to port1. (1× driver, TSV-to-TSV distance: $10\mu m$.)

TSVs is $10\mu m$. Note that the 3D simulator can only support termination condition of 50-Ω. As the figure shows, our TSV model is very accurate and the maximum difference is less than 1dB.

In the basis of our TSV model, We use 1× inverter (w_p=260nm, w_n=130nm) for each I/O driver. A driver is modeled as a resistance (output resistance) connected to the supply voltage, and a load as a capacitance (input capacitance) connected to the ground. Here, we show the voltage noise level observed at Port3 when 1GHz digital signal is inserted at port 1 in Figure 4. Despite the small driver size on port 1, the peak noise is $-101.7mV$, which is not negligible.

III. ANALYSIS OF TSV-TO-TSV CROSSTALK

A. Crosstalk Equations Under High-Impedance Termination

In the frequency range under 20GHz, silicon substrate, bumps and the insulator (silicon dioxide) around TSVs form a channel having very high impedance. On the other hand, the impedance composed of TSV resistance and inductance is very low. If we ignore the low impedance components, the lumped circuit model in Figure 2 can be simplified as a model having only high-impedance components as shown in Figure 5. Applying Kirchhoff's laws to the model in Figure 5(b), we obtain the following matrix for V_1 and V_2:

$$\begin{bmatrix} \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_5} & -\frac{1}{Z_5} \\ -1 & 1 + \frac{Z_5}{Z_3} + \frac{Z_5}{Z_4} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{V_{\text{in}}}{Z_1} \\ 0 \end{bmatrix} \quad (5)$$

where Z_5 is the impedance of the TSV channel in the simplified model. Solving for V_2, we finally obtain the following equation:

$$V_2 = V_{\text{in}} \cdot \frac{Z_2 Z_3 Z_4}{Z_1 \cdot Z_A + Z_2 Z_3 Z_4 + Z_5 \cdot Z_B} \quad (6)$$

where

$$Z_A = Z_2 Z_3 + Z_2 Z_4 + Z_3 Z_4 + Z_3 Z_5 \quad (7)$$
$$Z_B = Z_1 Z_4 + Z_2 Z_3 + Z_2 Z_4 \quad (8)$$
$$Z_5 = \frac{Z_{C_{\text{Bump}}}(Z_{C_{si}}//Z_{R_{si}} + 2Z_{C_{\text{TSV}}})}{Z_{C_{si}}//Z_{R_{si}} + Z_{C_{\text{Bump}}} + 2Z_{C_{\text{TSV}}}} \quad (9)$$
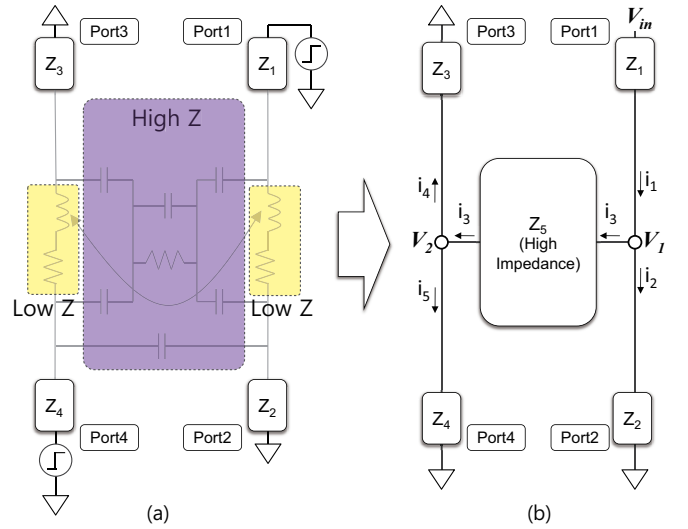

Fig. 5. (a) Impedance level of each component in the lumped circuit model, (b) Simplified model for coupling analysis.

Equation (6) shows that the coupling between two TSVs depends not only on the channel impedance (Z_5) between the TSVs, but also on the termination condition (Z_2, Z_3, Z_4) and the driver condition (Z_1).

B. Comparison of Termination Conditions

As mentioned in Section I, S-parameter-based coupling analysis assumes a 50-Ω termination condition which is very unlikely inside a digital IC. Therefore we change termination conditions, compute coupling, and compare their results in this section.

Figure 6 compares two different termination conditions. When all ports are terminated with 50-Ω resistance (solid line), the coupling coefficient is below -30dB even in the highest frequency region (under 20GHz). However, when all ports are terminated in high impedance (1× driver at all ports), the coupling coefficient reaches almost up to -10dB. The coupling coefficient in this case is so high that it causes serious crosstalk in over GHz high frequency range. This cannot be observed if we assume 50-Ω termination, and this is the special channel-termination condition which we face in 3D ICs.

C. Macro Impact of Port Impedance on TSV-to-TSV coupling

In this section, we explain the macro impact of port impedance on TSV-to-TSV coupling using Equation (6). Regarding equation (6), it is Z_2, Z_3, and Z_4, which are the dominating variables inside the total equation. Assume a typical signal coupling channel where the ports are driven by a typical size driver (Z_1). In this case the port impedances at Z_2, Z_3, Z_4 are in the same scale. Replacing Z_2, Z_3, and Z_4 with the same term Z_{port} ($Z_2 = Z_3 = Z_4 = Z_{port}$), we can rewrite equation (6) as:

$$V_2 = V_{\text{in}} \cdot \frac{Z_{\text{port}}^3}{Z_{\text{port}}^3 + Z_{\text{port}}^2(3Z_1 + 2Z_5) + 2Z_{\text{port}} Z_1 Z_5} \quad (10)$$
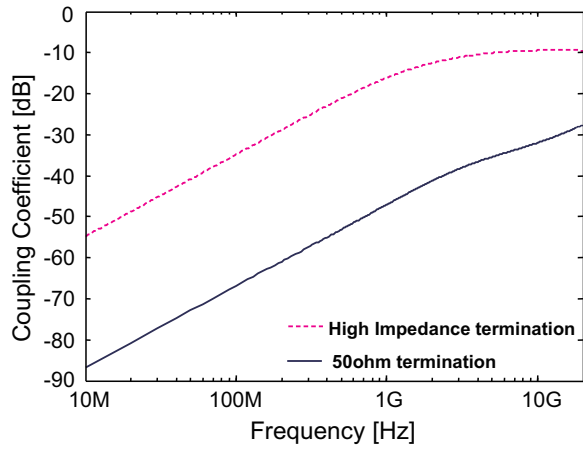
Fig. 6. Coupling coefficients of the 50Ω termination condition (solid line) and the high impedance termination ($1\times$ driver, dotted line) condition.

Equation (10) shows that if the port impedance is much higher than the channel impedance, the coupling level can be very large, even close to the agrressor voltage.

However, there are factors limiting the coupling voltage to a certain range. In the previous analysis, we didn't consider the TSV capacitance at the other side (not on the coupling side) which connects to ground through substrate. This capacitance is large, and in parallel with the port impedance. A TSV not only sees the port impedance but also sees the GND capacitance. With this capacitance the coupling voltage is limited to a certain level. Thus, even when a port impedance is too high, the GND capacitance acts like a buffer and screens out the high port impedance (see Figure 7).

In 3D ICs, we are dealing with a situation where the ports impedance (less than a few fF capacitance) is much higher than the coupling channel impedance (tens of fF capacitance series to fF capacitance and kΩ resistance). However, due to the high capacitance we see between the TSVs and the GND, this capacitance limits the coupling voltage to be at a certain level.

D. Micro Impact of Port Impedance on TSV-to-TSV coupling

In this section, we explain the micro impact of port impedance on TSV-to-TSV coupling when all port impedance numbers are not the same, but are fixed in a specific range, using Equation (6) and Figure 8. Here, we discuss the individual role of each ports to channel coupling. First, when the driver (Port1) is big (low output resistance = low Z_1), it becomes a strong aggressor, and increases crosstalk. This is also observed quantitatively in Equation (6) because Z_1 exists only in the denominator. On the other hand, if the sink (Port2) is big (high input capacitance = low Z_2), the impedance at Port2 becomes low and the impact of the aggressor decreases. Similarly, if the sink (Port3 or Port4) in the victim net is big (high load capacitance = low Z_3, high load capacitance and low output resistance = low Z_4), it reduces the crosstalk.
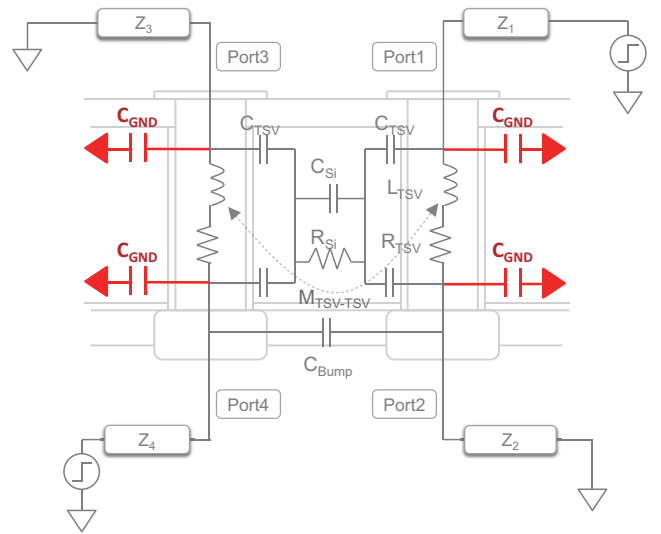

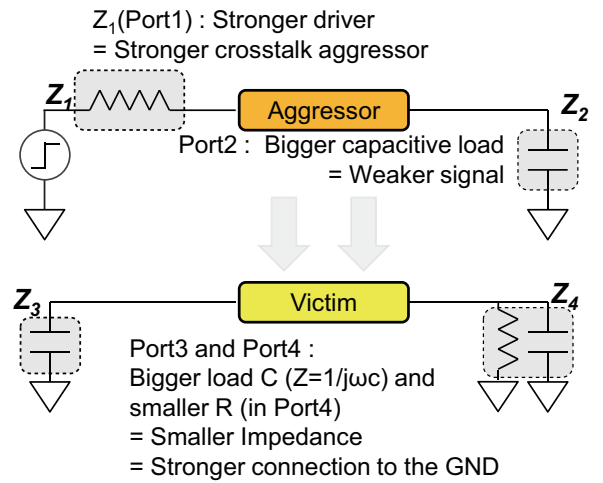Fig. 7. Impact of GND capacitance in TSV coupling channel.

Fig. 8. Visualization of a driver strength, load impedance, and the relationship between the aggressor and the victim.

In fact, Equation (6) can be rewritten as:

$$V_2 = V_{\text{in}} \cdot \frac{ax}{(a+b)x + c} = \frac{a}{a+b} \cdot \left(1 - \frac{c}{(a+b)x + c}\right) \quad (11)$$

where x is a variable which can be one of Z_2, Z_3, or Z_4 (say, $x=Z_2$), and a, b and c are constants when the frequency is fixed and Z_n ($\neq x$) is a constant (say, Z_3 and Z_4 are fixed). We can observe from this equation transformation that V_2 increases monotonically as x increases. Therefore, high load capacitance (low load impedance) reduces the impact of the aggressor. A stronger driver at victim net and a weaker driver at aggressor net also reduce the coupling level.

E. Dependency of Channel Impedance on Low Frequency

Unlike wire coupling channels, TSV coupling has a very unique coupling channel characteristic. Due to the various types of components in the coupling channel, the impedance
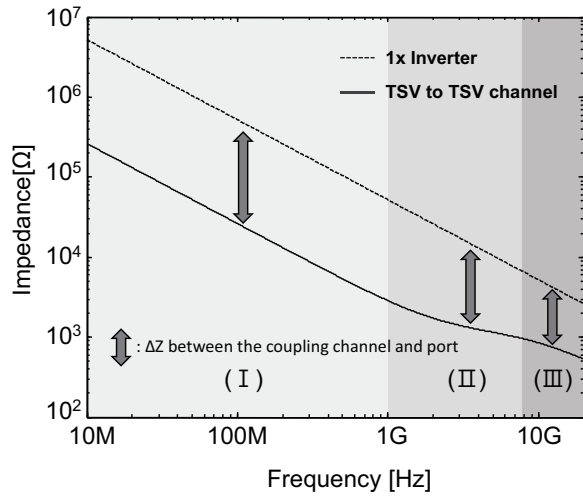
Fig. 9. Impedance difference between the silicon substrate channel, and the gate capacitance in different regions: (I) low frequency (< 1GHz), (II) middle frequency (1GHz to 8GHz), (III) high frequency (> 8GHz).
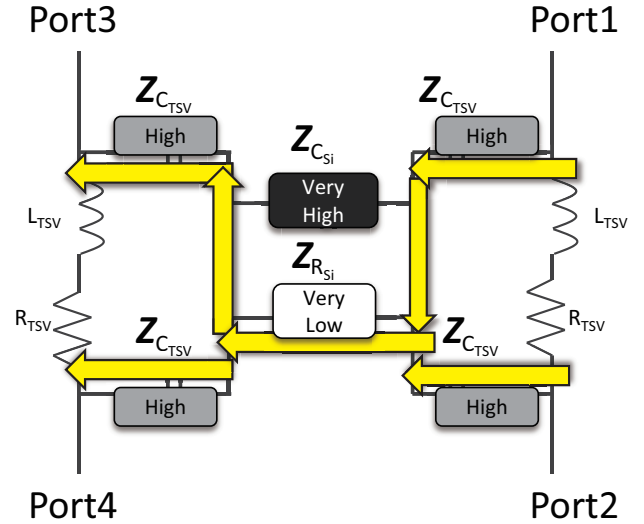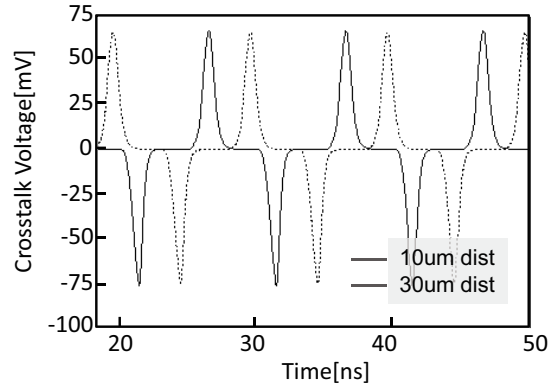

Fig. 10. Coupling path in the low frequency region.

Fig. 11. Crosstalk voltage of 100MHz digital signal when the distance between TSV is 10um, and 30um ($1\times$ driver).

of the channel differs in each frequency range (see Figure 9). Thus, by analyzing how the lumped components react to each other in the specific frequency range, we can predict how coupling would occur in each frequencies. In this paper, we categorize these frequencies in to three regions: the low frequency region ($< 1GHz$, (I)), the middle frequency region ($1GHz$ to $8GHz$, (II)), and the high frequency region ($> 8GHz$, (III)). Here, C_{bump} is ignored in the analysis due to the high impedance in all frequency regions, and $M_{TSV-TSV}$ is also ignored due to the small impact it has in the analysis.

In the low frequency region, the coupling path can be defined by C_{TSV} and R_{si}. Since the impedance of C_{si} is very high in this region, all the coupling current will detour through R_{si} (see Figure 10). Thus, inside the silicon substrate, the dominant coupling factor is the resistive coupling by R_{si}. The impedance of the channel in this frequency will be the impedance sum of C_{TSV} and R_{si}. However, since $Z_{R_{si}}$ is very low compared to $Z_{C_{TSV}}$, the impedance of the channel in this frequency can be expressed as the impedance sum of C_{TSV}s.

$$Z_{\text{Channel,Lowfreq}} \approx Z_{C_{TSV}} \qquad (12)$$

In contrary to the common belief, this phenomena describes that changing the distance between TSVs to alleviate coupling in this frequency region does not work well. For a digital signal in a specific frequency, it has its harmonic components (up to $7\times$). However, if there is a digital signal, whose frequency harmonics are all inside this low frequency range, changing the distance between TSVs would have a very small effect on alleviating coupling.

There are two reasons for this. Regarding Figure 9, the difference between channel impedance and the port impedance in the low frequency region is very big (more than 20dB). Due to the huge difference of the impedance, a slight change in the channel impedance would not result in a big difference

on the total coupling (see equation 6). The other reason is that the channel impedance is mainly determined by the TSV capacitance(see equation 12). C_{TSV} is defined as the capacitance between TSV and silicon substrate, which is mainly determined by the thickness of insulator. Therefore C_{TSV} is a fixed value once a 3D IC is made, and is insensitive with TSV distance change. Therefore, in this low frequency region, changing the distance between TSVs would not have a big impact. As it can be seen in Figure 11, the crosstalk voltage of a 100MHz digital signal that is generated at port 1 (size of $1\times$) in 10um distance TSVs and 30um TSVs are almost the same.

F. Dependency of Channel Impedance on Middle Frequency

In the middle frequency region ($1GHz$ to $8GHz$), the impedance of C_{TSV} becomes sufficiently low, and the impedance of C_{si} becomes comparable with $Z_{R_{si}}$. However, the impedance of C_{si} is still higher than R_{si} in this region, and most of the coupling current flows through R_{si}. The new phenomena which is observed in this region is that due to the
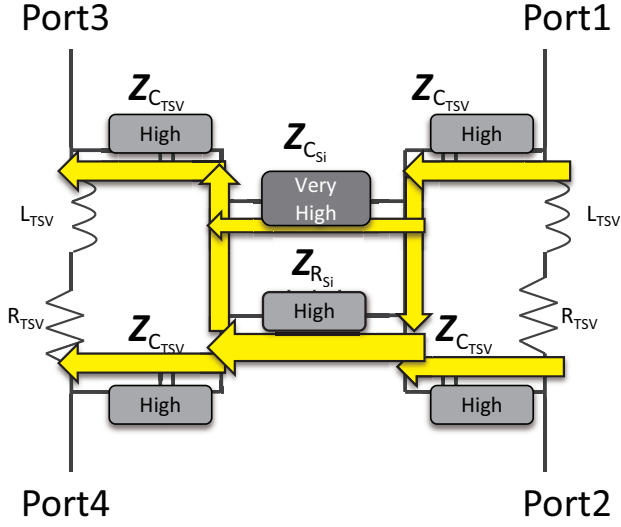
Fig. 12. Coupling path in the middle frequency region

Fig. 13. Crosstalk voltage of 3GHz digital signal when the distance between TSV is 10um, and 30um ($1\times$ driver).

smaller difference of these two impedances, C_{si} becomes a path for the coupling current to flow (see Figure 12). In this region, neither R_{si} nor C_{si} is a dominant coupling factor inside the silicon substrate. Both R_{si} and C_{si} affects the substrate coupling.

In conclusion, In the middle frequency region, impedance of all the components become similar to each other. Unlike in the low frequency region, no component has the dominating impedance value, and all the components are equally responsible for the coupling path. Thus impedance of the channel in this frequency region can be expressed as the sum of all components inside the channel.

$$Z_{\text{Channel,Midfreq}} = Z_{\text{C}_{\text{TSV}}} + Z_{\text{C}_{\text{si}}}//Z_{\text{R}_{\text{si}}} \qquad (13)$$

In the middle frequency region, the difference of impedance between port and channel becomes smaller (see Figure 9). Now that ΔZ between the channel and port is smaller, the output starts to respond to the change of numbers of each components (R_{si}, C_{si}, C_{TSV}). Starting from this region, the coupling voltage becomes dependant on the TSV distance.

Figure 13 describes the effect of TSV-to-TSV coupling in this region. For a signal whose harmonics are partly in the middle frequency region, the change of distance between TSVs affects TSV-to-TSV coupling.

G. Dependency of Channel Impedance on High Frequency

In the high frequency region (Over $8GHz$), all capacitance components (C_{si}, C_{TSV}) have an impedance lower than the resistance of silicon substrate (R_{si}). Since R_{si} is the highest impedance showing in this region, the coupling current detours R_{si}, and mostly flows through Csi inside the substrate (see Figure 14). In this region, the dominant coupling that occurs inside the silicon substrate is capacitive coupling through C_{si}. Since the capacitance of C_{si} is mostly smaller than C_{TSV}, the impedance of C_{si} is bigger than C_{TSV}. Thus, the impedance in this region is dominated by the capacitance of silicon substrate.
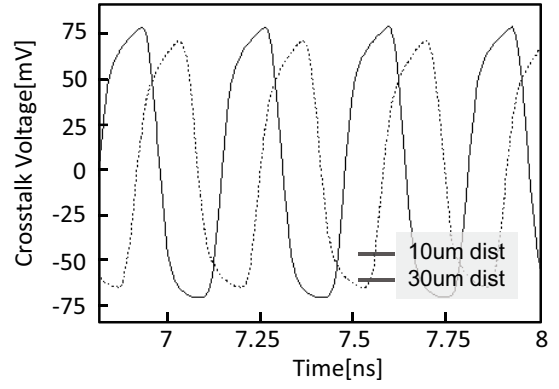
$$Z_{\text{Channel,Highfreq}} \approx Z_{\text{C}_{\text{si}}} \qquad (14)$$

The region that the coupling voltage is the most sensitive to the change of distance is the high frequency region. C_{si} is a factor which is solely determined by the change of distance. Since the dominating factor of $Z_{Channel,Highfreq}$ is C_{si}, this region is most sensitive to TSV distance.

The overall trend on TSV coupling to the change of distance is described in Figure 15. In the low frequency region (region 1), distance change among TSVs do not result in a big change in the coupling level. This is because the dominant component to the coupling is C_{TSV}, and C_{TSV} hardly changes with TSV distance. In the middle frequency region (region 2), distance change between TSVs starts to change the level of coupling. This is because C_{si} and R_{si} begin to have impact on $Z_{Channel,Midfreq}$ along with C_{TSV}. Since C_{si} and R_{si} are dependent on TSV distance, the coupling level starts to react on the change of TSV distance. In the high frequency region (region 3), the change in TSV distance has the biggest impact on coupling level. This is due to C_{si}, which dominates the impedance of the coupling channel.

H. A New Technique for Coupling Reduction

The most conventional way to reduce coupling is to increase the distance between TSVs. However, through our analysis in the previous chapters, we have shown that the change of distance between TSVs may not be very effective in reducing coupling. Therefore, in this section, we propose a technique to reduce coupling between TSVs.

TSV coupling reduction can be obtained by decreasing gate size of the aggressor, or increasing gate size of all other ports. Figure 16 compares the results of three different simulation settings when port 1 sends 1GHz digital signal ($1\times$ driver).

When the load impedance is fixed but TSV-to-TSV distance increases from $10\mu m$ to $30\mu m$, the peak noise decreases from $101.74mV$ to $95.13mV$. Although the distance change is big ($3\times$), the noise reduction is not as significant as the distance changes. This is because the $1GHz$ signal along with its major harmonics are in the low frequency region,
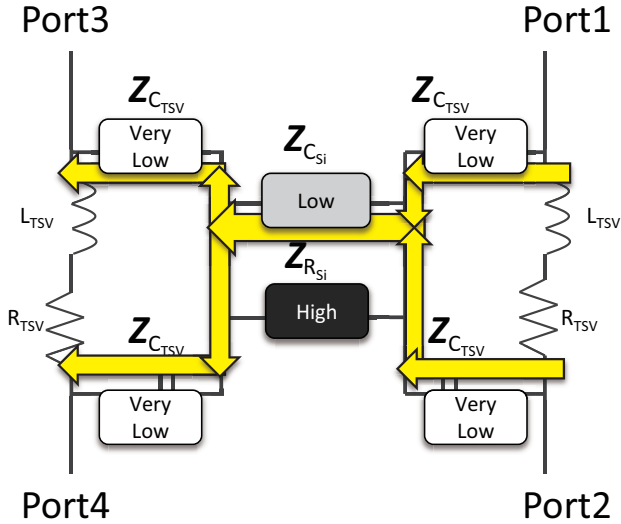
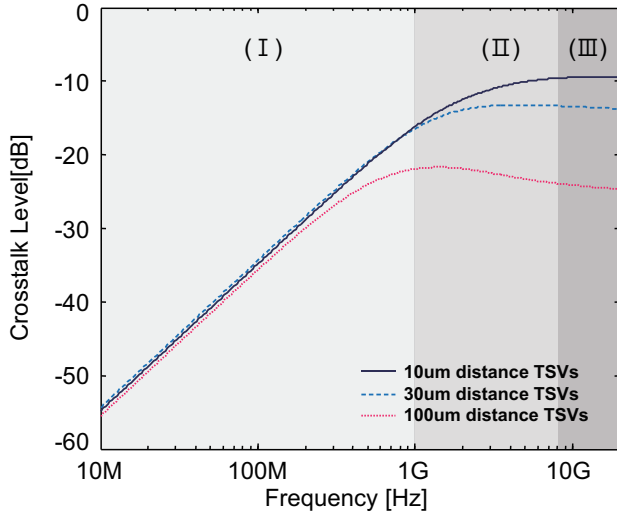Fig. 14. Coupling path in the high frequency region

Fig. 15. Frequency dependency on TSV coupling to distance on high impedance termination: (I) low frequency, (II) middle frequency, (III) high frequency.
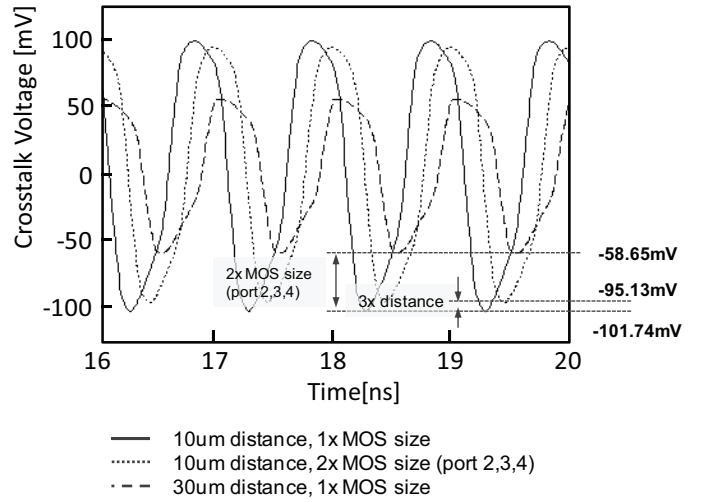

Fig. 16. Crosstalk voltage of 1GHz digital signal when distance and gate size have changed.

Based on this realistic model, we analyzed the impact of port impedance on TSV-to-TSV coupling, and showed coupling is more severe in high impedance termination than in 50-Ω termination condition.

We showed the relationship of TSV channel impedances in different frequency regions. We also showed that changing the distance between TSVs have different impact on different frequency regions. By this result, we proposed a new crosstalk reduction technique called gate sizing. By separating TSVs, we only achieved 6.5% improvement in the peak noise voltage (when $3\times$ distance), but by gate sizing ($2\times$ loads),we achieved 42.35% improvement in the peak noise voltage.

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where distance between TSVs does not affect the coupling level. On the other hand, when the TSV-to-TSV distance is fixed ($10\mu m$), while the load becomes $2\times$ bigger, the peak noise decreases from $101.74mV$ to $58.65mV$. Therefore, we observe that gate sizing (by increasing the gate size at the sink node, or increasing the gate size at the driving node on the victim net.) has more impact on coupling than increasing TSV-to-TSV distances.

IV. CONCLUSIONS

In this paper, we applied a lumped circuit model to analyze coupling between TSVs in 3D ICs and showed that this model is much more accurate than S-parameter-based coupling analysis with 50-Ω termination. This is mainly because high-impedance termination condition is more realistic than 50-Ω termination condition inside the digital IC.