Impact of Nano-scale Through-Silicon Vias on the Quality of Today and Future 3D IC Designs

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***Abstract*— One of the most effective ways to deal with the area and capacitance overhead issues with through-silicon vias (TSVs) in 3D ICs is to reduce the size of TSVs themselves. Today, the diameter of the smallest TSV available is around $1\mu m$, and this is expected to reach sub-micron dimensions in a few years. This downscaling of TSVs requires research on the impact of nano-scale TSVs on the quality of 3D IC designs to provide academia and industry with the quantified effects. In this paper, we investigate, for the first time, the impact of nano-scale TSVs on the area, wirelength, delay, and power quality of today and future 3D IC designs. For our future process technology, we develop a $22nm$ standard cell and interconnect library. We also use four sets of TSV-related dimensions in our GDSII-level 3D IC layouts. Based on these resources, we present a thorough study on the impact of nano-scale TSVs on the design quality of today and future 3D ICs.**

I. Introduction

Three-dimensional integrated circuits (3D ICs) are expected to achieve shorter wirelength, smaller critical path delay, and less power consumption than 2D ICs. However, it is shown that care must be taken to choose the right amount of through-silicon vias (TSVs) placed at the right spots in 3D IC layouts to achieve these goals [1]–[4]. This also indicates that if the area and capacitance overhead of TSVs themselves become smaller, less design effort is necessary to achieve improvement on area, delay, and power. This is the main motivation behind recent efforts in reducing the size of TSVs. For example, [5] uses $30\mu m$-diameter TSVs, [6] uses $5\mu m$-diameter TSVs, and [7] uses $1.2\mu m$-diameter TSVs. In addition, the TSV diameter in a recent research reaches $0.7\mu m$ [8]. According to these recent research and ITRS predictions, the TSV diameter will reach the sub-micron domain within the next few years.

Meanwhile, process technologies have advanced to $32nm$ [9]. In addition, more advanced process technologies such as $22nm$ and $16nm$ technologies are expected to be introduced within one to three years. Therefore, nano-scale (sub-micron) TSVs are likely to be used in future 3D IC designs with future process technologies. Then a major question would arise on whether these nano-scale TSVs used in future device/wire technologies will deliver significant improvement on performance and power. problems in reliability and cost. Our goal in this paper is to investigate the impact of nano-scale TSVs on the quality of current and future 3D ICs. The contributions of this paper are as follows:

- To investigate the impact of nano-scale TSVs on future 3D ICs, we develop a $22nm$ standard cell and interconnect library.
- We present detailed experimental results performed with various TSV sizes that represent today and future TSV technologies. Figure 1 shows the TSVs and gates used in our study. To the best of our knowledge, this is the first work that provides detailed GDSII-level demonstrations and predictions based on future process and TSV technologies.

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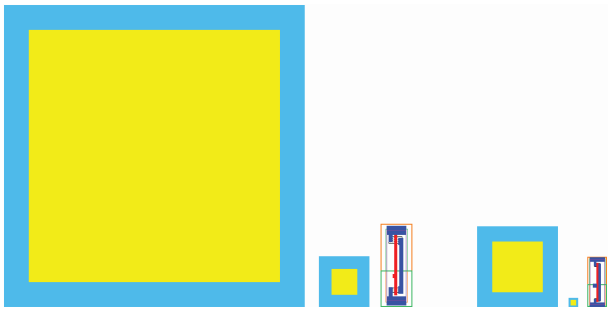

Fig. 1. TSVs and inverters (INV) under two different technologies used in our study (Cadence Virtuoso shot, shown in scale): (a) $5\mu m$ and $0.5\mu m$ width TSVs and INV under $45nm$ technology, (b) $1\mu m$ and $0.1\mu m$ width TSVs and INV under $22nm$ technology.

- Our study shows that TSV diameter has a huge impact on area, wirelength, delay and power consumption of 3D IC designs under both $45nm$ and $22nm$ technologies. In addition, we show that—if TSV count is carefully chosen—our 3D designs significantly outperform 2D counterparts in terms of wirelength and delay.

The rest of this paper is organized as follows. In Section II, we review negative impacts of TSVs on the quality of 3D ICs, and show motivations of this work. Section III demonstrates the development flow of our $22nm$ process technology, and compares a $45nm$ technology to our $22nm$ technology. In Section IV, we present the full-chip 3D IC design and analysis methodology used in our experiments. Various experimental results are presented and analyzed in Section V, and we conclude our work in Section VI.

II. Preliminaries

A. Negative Impacts of TSVs

The usage of TSVs in 3D ICs causes two negative impacts on the quality of 3D ICs: area and delay overheads. According to a recent research on TSV area overhead [10], silicon area occupied by TSVs is quite significant, which in turn reduces the wirelength benefit of 3D ICs. In addition, according to a recent research on TSV capacitance overhead [3], TSV capacitance is a significant source of delay on 3D signal paths. Moreover, buffer insertion performed to decrease the effect of TSV capacitance causes another problem: additional silicon area for buffers. Buffers also tend to increase the total wirelength. Therefore, ignoring TSV area and TSV capacitance leads to highly inaccurate estimation of wirelength, delay, and power.

The degree of negative effects of TSVs on 3D ICs is dependent on various technology and design parameters. For example, if we use

$5\mu m$ TSVs[1] with state-of-the-art process technologies such as $32nm$ technology in 3D IC designs, these TSVs may cause a huge area overhead. On the other hand, if we use $5\mu m$ TSVs with relatively old technologies such as $0.18\mu m$ technology, these TSVs may not cause any area overhead because the gates in these old technologies have similar area as the TSVs. Similarly, small TSVs (e.g., $1\mu m$ TSVs) can have huge capacitance if its liner is very thin. In this case, small TSVs may not cause serious area overhead, but they may cause serious delay overhead. The investigation of the degree of negative effects of TSVs in 3D ICs requires taking all the technology and design parameters such as TSV size, landing pad size, and TSV capacitance into account.

B. Motivations of Our Work

Downscaling of devices reached $32nm$ node [9] in 2009, and $22nm$ and $16nm$ technologies are currently under development. In addition, new TSVs with sub-micron dimensions are fabricated using state-of-the-art process technologies as presented in [5]. As the devices are downscaled as the process technologies advance, TSVs are also getting smaller. Although research is still being carried out to create $3\mu m$ to $5\mu m$ diameter TSVs, it is recently demonstrated that $0.7\mu m$ diameter TSVs can also be fabricated reliably [8] as of 2009. In addition, according to the ITRS predictions on TSV diameter and TSV aspect ratio, the TSV diameter will continue to decrease while the TSV aspect ratio will increase. Therefore, we expect that nano-scale TSVs will be developed and be ready for use within the next few years.

However, all of the existing work on the impact of TSVs on the quality of 3D IC designs are done with micron-size TSVs and current ($45nm$) or even old ($90nm$ and $130nm$) process technologies. For example, a $45nm$ technology and $1.67\mu m$ TSVs are used in [2], whereas a $45nm$ technology and TSVs whose width is approximately $4\mu m$ are used in [4]. As of 2011, $130nm$ is the only technology available for 3D multi-project wafer (MPW) runs via Tezzaron/MOSIS [11]. None of these works discuss what will occur if smaller TSVs are used in $45nm$ technology, or what will occur if the same-size TSVs are used in different process technologies (e.g., a $90nm$, $32nm$, or $22nm$ technology). However, it is crucial to accurately predict the impact of a new TSV technology on the design quality of 3D ICs in order to refine the technology or justify the investment and cost. Our goal in this paper is to study the impact of nano-scale TSVs on the area, wirelength, delay, and power quality of today and future 3D IC designs. For our future process technology, we develop a $22nm$ standard cell and interconnect library. We also use four sets of TSV-related dimensions in our GDSII-level 3D IC layouts. Lastly, we present a thorough study on the impact of nano-scale TSVs on the design quality of today and future 3D ICs.

III. Our 22nm Library

In this section, we show the development process of our $22nm$ process technology and its standard cell library. For $22nm$ transistor models, we use the $22nm$ high-performance transistor model of the predictive technology model ($22nm$ PTM HP model V2.1) [12]. The supply voltage of this transistor model is 0.8V.

A. Overall Development Flow

For the development of a $22nm$ process technology and its standard cell library, we follow a typical design flow illustrated in Figure 2. We first define device and interconnect layers. From the defined layers, we create a tech file (.tf), a display resource file (.drf), an interconnect technology file (.ict), a design rule file, a layout-versus-schematic rule file, and an RC parasitic extraction rule file. With the tech file, we draw layouts of standard cells. After the layout generation, we perform abstractions on these layouts to create a library exchange format file (.LEF), and run RC extraction and create SPICE netlists (post_xRC.cdl). With these SPICE netlists, we perform library characterization to create timing and power libraries (.lib and .db). We also generate a capacitance table and a .tch file for sign-off RC extraction and timing analysis.

[1]A "$X\mu m$ TSV" in this paper denotes a TSV whose width (= for square-shaped TSVs) or diameter (= for cylindrical-type TSVs) is $X\mu m$.

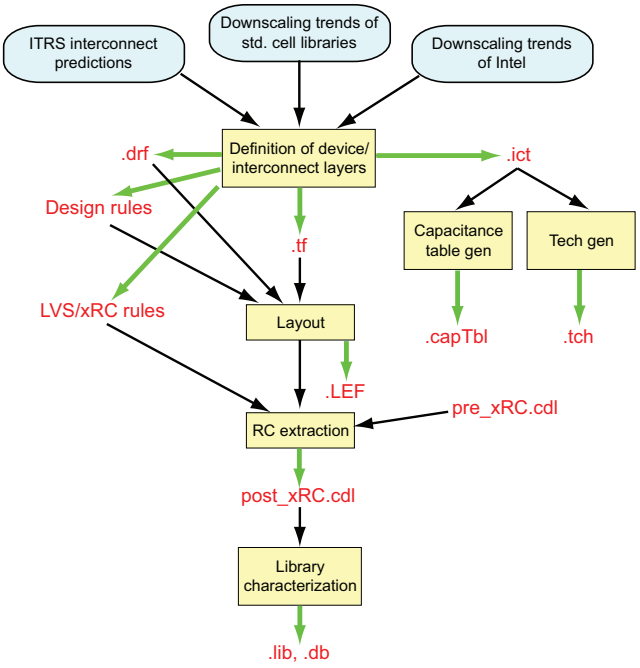

Fig. 2. Design flow of our $22nm$ standard cell library.

TABLE I
INTERCONNECT SCALING TREND OF $65nm$ [13], $45nm$ [14], $32nm$ [9], AND $22nm$ (OUR PREDICTION).

Layer	Pitch (nm)			
	$65nm$	$45nm$	$32nm$	$22nm$
Contacted Gate	220	160	112.5	86
Metal 1	210	160	112.5	76
Metal 2	210	160	112.5	76
Metal 3	220	160	112.5	76
Metal 4	280	240	168.8	130
Metal 5	330	280	225.0	206
Metal 6	480	360	337.6	206
Metal 7	720	560	450.1	390
Metal 8	1080	810	566.5	390

B. Interconnect Layers

We create interconnect layers of our $22nm$ technology based on ITRS interconnect predictions, downscaling trends of other standard cell libraries, and the downscaling trend of Intel process technologies [9], [13], [14]. According to ITRS predictions on interconnect layers, the pitch of the metal 1 wire at $22nm$ is about $72nm$, and the pitch of the semi-global wire at $22nm$ is about $160nm$. Table I shows the downscaling trend of the contacted gate pitch and pitches of metal 1 to metal 8 in Intel process technologies. Based on ITRS

TABLE II

INTERCONNECT DIMENSIONS USED IN OUR $22nm$ TECHNOLOGY. "ROUTING PITCH" IS THE ROUTING PITCH OF EACH METAL LAYER IN OUR $22nm$ STANDARD CELL LIBRARY.

Layer	Pitch (nm)	Thickness (nm)	Aspect ratio	Routing pitch (nm)
Contacted Gate	86			
Metal 1, 2, 3	76	64.8	1.8	90
Metal 4	130	108	1.8	136
Metal 5, 6	206	172.8	1.8	208
Metal 7, 8	390	324	1.8	400
Metal 9, 10	800	720	1.8	800
Metal 11, 12	1600	1440	1.8	1600

TABLE III

STANDARD CELLS IN OUR $22nm$ STANDARD CELL LIBRARY.

Type	Available sizes
AND2/3/4, AOI21/211/221	$1\times$, $2\times$, $4\times$
BUF, INV	$1\times$, $2\times$, $4\times$, $8\times$, $16\times$, $32\times$
LOGIC 0, LOGIC 1	$1\times$
MUX2	$1\times$, $2\times$
NAND2/3/4/, NOR2/3/4	$1\times$, $2\times$, $4\times$
OAI21/22/211/221/222	$1\times$, $2\times$, $4\times$
OAI33	$1\times$
OR2/3/4	$1\times$, $2\times$, $4\times$
XNOR2, XOR2	$1\times$, $2\times$
DFF	$1\times$, $2\times$
FA, HA	$1\times$

predictions and this trend, we show our predictions on the contacted gate pitch and pitches of metal layers of $22nm$ in the fifth column of Table I. Table II shows the pitches, thicknesses, aspect ratios, and routing pitches of metal layers of our $22nm$ technology. Since the aspect ratio of the Intel $32nm$ technology remains between 1.5 and 1.8, we use 1.8 for the aspect ratio of all metal layers. We also use 1.9 for the dielectric constant of the inter-layer dielectric, and 3.8 for the dielectric constant of the barrier material.

C. Standard Cell Library

We first create a tech file defining device and interconnect layers, and a set of design rules. Then, we draw standard cell layouts with this tech file and the design rules referring to standard cell layouts of the Nangate $45nm$ standard cell library [15]. We create about 90 cells, and Table III shows the list of these standard cells except antenna and filler cells. The placement site width and height of our $22nm$ technology are $0.1\mu m$, and $0.9\mu m$, respectively, and the width of the $1\times$ inverter, which is the smallest functional cell, is $0.3\mu m$.

D. 45nm vs 22nm Comparison

Before we proceed to the comparisons between 2D and 3D ICs in Section V, we compare our $22nm$ technology and standard cell library with the Nangate $45nm$ technology and standard cell library [15].

1) Gate and Interconnect Comparison: We perform SPICE simulations for a minimum-size inverter driving a load capacitor to compare drive strength of minimum-size inverters. To compare intrinsic characteristics of transistors, we do not include any parasitic RC of the inverter in this simulation. Figure 3 shows the rise and fall time of $45nm$ and $22nm$ inverters. As shown in the figure, the rise time of the $22nm$ inverter is smaller than that of the $45nm$ inverter, whereas the fall time of the $22nm$ inverter is larger than the $45nm$ inverter.

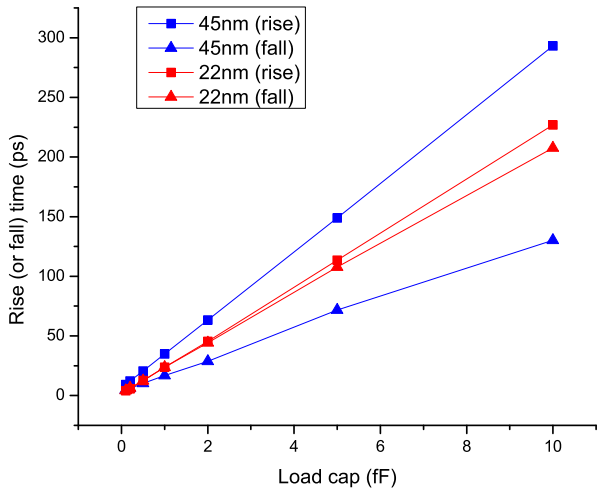

Fig. 3. Comparison of drive strength of a minimum-size inverter driving a load capacitor. Parasitic RC is not included.

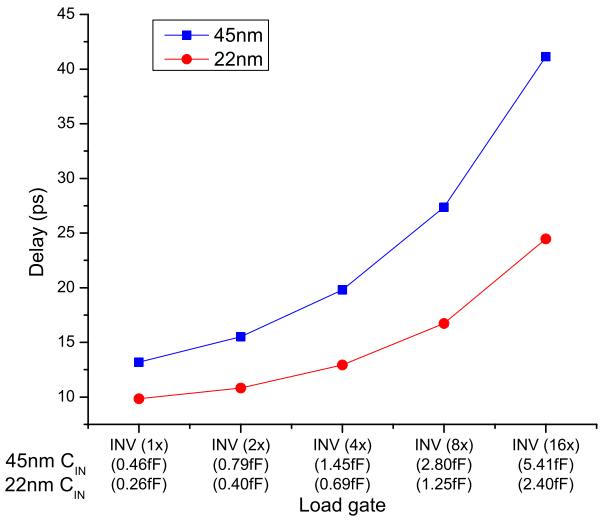

Fig. 4. Delay of a minimum-size inverter driving an $n\times$ inverter (n = 1, 2, 4, 8, 16). Parasitic RC is included. The numbers in the parentheses of the second (or the third) row in the x-axis are the input capacitances of the $n\times$ inverter.

In the above simulation, we apply a same load capacitance to the $45nm$ and the $22nm$ technologies. However, a gate drives other gates in real layouts. Therefore, if a gate is downsized in the next-generation process technology, load capacitance is also decreased. Thus, we also need to compare the delay of a gate driving other gates (e.g., FO4 delay). Therefore, we compare the delay of a minimum-size inverter driving a load inverter. In this simulation, we include RC parasitics and perform SPICE simulations on a minimum-size inverter driving a load gate, which is an $N\times$ inverter. Figure 4 shows the comparison. As the numbers in the second and the third x-axis rows in the figure show, the input capacitances of the $22nm$ inverters are smaller than those of the $45nm$ inverters. Therefore, the $22nm$ inverters have smaller delay than the $45nm$ inverters.

To compare the input capacitances of standard cells, we show the input capacitances of Nangate $45nm$ standard cells and our $22nm$ standard cells in Table IV. As shown in the table, input capacitances of our $22nm$ standard cells are approximately two times smaller than

TABLE IV

INPUT CAPACITANCES OF NANGATE $45nm$ STANDARD CELLS AND OUR $22nm$ STANDARD CELLS. IF A GATE HAS MULTIPLE INPUT PINS, WE SHOW THE AVERAGE INPUT CAPACITANCE OF ALL INPUT PINS.

Cell	Cap (fF)		Cell	Cap (fF)	
	$45nm$	$22nm$		$45nm$	$22nm$
AND2 1×	0.54	0.25	INV 4×	1.45	0.69
AOI211 1×	0.64	0.30	MUX2 1×	0.95	0.42
AOI21 1×	0.55	0.23	NAND2 1×	0.50	0.24
BUF 4×	0.47	0.28	OAI21 1×	0.53	0.25
DFF 1×	0.90	0.41	OR2 1×	0.60	0.26
FA 1×	2.46	1.31	XOR2 1×	1.08	0.55

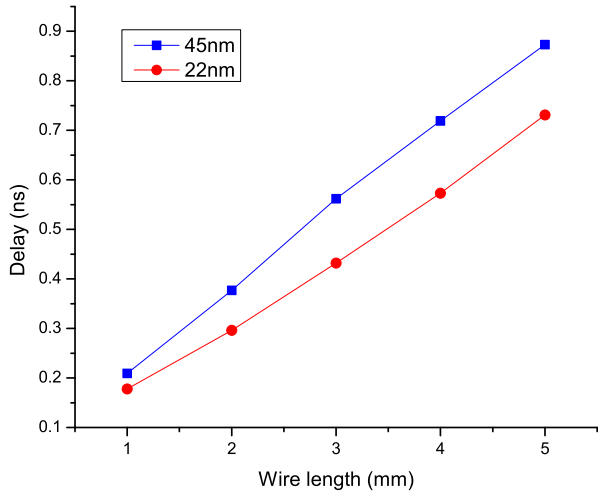

Fig. 5. Delay comparison of buffered global interconnects in $45nm$ vs $22nm$

those of the $45nm$ standard cells.

Figure 5 shows the comparison of the minimum propagation delay through a Xmm wire between two $1\times$ inverters after buffer insertion by Cadence Encounter. As shown in the figure, the $22nm$ model achieves better performance than the $45nm$ model. In this simulation, however, little capacitive coupling exists because only a single wire track is used between buffers. Therefore, we also perform another simulation when capacitive coupling exists between wires. In this comparison, the $22nm$ technology still shows lower delay than the $45nm$ technology.

2) Full-chip Design Comparison: In this experiment, we synthesize, design, and optimize benchmark circuits using the $45nm$ and the $22nm$ standard cell libraries under the same target frequency. Table V shows the comparison results. The chip area of the $45nm$ technology is about three times larger than that of the $22nm$ technology for both benchmarks. In addition, the total wirelength of the $45nm$ technology is about $1.9\times$ longer than that of the $22nm$ technology. The $22nm$ technology also shows better performance as shown in the table. The critical path delay of the $22nm$ technology is approximately 12% smaller than that of the $45nm$ technology for both the benchmark circuits. Similarly, the $22nm$ technology shows lower power consumption than the $45nm$ technology due to smaller pin capacitance, shorter total wirelength, and smaller device size.

IV. FULL-CHIP 3D IC DESIGN AND ANALYSIS METHODOLOGY

To generate 3D IC layouts, we use the 3D RTL-to-GDSII tool obtained from [4]. For a given 2D gate-level netlist, this tool partitions

TABLE V

COMPARISON OF THE $45nm$ AND $22nm$ TECHNOLOGIES FOR TWO BENCHMARK CIRCUITS.

	BM1 (120K gates)		BM2 (350K gates)	
	$45nm$	$22nm$	$45nm$	$22nm$
Area (mm^2)	0.189	0.063	0.912	0.317
Wirelength (m)	1.469	0.713	5.215	2.96
Delay (ns)	1.74	1.52	1.87	1.66
Power (W)	1.32	0.64	1.61	1.10

TABLE VI

BENCHMARK CIRCUITS

Tech.	Circuit	Profile	# Gates	# Nets
$45nm$	ckt1	Data Encryption Standard	108K	111K
	ckt2	Fast Fourier Transform (FFT)	278K	356K
$22nm$	ckt1	Data Encryption Standard	127K	128K
	ckt2	Fast Fourier Transform (FFT)	352K	372K

gates in x-, y-, and z-directions iteratively to place gates globally in 3D. After the global placement, it constructs a 3D Steiner tree for each net, and inserts TSVs into each placement grid based on the 3D Steiner tree. Then, it runs detailed placement in each placement grid using Cadence Encounter [16]. Routing for each die is also performed by Cadence Encounter. The tool finally produces a verilog netlist and a design exchange format (DEF) file containing TSV locations for each die, a top-level verilog netlist that contains die-to-die connections, and a top-level standard parasitic exchange format (SPEF) file.

After generating 3D IC layouts, we perform 3D timing optimization. We first perform a 2D layout generation and initial timing optimization for each die. Then, we feed all the layouts, timing analysis results, and the target clock frequency into the 3D timing optimization tool obtained from [17]. This 3D timing optimization tool iterates the following steps: (a) it performs RC extraction and obtains an SPEF file for each die, and (b) it performs 3D timing analysis using the SPEF files and the top-level SPEF file in Synopsys PrimeTime [18]. (c) Based on the timing analysis result and the target clock frequency, the tool scales target delays of 3D paths and creates a timing constraint file for each die. (d) Since each die has its own netlist and timing constraint file, we perform timing optimization for each die separately. We iterate this timing optimization process several times until the overall timing improvement saturates.

3D power analysis needs (a) a top-level netlist as well as a 2D netlist for each die, (b) a top-level SPEF file as well as a 2D SPEF file for each die, and (c) switching activities of cells and nets. To obtain switching activities of cells and nets, we load verilog netlists generated by the 3D RTL-to-GDSII tool obtained from [4] into Cadence Encounter, and run power analysis. This power analysis in Encounter internally generates and stores switching activities of cells and nets, so we dump these informations into an output file after the power analysis. Then, we load all the netlists, SPEF files, and the switching activity file into Synopsys PrimeTime [18], and run power analysis. This power analysis method produces true full-chip 3D power analysis results.

V. EXPERIMENTAL RESULTS

A. Experimental Settings

We use two benchmark circuits, ckt1 and ckt2, as shown in Table VI. For a $45nm$ technology, we use the Nangate $45nm$

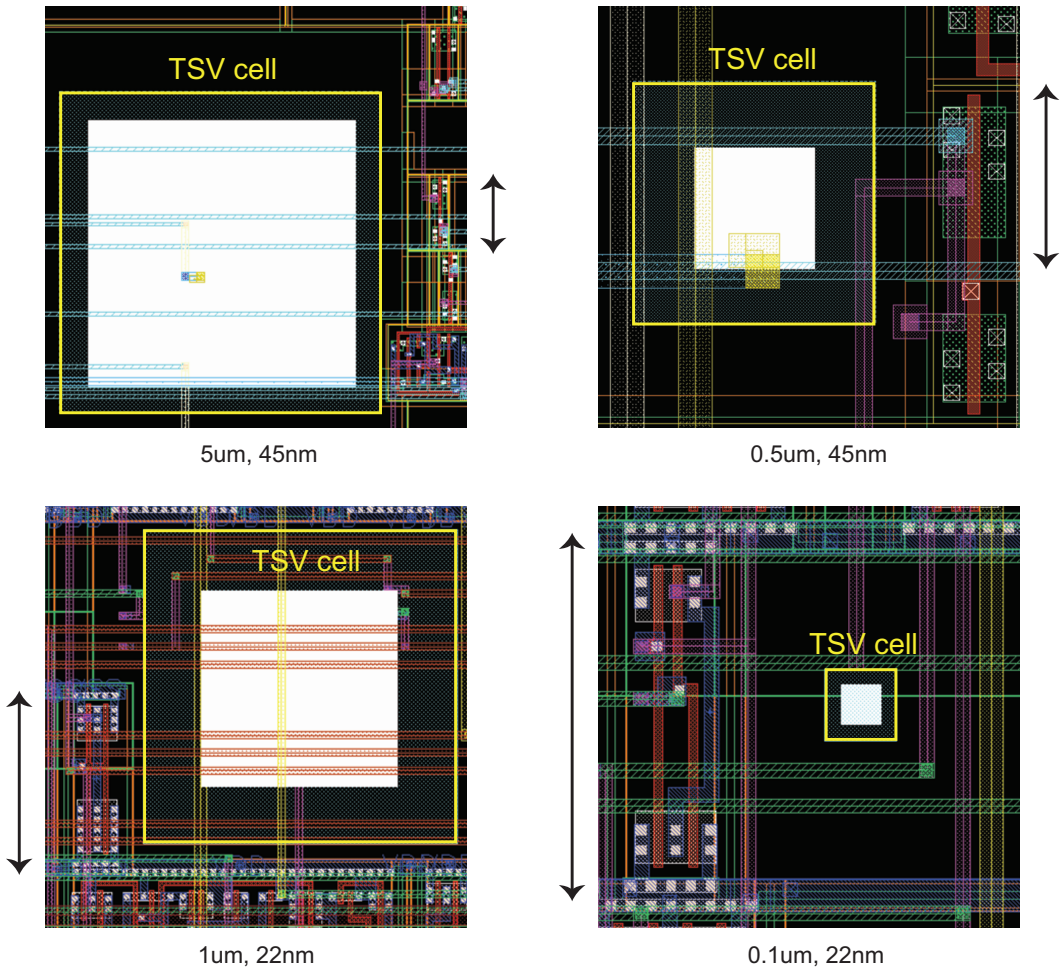

Fig. 7. TSV vs gate size comparison (Cadence Virtuoso GDSII layouts). The TSV cell (= yellow box) includes TSV landing pad and its keep-out zone. The arrow shows the height of the standard cell in each layout.

TABLE VIII

COMPARISON OF TSV AREA AND CELL AREA. WE SHOW THE RATIO BETWEEN THE TOTAL AREA OCCUPIED BY THE TSVS AND GATES. TSV COUNTS ARE SHOWN IN PARENTHESES.

Tech.	Circuit	3D									
		$0.5um$ TSV					$5um$ TSV				
$45nm$	ckt1	0.059 (4007)	0.099 (6719)	0.106 (7208)	0.111 (7537)	0.112 (7606)	1.469 (4002)	2.467 (6720)	2.643 (7200)	2.765 (7534)	2.790 (7601)
	ckt2	0.019 (6198)	0.107 (34448)	0.130 (41919)	0.164 (52835)	0.178 (57369)	0.213 (2744)	0.396 (5103)	1.301 (16786)	2.502 (32266)	3.379 (43576)
Tech.	Circuit	3D									
		$0.1um$ TSV					$1um$ TSV				
$22nm$	ckt1	0.003 (4856)	0.005 (7502)	0.006 (8615)	0.006 (8636)	0.006 (8543)	0.243 (3638)	0.368 (5497)	0.475 (7097)	0.497 (7434)	0.515 (7697)
	ckt2	0.003 (17989)	0.004 (19194)	0.004 (19269)	0.004 (19876)	0.004 (22200)	0.351 (19129)	0.366 (19960)	0.373 (20323)	0.368 (20047)	0.379 (20640)

technology and standard cells [15]. We also use four sets of TSV-related dimensions shown in Table VII. In our experiments, we use $5\mu m$ and $0.5\mu m$ TSVs with the $45nm$ technology, and $1\mu m$ and $0.1\mu m$ TSVs with our $22nm$ technology. The standard cell height of this $45nm$ technology is $1.4\mu m$, so the $5\mu m$ TSV occupies five $45nm$ standard cell rows while the $0.5\mu m$ TSV occupies one $45nm$ standard cell row, as shown in Table VII.

The standard cell height of our $22nm$ technology is $0.9\mu m$. Therefore, a $1\mu m$ TSV occupies three $22nm$ standard cell rows, and the $0.1\mu m$ TSV occupies 0.26 $22nm$ standard cell row. Notice that this occupancy includes the TSV width, the liner and barrier thicknesses, and the keep-out zone to satisfy the minimum TSV-to-TSV spacing and the minimum TSV-to-device spacing. Figure 6 shows top-down and side views of our four different TSVs, and Figure 7 shows GDSII images of our TSVs and standard cells under $45nm$ and the $22nm$ technologies.

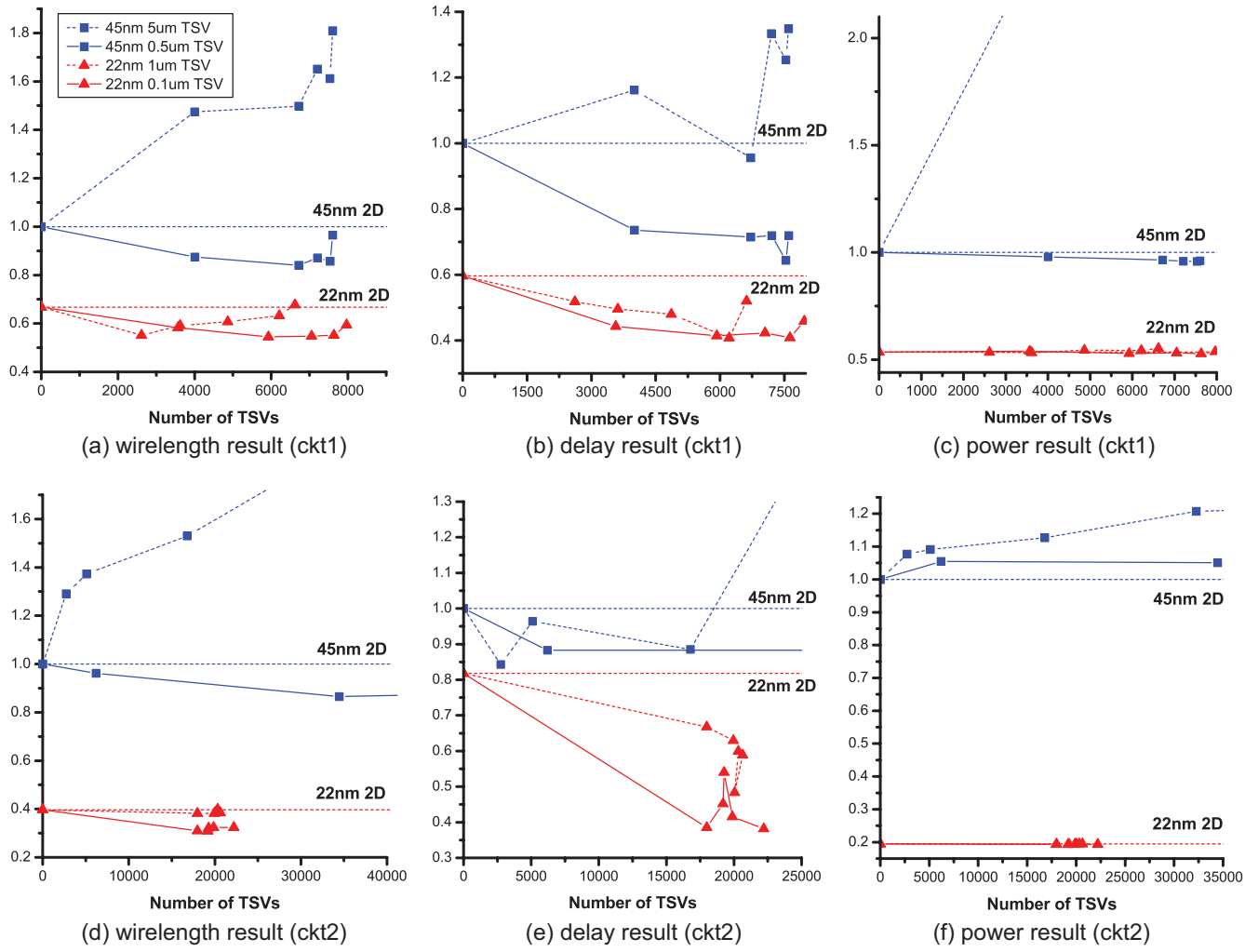

Fig. 8. Wirelength, delay, and power comparison among the full-chip 3D layouts designed with (1) $45nm$ technology + $5\mu m$ width TSV, (2) $45nm$ technology + $0.5\mu m$ width TSV, (3) $22nm$ technology + $1\mu m$ width TSV, and (4) $22nm$ technology + $0.1\mu m$ width TSV.

TABLE VII
TSV-RELATED DIMENSIONS, DESIGN RULES, AND TSV CAPACITANCE.

Dimensions	TSV-5	TSV-0.5	TSV-1	TSV-0.1
Width (μm)	5	0.5	1	0.1
Height (μm)	25	8	5	5
Aspect ratio	5	16	5	50
Liner thickness (nm)	100	20	30	10
Barrier thickness (nm)	50	20	30	5
Landing pad width (μm)	6	1	1.6	0.18
TSV-to-TSV spacing (μm)	2	0.6	0.8	0.1
TSV-to-device spacing (μm)	1	0.36	0.4	0.1
TSV capacitance (fF)	20	3.2	2.67	0.8
Underlying process tech	$45nm$	$45nm$	$22nm$	$22nm$
Standard cell row height	$1.4\mu m$	$1.4\mu m$	$0.9\mu m$	$0.9\mu m$
# cell rows occupying	5	1	3	0.26

B. Impact on Full-chip Area and Wirelength

Figure 8(a) and Figure 8(d) show the wirelength results normalized to that of the $45nm$ 2D design for ckt1 and ckt2. As shown in these figures, the $45nm$ + $5\mu m$ TSV cases have the longest wirelength for both circuits, while the $45nm$ + $0.5\mu m$ TSV cases have shorter wirelength than the $45nm$ 2D cases. In the $22nm$ technology cases, however, 3D designs are almost always better than the $22nm$ 2D designs. From these observations, we expect that the proper TSV size for $45nm$ process technologies is less than or equal to $0.5\mu m$ (or a bit larger than $0.5\mu m$) while the proper TSV size for $22nm$ process technologies is less than or equal to approximately $0.5\mu m$.

If we use $5\mu m$ TSVs with a $45nm$ technology, we cannot obtain any wirelength benefit from 3D designs. Even if we add TSVs to further reduce the wirelength as suggested in [2], the wirelength dramatically increases as shown in Figure 8(a) and Figure 8(d). This is because the area occupied by TSVs is so large that the footprint area increases significantly, and the average distance between cells increases, too.

Table VIII shows ratios between the total area occupied by TSVs and the total area occupied by gates. We also show the total TSV usage in parentheses. As shown in the table, $5\mu m$ TSVs occupy significant portion of the total area. For example, when $4,002$ TSVs are used in the $45nm$ design of ckt1, the total area occupied by TSVs is 1.469 times larger than the total cell area. Similarly, when $5,103$ TSVs are used in the $45nm$ design of ckt2, the total area occupied by TSVs is approximately 40% of the cell area. This big area overhead causes significant wirelength increase as shown in Figure 8(a) and

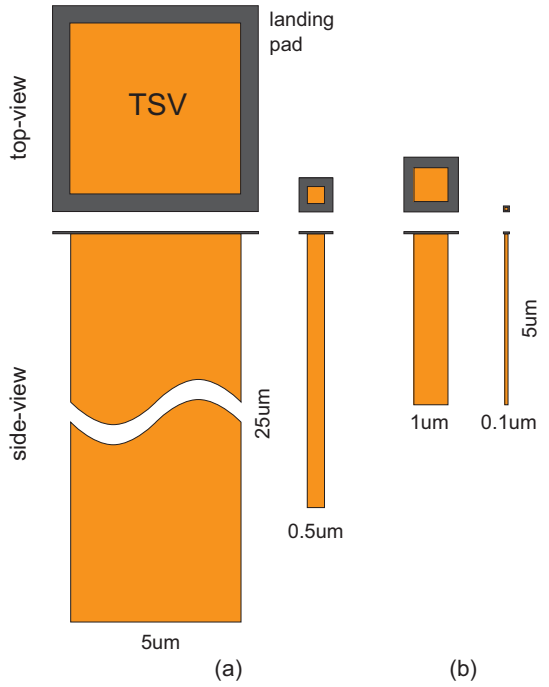

Fig. 6. Size comparison of the 4 TSVs used in our study: (a) $5\mu m$ and $0.5\mu m$ width used for $45nm$ technology, (b) $1\mu m$ and $0.1\mu m$ width used for $22nm$ technology.

Figure 8(d). However, when $0.5\mu m$ TSVs are used with the $45nm$ technology, the maximum TSV area overhead shown in Table VIII is only 11.2% for ckt1 and 17.8% for ckt2. Thus, TSVs in this case do not cause serious area overhead, which in turn helps us obtain shorter wirelength than 2D designs.

If we use the $22nm$ technology with $1\mu m$ or $0.1\mu m$ TSVs, the wirelength benefit of 3D designs increases further as shown in Figure 8(a) and Figure 8(d). Even when we use $1\mu m$ TSVs, the wirelength of 3D designs is shorter than the wirelength of 2D designs by up to 33%. However, we again observe that wirelength reduction is small or even minus (i.e., wirelength of 3D designs is longer than wirelength of 2D designs) when the TSV area occupancy is high (e.g., more than 40% of the cell area).

We also observe that the wirelength of 2D designs built with newer process technologies could be shorter than that of 3D designs built with older process technologies. For example, in both ckt1 and ckt2, the wirelength of $22nm$ 2D designs is shorter than the wirelength of $45nm$ 3D designs. This observation clearly implies that both the process technologies as well as TSV technologies have significant impact on the quality of 3D IC designs.

C. Impact on Full-chip Delay

Although 3D designs built with the $45nm$ technology and $5\mu m$ TSVs show much longer wirelength than 2D designs as shown in Figure 8(a) and Figure 8(d), critical path delays of 3D designs are not always worse than 2D designs as shown in Figure 8(b) and Figure 8(e). In Figure 8(b), the 3D design that uses $6,500$ TSVs shows smaller critical path delay than the 2D design. Similarly, when we use less than $17,000$ TSVs in Figure 8(e), the critical path delays of 3D designs are smaller than 2D designs. Therefore, we see that although $5\mu m$ TSVs cause serious area and wirelength overhead, critical path delay of 3D designs could be smaller than that of 2D designs.

3D designs built with the $45nm$ technology and $0.5\mu m$ TSVs have much smaller critical path delays than 2D designs for ckt1 as shown in Figure 8(b). In the best case in ckt1, the critical path delay is approximately 36% smaller than that of 2D designs. In ckt2, we also observe that the critical path delays of 3D designs are always smaller than the 2D designs.

In the $22nm$ technology cases, 3D designs always show smaller critical path delays than 2D designs. This is because $1\mu m$ and $0.1\mu m$ TSVs do not cause big problems in area and wirelength. Moreover, these TSVs have smaller TSV capacitance as shown in Table VII. Therefore, 3D designs of ckt1 have approximately 33% better delay than 2D designs, and 3D designs of ckt2 have approximately 100% better delay than 2D designs as shown in Figure 8(b) and Figure 8(e).

We also observe that 3D designs using the $45nm$ technology do not outperform the 2D design built with the $22nm$ technology. Therefore, we see that 3D designs built with older process technologies may not be able to outperform 2D designs built with newer process technologies in terms of critical path delay.

D. Impact on Full-chip Power

The parasitic capacitance of a $5\mu m$ TSV is about $20fF$, which is similar to the capacitance of a $100\mu m$-long wire, capacitively-coupled with neighboring wires in a $45nm$ technology. This large TSV capacitance for a $5\mu m$ TSV significantly increases the interconnect power. Figure 8(c) and Figure 8(f) show power overhead caused by TSV capacitance. For example, if $6,000$ $5\mu m$ TSVs are used for ckt1, the total TSV capacitance is larger than the total wire capacitance, and this huge total TSV capacitance results in a serious power overhead. In the ckt2 cases, however, power consumed in cells and wires is dominant, so the effect of the total TSV capacitance is not as large as that in ckt1 as shown in Figure 8(f). On the other hand, the TSV capacitance of a $0.5\mu m$ TSV is approximately $3.2fF$, which is about one-sixth of that of a $5\mu m$ TSV. Therefore, this capacitance does not cause any power overhead in ckt1. However, it leads to a bit higher power consumption in ckt2.

Although the TSV capacitance of a $1\mu m$ TSV is similar to that of a $0.5\mu m$ TSV, using $1\mu m$ TSVs does not cause any power overhead as shown in Figure 8(c) and Figure 8(f). Certainly, using $0.1\mu m$ TSVs does not lead to higher power consumption. The reason that $1\mu m$ TSVs or $0.1\mu m$ TSVs do not cause any power overhead is because the additional capacitance from TSV capacitance is compensated by the reduced total wire capacitance.

VI. Conclusions

In this paper, we investigate the impact of nano-scale TSVs on wirelength, delay, and power of current and future 3D ICs. For a future process technology, we create a $22nm$ technology and its standard cell library based on ITRS predictions and downscaling trends of process technologies. We also create four sets of TSV-related dimensions for use in current and future 3D ICs. With these process technologies and TSV dimensions, we generate several 3D IC layouts using 3D RTL-to-GDSII tools. The experimental results show that there exist proper TSV sizes for each process technology. For example, $0.5\mu m$ TSVs are suitable for $45nm$ technologies, while $0.1\mu m$ to $0.5\mu m$ TSVs are suitable for $22nm$ technologies. In addition, the TSV capacitance used in $45nm$ and $22nm$ technologies should be less than about $5fF$ and about $10fF$, respectively, to benefit from 3D designs. We also observe that wirelength and critical path delay of 3D designs built with older process technologies could be worse than 2D designs built with newer process technologies.

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