Backend Dielectric Chip Reliability Simulator for Complex Interconnect Geometries

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***Abstract*—Backend dielectric breakdown degrades the reliability of circuits. We present test data and a methodology to estimate chip lifetime due to backend dielectric breakdown. Our methodology incorporates failures due to parallel tracks, the width effect, and field enhancement due to line ends. The impact of line ends has been found to be very significant experimentally, and it is demonstrated that this component can dominate the failure rate of the chip due to dielectric breakdown.**

Keywords-TDDB; dielectric breakdown; chip lifetime; reliability; irregular interconnect geometries

I. INTRODUCTION

Each technology generation reduces the interconnect dimensions without always reducing the supply voltage in proportion. This results in higher electric fields within the backend dielectric. At the same time, at the dielectric constant (k) decreases to reduce parasitics, as prescribed by the *International Technology Roadmap for Semiconductors,* the porosity of materials must increase, at the possible cost of increasing the vulnerability of materials to breakdown. These factors combine to increase the risk of failure of chips due to backend dielectric breakdown in the newer technology nodes.

To better understand the impact of the backend dielectric on design, this work builds an interface between reliability physicists, semiconductor foundry engineers, and designers by linking test structure data to chip-level lifetime estimates. The purpose of our work is to introduce backend dielectric reliability in design, by conveying to the designer accurate estimates of chip lifetimes in a designer-friendly manner. To do this, we need to understand the relationship between interconnect geometries and lifetime.

It is a common assumption that the vulnerable area for backend dielectric breakdown for a full chip is the area between minimum spaced lines. However, in prior work, we have shown that it is necessary to take into account all areas with different line spaces [1],[2]. If only the area between minimum spaced lines is considered, as suggested in [3], lifetime estimates will be inaccurate.

In addition to the vulnerable area, we have found that lifetime depends on linewidth [2],[4] even when the line space is constant, due to aspect ratio dependent etch (ARDE) [5],[6]. Others have demonstrated dependencies on the presence of vias [7] and line edge roughness [8].

As the number of unique features in a layout increases, because of challenges in reducing the wavelength in lithography, the layout geometries that we have considered so far may not be sufficient. In fact, 193 nm lithography has been used for at least five technology generations and the domain of influence of lithography now extends well beyond the nearest feature and the nearest neighboring cell in a standard cell design. The ability to print smaller geometries has been accomplished through a variety of mask engineering techniques. The mask engineering techniques, nevertheless, cannot guarantee that a layout will result in a circuit that yields adequately due to modeling errors and algorithmic inaccuracies. In fact, only lithography (and only the aerial image) and chemical mechanical polishing (CMP) have reasonably accurate process models [9]. Other models are empirical and calibrated to rapidly changing processes. Hence, design rule clean layouts have been known to yield poorly due to unanticipated layout geometries [9]. Therefore, it is important to consider the impact of these irregular geometries on backend dielectric breakdown.

This work focuses on the impact of geometry on lifetime. We analyze data from backend dielectric test structure with irregular geometries and show that they may dominate full chip lifetimes.

In this paper, we first summarize our methodology to estimate lifetime, based on data collected from test structures, in the next section. Section 3 discusses our test structures, test data, and analysis of the impact on circuit lifetime. Section 4 incorporates the test structure features in the simulator. We present the algorithms and results in Section 5 and 6, respectively. This paper is concluded in Section 7 with a summary.

II. BACKEND DIELECTRIC BREAKDOWN MODELS AND SIMULATION

The most important reliability concerns for interconnects are electromigration, stress-induced voiding, and time-dependent dielectric breakdown (TDDB) of the backend dielectric. Our purpose is to consider only TDDB of the backend dielectric.

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A. TDDB Models

We note that models that describe backend TDDB, although they may have been initially developed for device TDDB, are of the general form [10]-[13]

$$\ln TF = A - \gamma E^m \tag{1}$$

where A is a constant that depends on the material properties of the dielectric, γ is the field acceleration factor, m is one for the E model and $1/2$ for the $\sqrt{E}$ model, and TF is the time-to-failure. Equation (1) provides a correction between the electric field during use conditions and during accelerated stress tests. Geometries with different line spacings scale differently to use conditions, as noted in [1],[3]. It should also be noted that although these models can be generally represented in this form, they are based upon very different physical mechanisms. This representation is only used for modeling.

Time-to-failure is also a function of temperature. The temperature dependence is modeled with an Arrhenius relationship [12] [14]

$$\ln TF = A - Ea/kT\,, \tag{2}$$

where A is a constants, k is the Boltzmann constant and the activation energy, Ea, is field dependent and can be derived as:

$$Ea \propto q(\phi_B - \sqrt{qE/\pi\varepsilon})\,, \tag{3}$$

where q is the electronic charge, ϕ_B is the trap barrier height, and ε is the dielectric constant. Equation (2) provides a correction between chip operating conditions and accelerated stress conditions. There is a concern that stressing at high temperatures can activate failure modes that are not present during use conditions. Hence, stressing at high electric fields is preferred in comparison with testing at high temperatures. Our tests were conducted at $150^o C$.

B. Chip Lifetime Models

It should be noted that circuits wearout for a variety of reasons, both related to devices and interconnect. All of these wear-out mechanisms happen simultaneously. It is common to describe reliability mechanisms with a Weibull distribution

$$P(TF) = 1 - \exp\left(-(TF/\eta)^{\beta}\right), \tag{4}$$

having two parameters: the characteristic lifetime, η, and shape parameter, β. The characteristic lifetime is the time-to-failure at the 63% probability point, when 63% of the population have failed, and the shape parameter describes the dispersion of the failure rate population. Typically, the shape parameter is close to one. If we have a collection of n independent wearout mechanisms modeled with Weibull distributions, having parameters, $\eta_i, i = 1,...,n$, and $\beta_i = i = 1,...,n$, then the characteristic lifetime of the system, η_{chip}, i.e. the time when 63% of the population has failed from any mechanism, is the solution of [1],[2],[15]:

$$1 = \sum_{i=1}^{n} \left(\eta_{chip}/\eta_i\right)^{\beta_i} \tag{5}$$

Similarly [2],

$$\beta_{chip} = \sum_{i=1}^{n} \beta_i \left(\eta_{chip}/\eta_i\right)^{\beta_i}\,. \tag{6}$$

The components in equations (5) and (6) could be different wearout mechanisms, different layers of a chip, different geometries within a layer, or different geometries within a layer at different temperatures. Hence, all a reliability simulator has to do is to (a) determine the characteristic lifetimes and shape parameters for all of the underlying wearout mechanisms and geometries, after all components are scaled for temperature and to use conditions with equations (1) and (2), and (b) apply equations (5) and (6) to solve for η_{chip} and β_{chip}.

III. The Test Structures and Test Results

A. The Test Structures

Test structures have been used to collect data on individual features in a layout. We have implemented test structures that vary area, linespace, and linewidth [2],[4],[16]. Fig. 1 shows top views of comb test structures used in this study. The test structure in Fig. 1(a) is used to determine the lifetime of the dielectric between parallel tracks with a specific line spacing. This test structure has a fixed linespace, *S,* and vulnerable length, *L*. The vulnerable area is *LS*. To test the lifetime of such a feature, a voltage difference is applied between the two combs. The current between the combs is monitored to determine the time-to-failure. The data set from several samples is fit with a Weibull distribution to estimate η_t and β_t.

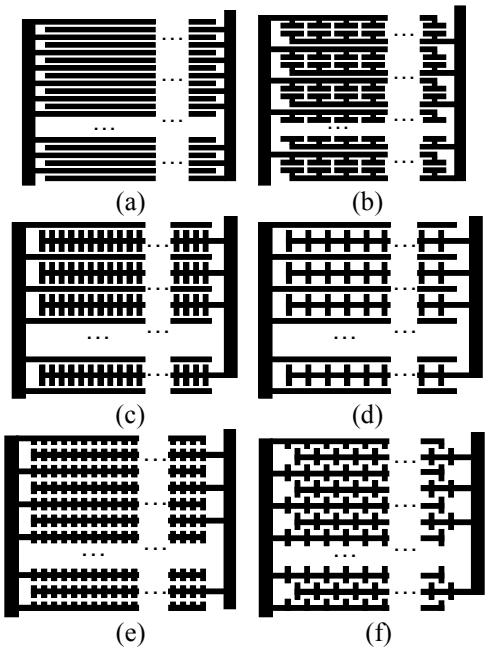

Fig. 1. Test structures to characterize the impact of geometry on backend time-dependent dielectric breakdown. (a) Reference, (b) PTT, (c) TLa, (d) TLb, (e) TTa, and (f) TTb

Because the features on a chip differ from this feature in a a test structure layout, area scaling must be performed to adjust the lifetime to take into account the difference in vulnerable area between the chip and the test structure. To do this, let L_t and L_i be vulnerable lengths of the test structure and chip, i.e. the length of the lines that run in parallel in the test structure and chip, respectively, with the same line space, *S.* η_t is determined by stressing a test structure with vulnerable linespace *S* of length L_t. Then the corresponding characteristic lifetime for that feature in the chip is

$$\eta_i = \eta_t (L_t / L_i)^{1/\beta} . \quad (7)$$

In previous work, we have shown that there can be substantial field enhancement at tips and bends of irregular geometries [17]. Some geometries have been shown to increase the electric field within the dielectric by as much as a factor of three. Such field enhancement may lead to reduced lifetimes.

We have designed test structures that have several irregular features in order to determine any impact of field enhancement. Fragments of the test structures are shown in Fig. 1(b)-(f). PTT emphasizes the electric field between parallel routing tracks that end at the same point. TLa and TLb emphasize the electric field between line ends and perpendicular lines. TLb includes additional fringing fields, since the line ends are more widely spaced. TTa and TTb emphasize electric fields between line ends. In TTa, the line ends abut, and in TTb the line ends are in parallel tracks. TTb has 522 line ends and TLa, TLb, TTa have 264 line ends each. The separation between line ends is the same for all test structures.

All test structures in Fig. 1 have the same minimum line space, 140nm. If the drawn line space is consistent with the printed line space, then the relative influence of each geometry would be the same. Moreover, the number of vulnerable line ends for each geometry in Figs. 1(c)-(e) is constant, i.e. 264 line ends each. Hence, when comparing the test structure in Figs. 1(c)-(e), no area scaling is required (using equation (7)) when comparing the results. On the other hand, we require area scaling to determine if the test structures in Fig. 1(b)-(e) results in an increase failure rate in comparison with parallel lines, as in Fig. 1(a). The test structures were tested at 3.6MV/cm and at $150^\circ C$, and the current between the lines was monitored . A current limit of 10 μA was set to detect dielectric breakdown.

B. Test Results

Let's suppose that there is no field enhancement due to any of the features in Figs. 1(b)-(f). Then the lifetime data from the test structure in Fig. 1(a) would be sufficient to predict the lifetimes of the test structures in Figs. 1(b)-(f). We make this assumption and extract the vulnerable length, *L,* and linespace, *S,* for the test structures in Figs. 1(a)-(f).

Next, we compare the measured Weibull curves for the test structures in Fig. 1(b)-(e) with the Weibull curve from the standard comb test structure with the same linespace, *S,* in Fig. 1(a), area scaled [18] – by using the Poisson area scaling invariance of the Weibull distribution – to match the vulnerable length of the test structures in Figs. 1(b)-(e).

Specifically, let $N = L_t/L_i$ be the ratio of vulnerable length, where L_t corresponds to the vulnerable length of the standard comb structure in Fig. 1(a) and L_i corresponds to the vulnerable length in one of Figs. 1(b)-(e). To area-scale the standard comb structure to give us the lifetime distribution for a different (smaller) vulnerable area, we plot

$$\ln \eta_t = \ln TF - \frac{1}{\beta} ln\left(-\frac{1}{N} ln(1 - P(TF))\right) . \quad (8)$$

The data collected from the test structures is presented in Fig. 2, Fig. 3, and Fig. 4. An area scaled version (with (8)) of the data from the reference structure is also included for comparison. It can be seen that all test structures (PTT, TLa, TLb, TTa, and TTb) result in a significantly reduced lifetime in comparison with the reference test structure. The data also indicate that TLa and TLb fail at the same rate, indicating that fringing fields are not significant. The data from these two test structures can be merged to determine a single model. TTa has an improved lifetime, in comparison with TLa/b. Most likely this is due to line-end pull-back. Specifically, if TLa and TLb experience pull-back, then TTa experiences twice the pull-back. No reference curve is included for comparison for TTb because TTb has no vulnerable length.

Since the test results indicate all of the line ends create an increased vulnerability for PTT, TLa, TLb, TTa, and TTb and fail more rapidly, the counts of the vulnerable line ends with these geometries need to be incorporated separately from the vulnerable length in the simulator when estimating the wear-out of a full chip. These geometries are illustrated in Fig. 5.

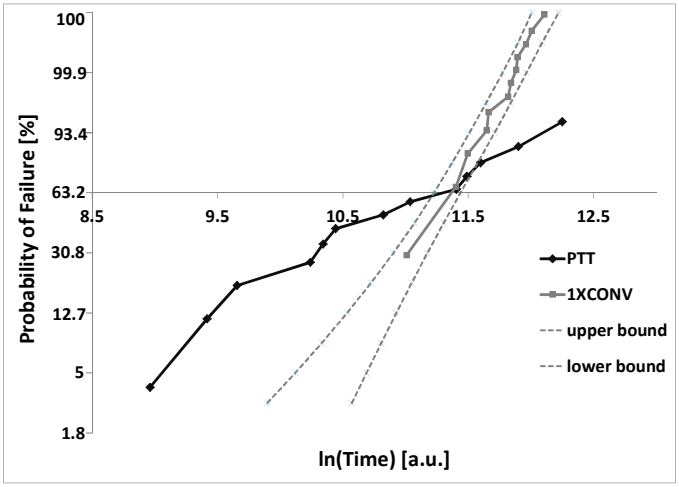

Fig. 2. Data collected from PTT vs. the reference structure. 2σ confidence bounds are included for the ara scaled reference test structure.

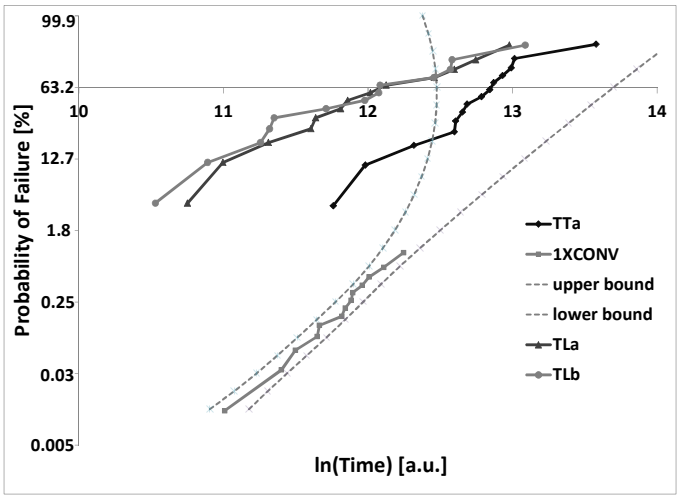

Fig. 3. Data collected from TLa, TLb, and TTa vs. the reference structure. 2σ confidence bounds are included for the area scaled reference test structure.

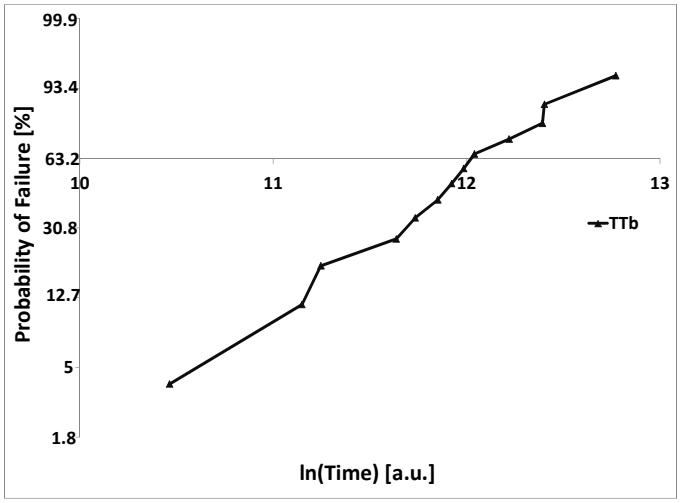

Fig. 4. Data collected from TTb.

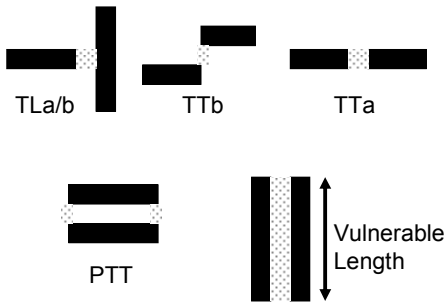

Fig. 5. Vulnerable line ends that need to be extracted from a layout.

C. Model Construction

A model was extracted for PTT, TLa/b, TTa, and TTb. We find the model for TTa and TTb with the standard method, involving fitting a linear function to the data to find η_{TTa}, β_{TTa}, η_{TTb}, and β_{TTb}.

Extraction of the model for TLa/b and PTT is more complex since these structures combine both line ends and vulnerable length. To find the model for line ends, it is necessary to subtract the effect of vulnerable length. Let η_{TS} and β_{TS} be the measured data from the test structures TLa/b and PTT. For each of these test structures we need to determine η_{ends} and β_{ends}, after eliminating the component due to vulnerable area, η_{area} and β_{area}. The parameters, η_{area} and β_{area}, are determined from the area scaled data from the reference test structure.

Relying on (5) and (6), we have that

$$1 = \left(\frac{\eta_{TS}}{\eta_{ends}}\right)^{\beta_{ends}} + \left(\frac{\eta_{TS}}{\eta_{area}}\right)^{\beta_{area}} \tag{9}$$

and

$$\beta_{TS} = \beta_{ends}\left(\frac{\eta_{TS}}{\eta_{ends}}\right)^{\beta_{ends}} + \beta_{area}\left(\frac{\eta_{TS}}{\eta_{area}}\right)^{\beta_{area}}. \tag{10}$$

Rearranging the equations results in

$$\beta_{ends} = \frac{\beta_{TS} - \beta_{area}\left(\frac{\eta_{TS}}{\eta_{area}}\right)^{\beta_{area}}}{1-\left(\frac{\eta_{TS}}{\eta_{area}}\right)^{\beta_{area}}} \tag{11}$$

and

$$\eta_{ends} = \eta_{TS}\left(1 - \left(\frac{\eta_{TS}}{\eta_{area}}\right)^{\beta_{area}}\right)^{-1/\beta_{ends}}. \tag{12}$$

These equations were used to extract the model for TLa/b. Because of the large separation between the data and the reference, the shift in η and β due to subtracting the impact of vulnerable area is less than 0.1% and 1%, respectively. This is illustrated in Fig. 6.

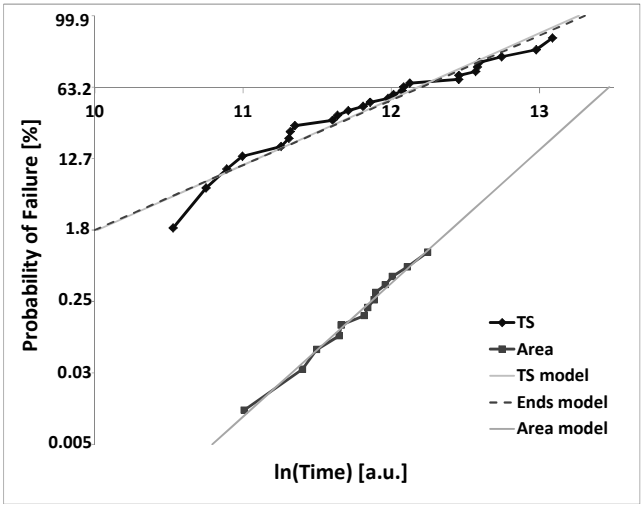

Fig. 6. Data collected from TLa/b vs. the reference structure. The models for the data from the test structure and the line ends, after subtracting the effect of area are nearly indistinguishable.

Equations (11) and (12) cannot be used for PTT. This is because (6) and (10) were derived by finding the probability density function of the combined failure rate as a function of the underlying parameters, converting to the Weibull probability scale (i.e. $\ln(-\ln(1-P))$), and evaluating the slope at the characteristic lifetime, η. As can be seen from Fig. 2, PTT impacts lower probabilities, and the slope is not well defined at the x-intercept of the Weibull plot.

Instead, we need to find η_{ends} and β_{ends} by defining the probability density function for the test structure as a function of *TF,* for any value of *TF,* i.e.,

$$P(TF) = 1 - exp\left(-\left(\frac{TF}{\eta_{TS}}\right)^{\beta_{TS}}\right). \quad (13)$$

Since this probability density function results from two independent mechanisms, we also have that

$$P(TF) = 1 - exp\left(-\left(\frac{TF}{\eta_{ends}}\right)^{\beta_{ends}} - \left(\frac{TF}{\eta_{area}}\right)^{\beta_{area}}\right). \quad (14)$$

Hence,

$$\left(\frac{TF}{\eta_{ends}}\right)^{\beta_{ends}} + \left(\frac{TF}{\eta_{area}}\right)^{\beta_{area}} = \left(\frac{TF}{\eta_{TS}}\right)^{\beta_{TS}}. \quad (15)$$

We solve for the unknowns, η_{ends} and β_{ends}, by finding the best fit to the data in the range where end failures are dominant, through linear regression. The results are shown in Fig. 7.

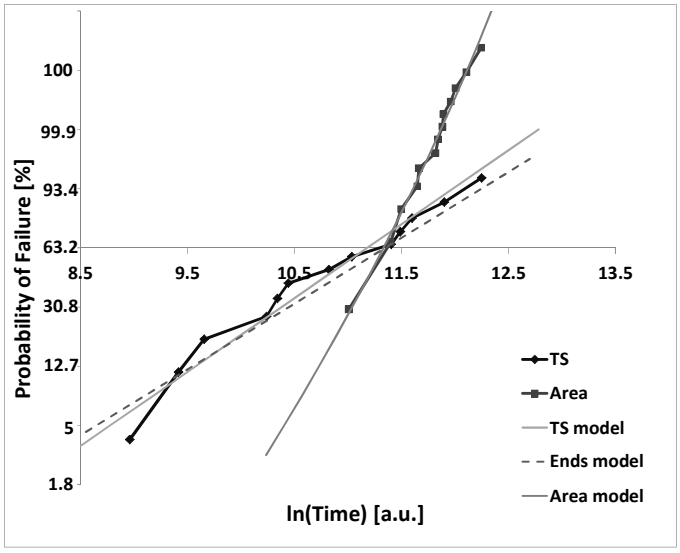

Fig. 7. Data collected from PTT vs. the reference structure. The graph shows the models for the data from the test structure vs. the line ends, after subtracting the effect of area.

IV. TDDB Chip Lifetime Simulator

A. Vulnerable Area and Full Chip Reliability Simulation

The simulator operates by determining the vulnerable area of the chip layout. In essence, our simulator extrapolates test structure results to the entire product die. The vulnerable area is defined as the area of a block of dielectric between the two copper lines separated by linespace S_i for length L_i and having an area S_iL_i. The feature that is extracted from layouts is the vulnerable length between two lines L_i associated with a linespace S_i, which is a function of the widths of the two adjacent lines, $W_{i,L}$ and $W_{i,R}$, illustrated in Fig. 8. A given layout is analyzed by determining the pairs ($S_i(W_L,W_R)$, L_i) for each layer for all linespaces surrounded by the linewidths W_L and W_R. The details of our methodology can be found in [1],[2],[15]. Here we give its gist in the following subsections.

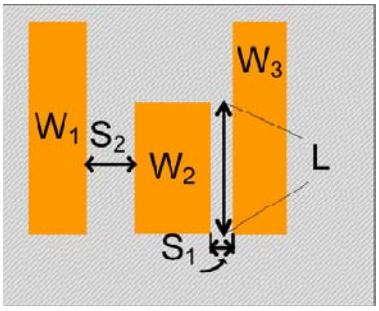

Fig. 8. Vulnerable area associated with a line space. The rectangles are Cu wires and the shaded area is the backend dielectric.

Next, after feature extraction, we compute features-level Weibull parameters and combine these to determine the full-chip lifetime parameters. Let η_t be the Weibull characteristic lifetime for a test structure with vulnerable linespace S_i of length L_t, and area $A_{it} = L_tS_i$. Then, if the chip has a vulnerable length L_{ij} associated with the same linespace S_i, and area $A_{ij} = L_{ij}S_i$, on the *j*th layer, the corresponding characteristic lifetime of the portion of the layer with linespace S_i is [1],[2]

$$\eta_{ij} = \eta_t(L_t/L_{ij})^{1/\beta ij}, \quad (16)$$

where β_{ij} is the Weibull shape parameter for the *i*th linespace in the *j*th layer. If there is not test structure with the linespace, S_i, η_t is found using other test structures and the field acceleration equation (2).

Since each layer has many spacings, S_i, and a chip has many layers, the characteristic lifetimes and shape parameters are combined with (5) and (6).

B. Inclusion of Line End Field Enhancement in Full Chip Reliability Simulation

In this work, we also extract counts of the features in Fig. 5. The line ends, with the geometries shown in Fig. 5, each add additional parameters, η_{PTT}, β_{PTT}, $\eta_{TLa/b}$, $\beta_{Tla/b}$, η_{Tla}, β_{Tla}, η_{TTb}, and β_{TTb} to (5) and (6). These parameters depend on the number of minimally spaced line ends in each category of the layout. Let's consider the computation of $\eta_{Tla/b}$ for the sake of

illustration. Let's suppose the test structure has N_{test} minimally spaced line ends, from which η_{test} and $\beta_{Tla/b}$ are computed. Then, for a layout with N_{chip} similar line ends, by area scaling

$$\eta_{Tla/b} = \eta_{test}(N_{test}/N_{chip})^{1/\beta_{TLa/b}}. \quad (17)$$

It should be noted that only the smallest values of η_{ij} influence the failure rate of a chip. Layout style can significantly influence the vulnerability of a chip to line ends.

V. Feature Extraction

A. Process

The NCSU 45nm technology library was used for our simulation experiments [19]. This process has ten metal layers, and the details of relevant features are given in Table 1.

TABLE 1. Metal layers in NCSU 45nm PDK

Metal Layer	Minimum Linewidth [nm]	Minimum Linespace [nm]
1	65	65
2,3	70	70
4, 5, 6	140	140
7, 8	400	400
9, 10	800	800

B. Circuits

We synthesized the radix-2 pipelined, 256-points, Fast Fourier Transform (FFT) HDL source code [20]. The circuit *cf_fft_256_8* has 324k gates and 329k nets. The block diagram of the circuit is shown in Fig. 9.

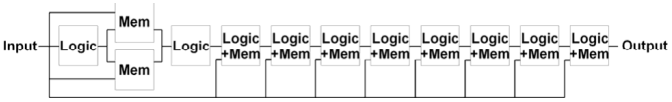

Fig. 9. Block diagram of a FFT circuit.

Synopsys Design Compiler is used for synthesis [21]. Cadence SoC Encounter is used for placement, clock-tree synthesis, routing, optimization, and RC extraction [22]. Synospys PrimeTime is used for timing analysis [23]. We use Metal1 to Metal5 during routing and analyzed the impact on reliability for each layers.

C. Vulnerable Area and Vulnerable Feature Extraction

In prior work, we presented the algorithm to extract vulnerable area [1]. In this work we have added the extraction of the vulnerable features in Fig. 8, as shown in Algorithm 1. Two inputs to the program are a layout L whose features are to be extracted and maximum line spacing, S_{max}. The program outputs a table for vulnerable areas and the number of new features (#TLa/b, #TTa, #TTb, #PTT).

Algorithm 1: Layout extraction flow

Input: The maximum line spacing S_{max} and a layout L
Output: Tables of vulnerable areas (VulnerableAreaTable) and new features (TLab, TTa, TTb, PTT)

```
for each metal layer m do
  LineData (m) ← ReadLineSegments (L);  // BucketSort
  TTa (m) ← 0;  TTb (m) ← 0;  PTT (m) ← 0;  TLab (m) ← 0;
  c ← 1;
  n ← 2;
  while c<N_line do  // N_line: # lines in LineData
    L1 ← LineData (m,c);  // c-th line
    L2 ← LineData (m,n);  // n-th line
    PTT (m) += CheckPTT (L1, L2);  // check PTT between L1 and L2
    TTa (m) += CheckTTa (L1, L2);  // check TTa between L1 and L2
    TTb (m) += CheckTTb (L1, L2);  // check TTb between L1 and L2
    TLab (m) += CheckTLab (L1, L2);  // check TLab between L1 and L2
    if Spacing (L1, L2)<=S_max then
      VulnerableAreaTable (m) ← VulnerableArea (L1, L2);
      LineData (m) ←Split (L1, L2);
      Adjust (N_line, c, n);
    else
      c ← c+1;
      n ← n+1;
    end
  end
end
```

All layouts of a layer have a preferred orientation of the wires. Let's assume that the preferred orientation is along the x-axis. From the given layout, we read lines for each metal layer and sort all the lines in the ascending order of the y-coordinate of the bottom-left corner of the lines (x-coordinate is used for tie-breaker). Since there exists numerous line segments (e.g., several million segments in a metal layer), we use a Bucket Sort algorithm to speed up the sorting process.

After sorting all geometries, we process them one by one. Let the current feature at the top of the list be S_1. We first check for TTa by looking at the spacing to the next geometry in the list. Then, we check the distance to the next feature (S_2) in the y-direction. If there is any feature within the minimum distance, we check if it contains geometries PPT, TLa/b, or TTb. Then, we determine the vulnerable area between S_1 and S_2. If there is more than one linespace between S_1 and S_2, then spilt S_1 into two sub line segments and insert them into the data structure. We extract the corresponding vulnerable length, linespace pairs. We then delete the feature at the top of the list, and move to the next feature.

Fig. 10 shows an example in which four line segments, S_1, S_2, S_3, and S_4, exist. For S_1 and S_2, we check PTT, TTa, TTb, and TLa/b relations and PTT is extracted as shown in Fig. 10(b). Then, we extract vulnerable area between S_1 and S_2 in Fig. 10(c). Since there exists a vulnerable area, we extract it and split S_1 into two segments by removing the overlapped area from S_1 in Fig. 10(d). We then check PTT, TTa, TTb, and TLa/b relations for S_{1_1} and S_2. Although there exists a TTb relation between S_{1_1} and S_2 as shown in Fig. 10(e), we do not add it to TTb because the left side of S_{1_1} was generated during the split operation. On the other hand, the right side of S_{1_1} is the right side of the original line S_1, so there exists a TTb

relation between S_{1_1} and S_3 as shown in Fig. 10(f). Then, we proceed to the next line S_2 and find a TLa/b relation between S_2 and S_4 as shown in Fig. 10(g). We also find a TTa relation between S_2 and S_3 in Fig. 10(h).

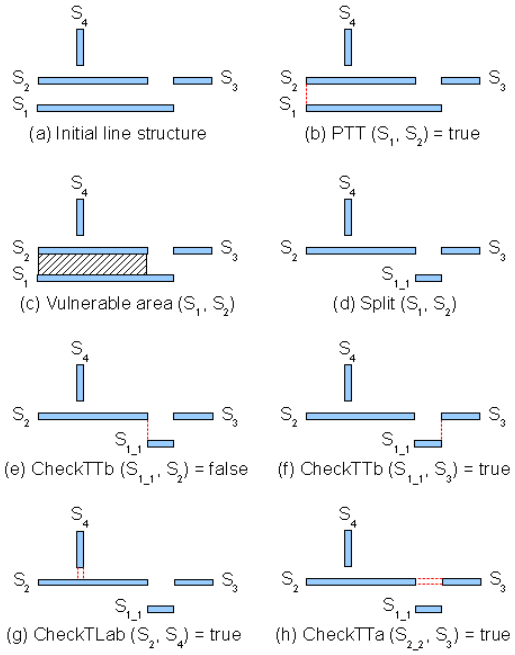

Fig .10. Extraction of vulnerable area and the new features. (a) Initial line structure, (b) PTT is extracted from S1 and S2, (c) Vulnerable area between S1 and S2 is extracted, (d) Postprocess after vulnerable area extraction, (e) TTb does not exist between S1_1 and S2, (f) TTb is extracted from S1_1 and S3, (g) TLa/b is extracted from S2 and S4, (h) TTa is extracted from S2 and S3.

VI. IMPACT ON CIRCUIT LIFETIME

A. *Results Incorporating Irregular Geometries*

We have compared the lifetime considering only area vs. each irregular geometry in Fig. 5 for Metal1-Metal5 for the circuit used in the study. The $\sqrt{E}$ model is used to take into account the difference in design rules for each of the layers, as noted in Table 1, i.e. *m=1/2* in (2). The results are shown in Fig. 11.

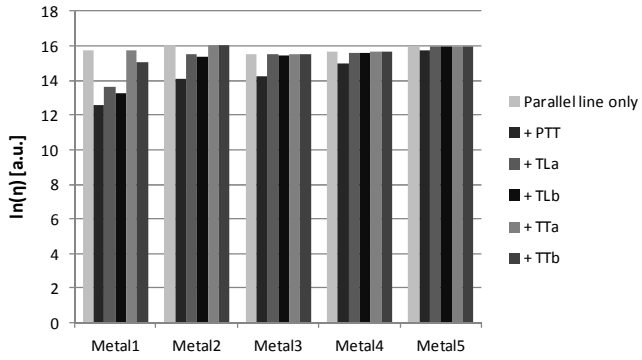

Fig. 11. Characteristic lifetime for individual layers of a fast fourier transform circuit considering only the dielectric between parallel lines and considering also the dielectric between irregular geometries.

We have also compared the lifetime considering only area vs. each of the irregular geometries in Fig. 5. Fig. 12. compares lifetimes of individual layers with and without the inclusion of degradation in lifetime due to PTT, TLa/b, TTa, and TTb for the layout of the circuit.

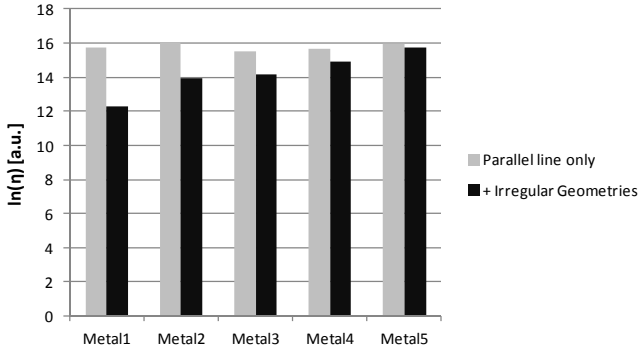

Fig. 12. Reliability for individual layers of a fast fourier transform circuit considering only the dielectric between parallel lines (gray) and considering also the dielectric between perpendicular lines (black).

B. *Observations*

Fig. 11 and Fig.12 shows that irregular features cause a negligible difference for Metal 5 and the biggest difference for Metal 1. Also, From Fig. 11, it can be seen that taking into account the PTT geometry impacts the lifetime of Metal 1 significantly, in comparison with considering only the area between parallel metal lines.

From Fig. 12, we can clearly find that the difference between the lifetime calculated by considering only the dielectric between parallel lines and the lifetime when considering also the dielectric of perpendicular lines decreases gradually from Metal 1 to Metal 5 of the circuit. This is because the number of irregular geometries decreases from Metal 1 to Metal 5, because of routing restrictions associated with higher layers of the circuit. Thus, from the result, we can clearly find that the irregular geometries do cause a significant impact on circuit lifetime and reliability, but mostly for lower layers of metal.

Fig. 11 shows that the worst lifetime from Metal 1 to Metal 5 occurs when we consider the dielectric impacted by the PTT geometry and the dielectric between parallel lines. This is because there are numerous PTT type geometries on Metal 1 and above. On the other hand, TTb type geometries rarely (or never) occur above Metal 1, and there is a neglibible impact of these geometries. TLa/b geometries essentially consist of two perpendicular wires. In general, each metal layer has a preferred routing direction, either horizontal or vertical. Perpendicular wires are usually not allowed for global routing. Therefore, TLa/b-type vulnerable areas above Metal 1 are rare. However, our layout extractor showed that TLa/b was frequently found on Metal 1, since Metal 1 is used in cell libraries for internal wiring.

VII. CONCLUSION

In this work, the impact of line ends in backend dielectric TDDB was studied and found to be clearly significant. These irregular geometries can potentially impact chip lifetime and need to be separately extracted and included in a backend dielectric chip reliability simulator.

This study integrates field enhancement into the TDDB chip lifetime simulator. It's also a step towards our goal of developing a tool to help designers predict failure rates of chips as a function of layout style.

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