Block-level Designs of Die-to-Wafer Bonded 3D ICs and Their Design Quality Tradeoffs

Krit Athikulwongse[§†], Dae Hyun Kim[§‡], Moongon Jung[§], and Sung Kyu Lim[§]
[§]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA
[†]National Electronics and Computer Technology Center, Khlong Luang, Pathum Thani, Thailand
[‡]Cadence Design Systems, San Jose, California, USA
e-mail: krit@gatech.edu, daehyun@gatech.edu, moongon@gatech.edu, limsk@ece.gatech.edu

Abstract— In 3D ICs, block-level designs provide various advantages over designs done at other granularity such as gate-level because they promote the reuse of IP blocks. In this paper, we study block-level 3D-IC designs, where the footprint of the dies in the stack are different. This happens in case of die-to-wafer bonding, which is more popular choice for near-term low-cost 3D designs. We study design quality tradeoffs among three different ways to place through-silicon vias (TSVs): TSV-farm, TSV-distributed, and TSV-whitespace. In our holistic approach, we use wirelength, power, performance, temperature, and mechanical stress metrics to conduct comprehensive comparative studies on the three design styles. In addition, we provide analysis on the impact of TSV size and pitch on the design quality of these three styles.

I. Introduction

Three-dimensional integrated circuits (3D ICs) are built in various design styles and at different levels. Wide-I/O memory technology provides extremely high memory bandwidth and very short core-to-memory connections [1]. Homogeneous 3D integration technology provides compact and high-degree of logic integration [2]. On the other hand, heterogeneous integration technology allows various electronic components such as analog circuits, memory elements, logic, and sensors in the same 3D-IC stack [3].

In many cases, 3D die stacking is done for the dies that have the identical footprint. The main motivation behind this is to allow wafer-to-wafer bonding, which in turn reduces the cost compared with other alternatives such as die-to-wafer and die-to-die bonding. However, there are several cases where die-to-wafer bonding is more practical and low cost. For example, in case of a two-tier memory+logic stacking [4], it is very possible for these two dies to be built by different companies and thus have different footprint. In this case, wafer-to-wafer bonding is simply not possible, which makes die-to-wafer bonding the only practical choice. The wafer will have larger dies, and the smaller dies will be aligned and bonded to the wafer individually. The same argument applies to logic-to-logic stacking, where the two dies are from different companies. It is also possible that designers use IP blocks that may enforce them to use different footprint between the two dies.

In this paper, we study how to design block-level 3D ICs, where the footprint of the dies in the stack are different. Among several possible configurations, we focus on a two-tier 3D IC, where the bottom die has a larger footprint. Both dies are facing down so that the heat sink is located above the back-side (= bulk) of the top die, and C4 bumps are below the front-side (= top metal layer) of the bottom die.[1] We further assume that the design of the top die is fixed so that we focus on the block-level design of the bottom die. Depending on the location of through-silicon vias (TSVs) in the bottom die, a redistribution layer (RDL) is necessary on the back-side of the bottom tier to connect the two dies as shown in Fig. 1.

[1]This stacking allows better power delivery and potentially better cooling if the top die consumes more power.

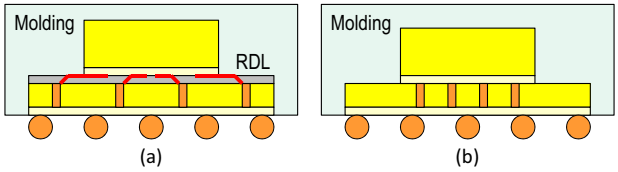

Fig. 1. Side view of a 3D IC (a) with RDLs and (b) without RDLs.

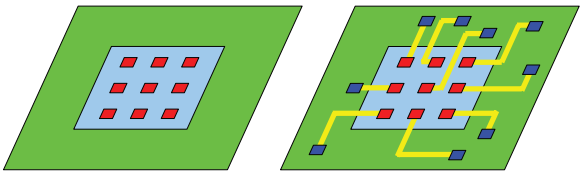

Fig. 2. RDL wires connecting TSVs on bottom die to bonding pads on top die.

In this work, three different ways to place TSVs in the bottom die, namely TSV-farm, TSV-distributed, and TSV-whitespace, are investigated. Since each design style has its own advantages and disadvantages, these three design styles are compared in terms of area, wirelength, timing, power, temperature, and mechanical stress. In addition, the TSV size and pitch are varied to investigate their impact on each design style. To the best of our knowledge, this is the first work that addresses these issues in practical 3D IC designs.

II. Preliminaries

A. Die Bonding and Redistribution Layers

For die-to-wafer bonding in 3D ICs, three methods have been proposed: back-to-back, face-to-back, and face-to-face. If back-to-back bonding is utilized, a signal should go through two TSVs when it is transmitted from one die to its adjacent die. Since TSVs have nonnegligible capacitance, transferring a signal through two TSVs might degrade the delay and the signal integrity of the net. On the other hand, both the face-to-back and the face-to-face bonding methods enable less TSV capacitance overhead than the back-to-back bonding. In addition, since metal layers can be deposited on the back side of silicon dies, they also enable the flip chip packaging for 3D ICs. The face-to-face and the face-to-back bonding methods also help reduce temperature because a heat sink can be mounted on the back side of the top die.

When the face-to-face bonding is utilized between two dies with different die sizes, I/Os must be positioned on exposed top layer of the metal on the large die. In this case, TSVs would not be needed. Wire-bonded packaging is usually utilized to connect the I/Os to the package pins. This kind of stacking, however, is not compatible with popular flip-chip packaging.

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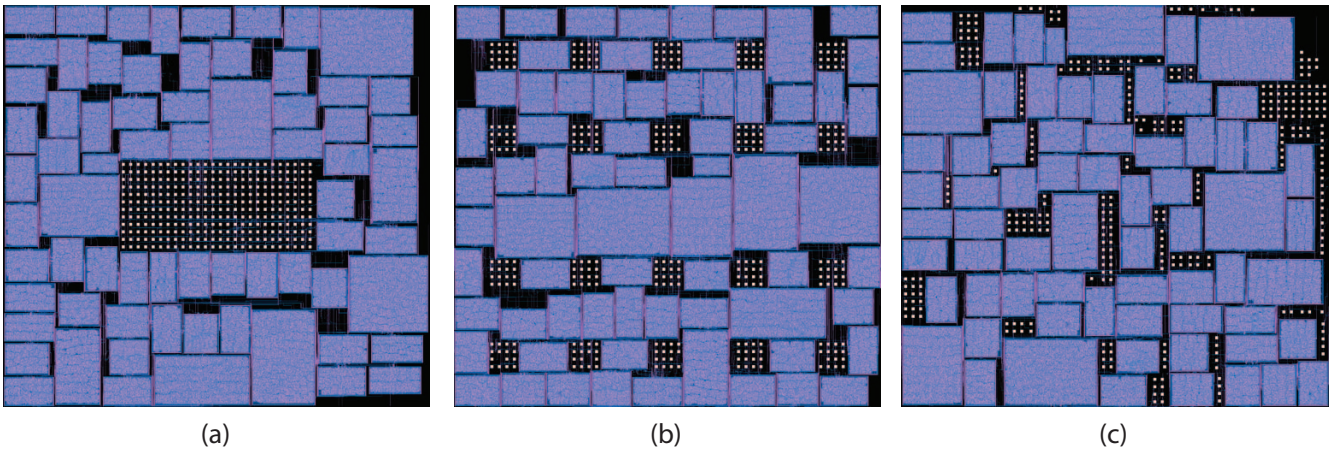

Fig. 3. Layout of bottom die of the circuit in (a) TSV-farm, (b) TSV-distributed, and (c) TSV-whitespace styles. TSVs are in white.

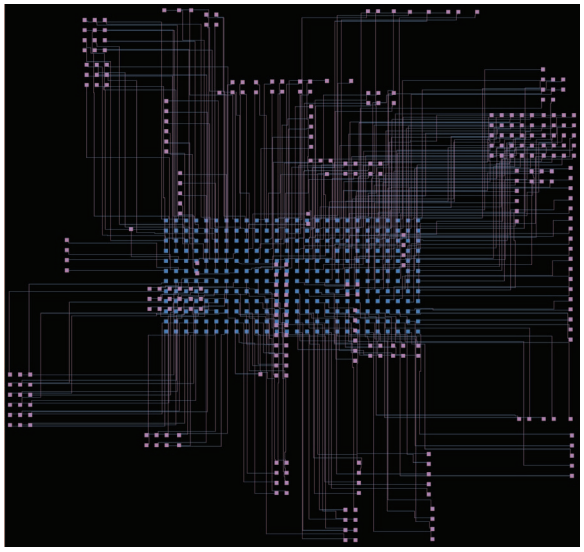

Fig. 4. RDL routing in TSV-whitespace style.

When the face-to-back bonding is utilized between two dies with different die sizes, redistribution-layer (RDL) routing on the back side of the bottom die is required in some cases. If all TSVs inserted in the bottom die are inside the footprint area of the top die as shown in Fig. 2(a), the TSVs in the bottom die can be directly bonded to the bonding pads in the top die. However, if some TSVs in the bottom die are outside the footprint area of the top die, RDL routing is necessary to connect the TSVs to the bonding pads of the top die as illustrated in Fig. 2(b).

Although the RDL allows connections between TSV landing pads on the back side of the bottom die and the bonding pads in the top die, it causes several negative effects. First of all, typical wires on the RDL are wide, possibly as wide as wires on the topmost metal layers. Thus, their parasitic capacitance is much higher than local metal wires, and causes timing degradation and dynamic power overhead. In addition, the large minimum pitch between adjacent wires in the RDL limits the minimum TSV pitch in a TSV array. For example, if four TSVs are placed in a 2×2 array, they can be placed as close to each other as possible. However, if 25 TSVs are placed in a 5×5 array, the TSV in the center cannot be routed by an escape routing unless the TSV pitch is several times greater than the minimum pitch.

B. The Goal of This Work

According to the above discussion, two options are available for the design of 3D ICs with different die sizes: insert all TSVs inside the footprint area of the top die so that RDL routing is not required, or insert TSVs wherever they are needed and perform RDL routing to connect them in the bottom die to the bonding pads in the top die. The former limits TSV locations, but it does not require RDL wires. The latter provides higher degree of freedom on TSV locations than the former option, but it requires RDL wires and routing. In addition, different TSV insertion styles lead to very different layout qualities. In this work, therefore, three different design styles: TSV-farm (without RDLs), TSV-distributed (with RDLs and regularly placed TSVs), and TSV-whitespace (with RDLs and irregularly placed TSVs), are compared. Since each design style has its own advantages and disadvantages, we used as many design metrics as possible so that the three design styles can be investigated in many different point of views. Two important design parameters, i.e., TSV diameter and pitch, impact the quality of each design. Therefore, these parameters are also varied, and their impact on various performance metrics is studied.

Since the 3D-IC design space is too large, the scope of this work is restricted to the following assumptions. Two dies are stacked, and face-to-back bonding is used between the two dies. Since placing the larger die of the two in the bottom of the 3D stack provides more benefits than the opposite case[2], the bottom die is also assumed to be larger than the top die. A heat sink is mounted on the back side of the top die.

III. Block-Level 3D-IC Design

In this section, the block-level design styles (TSV-farm, TSV-distributed, and TSV-whitespace) are explained in detail. These three design styles are distinguished by how TSVs are distributed in the layout. In the TSV-farm style, TSVs are placed inside the footprint area of the top die. In the TSV-distributed style, TSVs are evenly distributed over the layout. In the TSV-whitespace style, TSVs are irregularly inserted.

A. Partitioning

In the first stage of all design styles, blocks are partitioned into two dies by a partitioner. During partitioning, various factors should be

[2]For example, the bottom die is connected to the package, so large bottom die area allows the chip to have more I/Os for power and ground.

taken into account to control the quality of the 3D IC. The cut size, which is the number of cut 3D nets between the two dies, directly determines the number of TSVs. In addition, assigning low-power blocks to the bottom die and high-power blocks to the top die reduces temperature because the top die is closer to the heat sink than the bottom die. On the other hand, assigning thermally-sensitive blocks such as memory blocks to the top die and thermally-insensitive blocks to the bottom die increases predictability and reliability of the 3D IC. Because of these design factors, blocks are not moved across dies after partitioning. Partitioning are manually performed with all these factors considered.

B. TSV Insertion and Floorplanning

In the TSV-farm and the TSV-distributed styles, TSVs are preplaced in an array and treated as obstacles during floorplanning. In the TSV-farm style, an array of TSVs (and bonding pads) are placed in the middle of the bottom die (and top die). In the TSV-distributed style, on the other hand, TSVs are placed all over the bottom die. Therfore, some of the TSVs exist outside the footprint area of the top die.

After preplacing TSVs, floorplanning of the blocks in the bottom die is manually performed. Since functional blocks and TSVs should not overlap, blocks are placed around the TSV farm in the TSV-farm style. Since the TSV farm area is usually large, if all blocks are highly connected, the TSV-farm design style causes significant wirelength overhead. On the other hand, if the interblock connectivity is not high, the farm in the center of the layout does not cause wirelength overhead. The TSV-distributed style might not cause significant wirelength overhead because, unlike one large TSV array in TSV-farm style, TSVs are grouped in small arrays in TSV-distributed style. However, some large blocks have very limited locations for their positions because they cannot be placed in the space between adjacent TSV arrays. This design constraint might degrade wirelength, timing, and power. However, the TSV-distributed style is expected to show low temperature and small TSV stress.

On the other hand, a 3D floorplanner is used to obtain 3D-IC layouts of the TSV-whitespace style. After floorplanning, TSVs are manually inserted into whitespace existing between blocks close to a pin of each 3D net. Therefore, TSVs are irregularly placed. When TSVs are inserted, the current floorplan is perturbed by moving blocks to create or expand whitespace. Since a 3D floorplanner is used, the TSV-whitespace design style is expected to optimize the wirelength better than all other design styles.

C. Bonding Pad Assignment and RDL Routing

In the TSV-farm style, all TSVs exist inside the footprint of the top die. Therefore, the locations of the bonding pads in the top die are duplicated from the locations of the TSVs in the bottom die. In the TSV-distributed and the TSV-whitespace styles, the locations of the bonding pads in the top die are determined by recursive bipartitioning before floorplanning of the top die. The recursive bipartitioning increases the routability of the RDL routing. After the bonding pad assignment in the top die, the blocks in the top die are floorplanned. The primary objective at this point is to minimize the wirelength. After floorplanning of the top die, RDL routing is performed in the TSV-distributed and the TSV-whitespace styles.

IV. Design Evaluation

In this section, a brief overview of the methodology to evaluate 3D-IC layouts is presented. Traditional metrics and reliability metrics are reported in this work. The traditional metrics are area, wirelength, timing, and power, and the reliability metrics are temperature and mechanical stress.

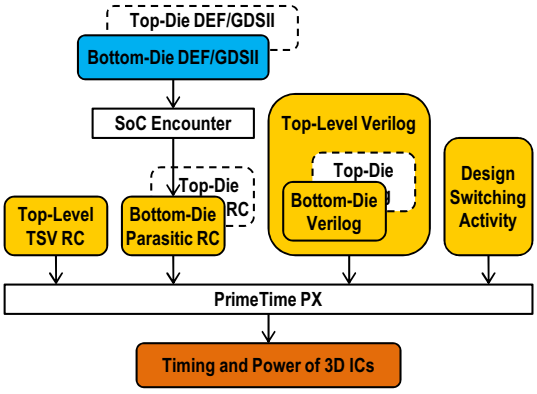

Fig. 5. Timing and power analysis flow for die-to-wafer stacked 3D ICs.

A. Traditional Metrics

Traditional metrics such as area and wirelength are important for both 2D ICs and 3D ICs. These traditional metrics are obtained directly from layouts of both bottom and top dies.

Timing (longest path delay) and power analysis flow is shown in Fig. 5. It is performed as follows. First, the parasitic resistance and capacitance of each die are extracted using Cadence QRC Extraction. Since the face-to-back die bonding style and 30-μm thick bottom die are assumed, the capacitive coupling between the bottom and the top dies are not included in resistance and capacitance extraction. Therefore, parasitic resistance and capacitance extraction of each die is performed separately. Parasitic resistance and capacitance of the RDL is also extracted. For 3D timing analysis, the top and the bottom dies are represented as modules in a top-level verilog file. A top-level SPEF file is also created. It includes not only the parasitic resistance and capacitance of both dies, but also resistance and capacitance of TSVs and the RDL wires. For accurate power analysis, switching activity of all logic cells is obtained by functional simulation of the whole chip. Synopsys PrimeTime is used to perform static timing and power analysis.

B. Thermal Analysis

The thermal analysis flow used in this work is shown in Fig. 6. For thermal analysis, Ansys FLUENT is used. To perform thermal analysis, first, a meshed structure is created. Each grid, which is called a thermal cell, in the meshed structure contains material composition information such as copper density in the cell. This information is extracted from GDSII layout files which include logic cells in the blocks as well as TSVs. These files together with power dissipation of each logic cell in the blocks are presented to the layout analyzer. The layout analyzer automatically generates a meshed structure and layout information of each thermal cell from its inputs. The layout information of a thermal cell consists of total power dissipated in the cell and thermal conductivity computed from the components inside the cell such as polysilicon used for transistor gates, tungsten used for vias, copper used for TSVs, and dielectric material. With a sufficiently fine thermal cell size, equivalent thermal conductivity can be computed based on thermal resistive model [5].

C. Mechanical Stress Analysis

The mechanical stress of a layout is analyzed using the stress analyzer obtained from [6]. Inputs to the analyzer are die size, TSV

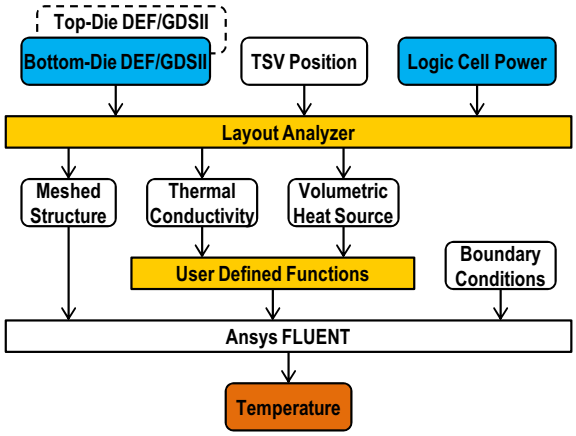

Fig. 6. GDSII layout-level thermal analysis flow.

TABLE I
CHARACTERISTICS OF THE TEST CIRCUIT (RECONFIGURABLE COMPUTING ARRAY) AND BASELINE DESIGN.

Total #gates	1,363,536	Total #blocks	95
#Interblock nets	1,853	#Blocks on top die	26
#TSVs	312	#Blocks on bottom die	69

diameter, TSV locations, simulation grid density, and precomputed data of TSV stress tensor. The analyzer outputs a von Mises stress map, which is a widely used mechanical reliability metric. Computation of stress at a point affected by multiple TSVs is based on the principle of linear superposition of stress tensors. With stress tensors obtained from finite element analysis (FEA) using an FEA tool ABAQUS, a full-chip stress analysis can be performed.

V. EXPERIMENTAL RESULTS

For the experiments, 45-nm technology [7] is used. An open-source hardware IP core [8] is synthesized using an open cell library [9]. The thickness of bottom die and top die is 30 μm and 530 μm, respectively. High-thermal-conductivity molding compound [10] is assumed.

A. Baseline Designs

Layouts of the circuit in the three different styles are first designed and compared. The characteristics of the test circuit and its baseline designs are listed in Table I. The number of TSVs depends on the partitioning of blocks and area ratio of the two dies. In this work, we use the same partitioning, thus same number of TSVs, in all the three styles for fair comparison. The TSV size is 10 μm, and TSV pitch is 30 μm. The parasitic capacitance and resistance are 50 fF and 50 mΩ, respectively. RDL wire width and spacing of 0.4 μm is used in the experiments. The layout of bottom die of the circuit in TSV-farm, TSV-distributed, and TSV-whitespace styles is shown in Fig. 3. The RDL routing of the circuit in TSV-distributed and TSV-whitespace styles is shown in Fig. 4.

1) Area, Footprint, and Wirelength: The area, footprint, and block-to-block (B2B) and RDL wirelength of layout in the three styles are shown in Table II. We use the same area and footprint for all the three styles. Design in TSV-farm style has the shortest wirelength because all the TSVs occupy only one area in the middle of the bottom die, confining the obstruction of optimal block placement in small area. Design in TSV-distributed style has the longest block-to-block wirelength (27 % longer than TSV-farm) because the TSV arrays distributed all over the bottom die obstruct optimal block placement. Design in TSV-whitespace style has little longer wirelength (2 %) than design in TSV-farm style because we start from optimal block placement, and move blocks only when it is necessary to insert TSVs in some position without whitespace nearby. Most TSVs are inserted in the original whitespace, and do not interfere with placement of the blocks much. In addition, the design in TSV-distributed and TSV-whitespace styles require RDL routing as shown in Fig. 4.

TABLE III
COMPARISON OF POWER AND TEMPERATURE OF DIFFERENT LAYOUTS. TSV-F, TSV-D, AND TSV-W ARE TSV-FARM, TSV-DISTRIBUTED, AND TSV-WHITESPACE, RESPECTIVELY. THE NUMBERS IN PARENTHESIS AFTER DESIGN STYLE ARE TSV SIZE AND PITCH IN μM.

Design style	P_{total} (mW)		T_{max} (°C)	T_{min} (°C)	T_{ave} (°C)
TSV-f (10,30)	1,183	(100.00 %)	76.87	38.04	47.56
TSV-d (10,30)	1,107	(-6.40 %)	62.43	39.15	46.28
TSV-w (10,30)	1,065	(-9.99 %)	77.04	38.65	46.19
TSV-f (5,30)	1,199	(+1.41 %)	77.55	38.29	47.88
TSV-d (5,30)	1,114	(-5.86 %)	62.53	39.22	46.45
TSV-w (5,30)	1,104	(-6.67 %)	78.71	39.20	46.94
TSV-f (5,15)	1,210	(+2.28 %)	74.85	41.33	48.47
TSV-d (5,15)	1,117	(-5.60 %)	59.17	39.81	47.46
TSV-w (5,15)	1,103	(-6.75 %)	79.26	39.76	48.10

2) Longest Path Delay and Buffers: The longest path delay (LPD) without and with timing optimization are also shown in Table II. The timing optimization proposed in [11] is used with the target delay of 1.25 ns. Without timing optimization, none of the designs meets the target delay; however, the design in TSV-farm style has the shortest delay. With timing optimization, all designs are closer to meet the target delay, and the delay of the design in TSV-farm style is still the shortest. The delay of the design in TSV-distributed and TSV-whitespace styles is longer than the delay of the design in TSV-farm style 10 % and 15 %, respectively. Because of long wirelength, it is hard to optimize the design in both TSV-distributed and TSV-whitespace styles to meet timing. In addition, no buffer can be added along the RDL routing because the routing is on the backside of the bottom die. The number of buffers inserted during timing optimization is also shown in Table II. The design in TSV-farm style uses the smallest number of buffers. Because of long wirelength, the design in TSV-distributed and TSV-whitespace styles uses 10 % and 27 % more buffers than the design in TSV-farm style.

3) Power and Temperature: Power analysis is performed. The total power at maximum speed of each design is shown in Table III. The design in TSV-distributed and TSV-whitespace styles consumes 6 % and 10 % less power than the design in TSV-farm style not because they are efficient design, but because they can only operate at slower speed than the design in TSV-farm style as discussed earlier.

Thermal analysis is performed at the maximum speed of each design. The maximum, minimum, and average temperatures are shown in Table III. Although the minimum and average temperature across all the three designs are about the same, the maximum temperature of the three designs is different. The design in TSV-distributed style has the lowest maximum temperature not actually because it consumes low power, resulted from relatively low speed, but primarily because TSVs distributed all over the bottom die help conduct heat to heat sink. Design in TSV-farm style has high maximum temperature because TSVs in the center of the bottom die cannot help conduct heat from high-power blocks far from them. The design in TSV-whitespace styles also has high maximum temperature although it consumes the least power because of the same reason.

The thermal profile of bottom dies of the circuit in TSV-farm, TSV-distributed, and TSV-whitespace styles at the maximum speed

TABLE II
COMPARISON OF AREA, FOOTPRINT, WIRELENGTH, LONGEST PATH DELAY (LPD) WITHOUT AND WITH OPTIMIZATION, AND NUMBER OF BUFFERS IN DIFFERENT LAYOUTS. TSV-F, TSV-D, AND TSV-W ARE TSV-FARM, TSV-DISTRIBUTED, AND TSV-WHITESPACE, RESPECTIVELY. THE NUMBERS IN PARENTHESIS AFTER DESIGN STYLE ARE TSV SIZE AND PITCH IN μM.

Design style	Area (mm^2)		Footprint (mm^2)		Wirelength (m)			LPD (ns)			# Buffers	
					B2B		RDL	w/o	w/ opt.			
TSV-f (10,30)	3.979	(100.00 %)	2.766	(100.00 %)	1.447	(100.00 %)	-	3.136	1.293	(100.00 %)	3,459	(100.00 %)
TSV-d (10,30)	3.979	(+0.00 %)	2.766	(+0.00 %)	1.842	(+27.30 %)	0.170	4.252	1.425	(+10.20 %)	4,386	(+26.80 %)
TSV-w (10,30)	3.979	(+0.00 %)	2.766	(+0.00 %)	1.483	(+2.46 %)	0.176	4.568	1.492	(+15.38 %)	3,798	(+9.80 %)
TSV-f (5,30)	3.979	(+0.00 %)	2.766	(+0.00 %)	1.450	(+0.23 %)	-	2.920	1.269	(-1.87 %)	3,462	(+0.09 %)
TSV-d (5,30)	3.979	(+0.00 %)	2.766	(+0.00 %)	1.814	(+25.32 %)	0.172	4.045	1.411	(+9.16 %)	4,288	(+23.97 %)
TSV-w (5,30)	3.979	(+0.00 %)	2.766	(+0.00 %)	1.475	(+1.91 %)	0.178	4.636	1.420	(+9.79 %)	3,709	(+7.23 %)
TSV-f (5,15)	3.699	(-7.03 %)	2.487	(-10.11 %)	1.482	(+2.39 %)	-	2.792	1.256	(-2.86 %)	3,545	(+2.49 %)
TSV-d (5,15)	3.699	(-7.03 %)	2.487	(-10.11 %)	1.741	(+20.31 %)	0.210	3.762	1.404	(+8.61 %)	4,081	(+17.98 %)
TSV-w (5,15)	3.699	(-7.03 %)	2.487	(-10.11 %)	1.471	(+1.62 %)	0.164	3.872	1.422	(+10.01 %)	3,887	(+12.37 %)

TABLE IV
COMPARISON OF STRESS OF DIFFERENT LAYOUTS.

Design style	$\sigma_{\max}$ (MPa)		$\sigma_{\text{ave},\sigma>10}$ (MPa)		Area$_{\sigma>10}$ (mm^2)	
TSV-f (10,30)	676.78	(100.0 %)	150.20	(100.0 %)	0.353	(100.00 %)
TSV-d (10,30)	691.29	(+2.1 %)	97.73	(-34.9 %)	0.598	(+69.7 %)
TSV-w (10,30)	688.99	(+1.8 %)	88.95	(-40.8 %)	0.695	(+97.2 %)
TSV-f (5,30)	629.97	(-6.9 %)	72.08	(-52.0 %)	0.276	(-21.8 %)
TSV-d (5,30)	629.97	(-6.9 %)	67.89	(-54.8 %)	0.294	(-16.6 %)
TSV-w (5,30)	629.97	(-6.9 %)	64.65	(-57.0 %)	0.310	(-12.0 %)
TSV-f (5,15)	643.76	(-4.9 %)	150.94	(+0.5 %)	0.087	(-75.3 %)
TSV-d (5,15)	654.71	(-3.3 %)	101.12	(-32.7 %)	0.143	(-59.4 %)
TSV-w (5,15)	657.18	(-2.9 %)	85.21	(-43.3 %)	0.183	(-48.2 %)

of each design is shown in Fig. 7. TSVs help reduce temperature. Local cool spots on bottom dies correspond to TSV arrays. Among 3D designs, design in TSV-distributed style has the lowest maximum temperature because TSVs are distributed across the bottom die. Design in TSV-whitespace style has the highest temperature because high-power blocks can be far from TSVs.

4) Mechanical Stress: Mechanical stress analysis is performed. The maximum and average stresses are shown in Table IV. The area with stress higher than 10 MPa is also shown in the table. Despite high TSV density, TSV-farm style has the lowest maximum stress among the designs. TSVs in this style are in complete rows and columns. Because stress interference on a TSV coming from horizontal and vertical directions has opposite impacts, their effect partially cancels each other [12]. The average stresses above the 10-MPa threshold on the bottom die shows the opposite trend. The design in TSV-farm style has the highest average stress. When TSVs are close to each other (relative to TSV size), the impact of interference from neighboring TSVs becomes noticeable. The trend of the area above the threshold is completely opposite to the trend of average stress. The design in TSV-whitespace has the widest area of stress above the threshold, and the design in TSV-farm style has the narrowest area of stress above the threshold. When TSVs are grouped in small area, stress increases because of interference from neighboring TSVs, but the impacted area decreases. The stress profile of the design in three different styles is shown in Fig. 8.

B. Impact of TSV Size

In this experiment, the size of TSVs is reduced to 5 μm. The parasitic capacitance and resistance are updated to 25 fF and 200 mΩ, respectively. We keep the same die area and footprint as shown in Table II. The block-to-block wirelength and RDL wirelength are not much different from the baseline designs as shown in the table. The decrease in TSV capacitance improves timing slightly. As shown in Table II, the longest path delay (LPD) without and with timing optimization decreases a little from the baseline designs. The design in TSV-farm style still has the shortest delay both without and with timing optimization. The longest path delay of the designs with 5-μm TSV is 2 % to 6 % shorter than the longest path delay of the designs with 10-μm TSV. As also shown in Table II, the number of buffers inserted during timing optimization decreases a little because of the decrease in TSV capacitance.

As shown in Table III, the total power at maximum speed of each design increases a little from the baseline designs because of the decrease in longest path delay. The maximum, minimum, and average temperatures at the maximum speed of each design are shown in Table III. The temperature increases a little because of the decrease of TSV size, thus decrease in thermal conductivity to heat sink, and the increase in power, resulted from the decrease in longest path delay. The design in TSV-distributed style still has the lowest maximum temperature.

The maximum and average stresses are different from the baseline designs as shown in Table IV. With decrease in TSV size, the stress decreases. The region affected by stress from each TSV shrinks, and stops overlapping each other, decreasing stress further. Because the TSV size, compared to TSV spacing, is now small, stress from TSVs is almost isolated from each other, resulting in the same maximum stress across all design styles. The average stresses above 10-MPa threshold is noticeably lower than that of the baseline designs, and are not much different across all the designs. Because of the decrease in TSV size, the area with stress higher than the threshold on the bottom die decreases dramatically from the baseline designs.

C. Impact of TSV Pitch

After reducing TSV size, the mechanical stress decreases, leading to an opportunity to place TSVs closer to each other. In this experiment, the pitch of TSVs is changed to 15 μm. The area and footprint decrease by 7 % and 10 %, respectively. As a result, wirelength decreases a little. However, the RDL wirelength for the design in TSV-distributed style increases because the bonding pad on the top die are moved closer to the center of the die.

The decrease in wirelength also affects timing noticeably. As shown in Table II, the longest path delay (LPD) without and with timing optimization decreases further. The design in TSV-farm style still has the shortest delay both without and with timing optimization. It almost meets the target delay now after optimization.

As shown in Table III, the total power at maximum speed of each design increases because of the decrease in longest path delay. The maximum, minimum, and average temperatures at the maximum speed of each design are shown in Table III. The minimum and average temperature increase because of the decrease in footprint area, thus increase in power density, and the increase in power, resulted from the increase in speed. The design in TSV-distributed style still has the lowest maximum temperature.

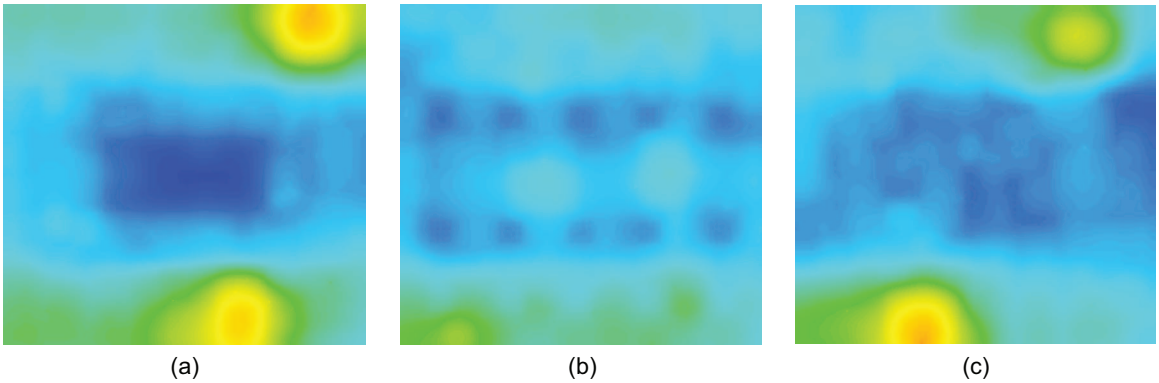

Fig. 7. Temperature of bottom die of the circuit in (a) TSV-farm, (b) TSV-distributed, and (c) TSV-whitespace styles.

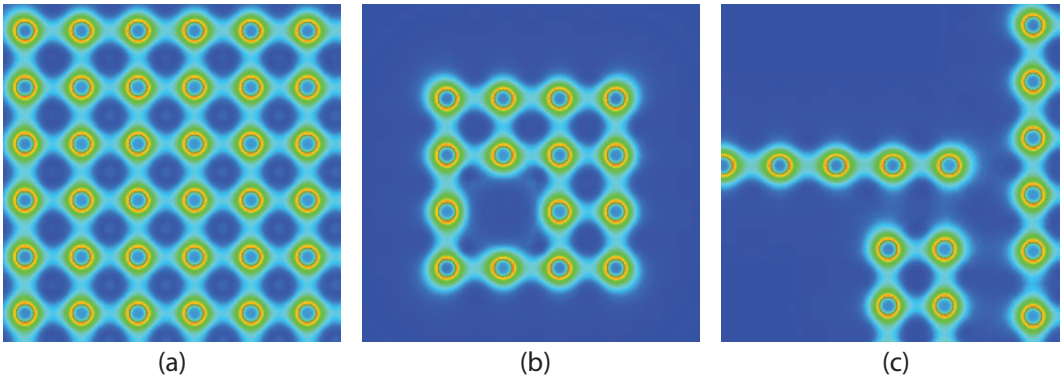

Fig. 8. Stress of bottom die of the circuit with 10-μm TSVs in (a) TSV-farm, (b) TSV-distributed, and (c) TSV-whitespace styles.

The maximum and average stresses increase as shown in Table IV. Because of decreasing TSV pitch, stress from each TSV starts overlapping each other again. The maximum stress of each design styles is still lower than that of the baseline designs with 10-μm TSV. The average stress above 10-MPa threshold on the bottom die increases to the same level as that of the baseline designs because of the same relative size of TSV to the pitch. The area with stress above the threshold on the bottom die decreases dramatically from the designs with 30-μm TSV pitch because TSVs are placed closer to each other.

VI. Conclusions

In this work, we investigate 3D-IC designs with different die sizes in the IC stack. We design layouts of a circuit at block level in various styles, and study the tradeoffs of the design styles on the area, footprint, timing, power, temperature, and mechanical stress. Because of the lack of RDL wiring, TSV-farm style has the best timing. The design in this style has the highest average stress, but the area impacted by stress is smallest. TSV-distributed style has the worst wirelength because TSV arrays interfere with block placement. However, it has the lowest temperature because TSVs distributed across the die help reduce temperature.

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