TSV-Aware Interconnect Distribution Models for Prediction of Delay and Power Consumption of 3-D Stacked ICs

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***Abstract*—3-D integrated circuits (3-D ICs) are expected to have shorter wirelength, better performance, and less power consumption than 2-D ICs. These benefits come from die stacking and use of through-silicon vias (TSVs) fabricated for interconnections across dies. However, the use of TSVs has several negative impacts such as area and capacitance overhead. To predict the quality of 3-D ICs more accurately, TSV-aware 3-D wirelength distribution models considering the negative impacts were developed. In this paper, we apply an optimal buffer insertion algorithm to the TSV-aware 3-D wirelength distribution models and present various prediction results on wirelength, delay, and power consumption of 3-D ICs. We also apply the framework to 2-D and 3-D ICs built with various combinations of process and TSV technologies and predict the quality of today and future 3-D ICs.**

***Index Terms*—3-D IC, interconnect prediction, through-silicon via (TSV), wirelength distribution.**

I. Introduction

THREE-DIMENSIONAL integrated circuits (3-D ICs) have new design parameters such as die-to-die bonding styles, through-silicon-via (TSV) types, TSV size, and the die count to be stacked. Therefore, 3-D ICs have much larger design space than traditional 2-D integrated circuits (2-D ICs), so the need for fast estimation of the quality (area, delay, power, etc.) of 3-D ICs is increasing for early design space exploration. Among various quality estimation methodologies such as system-level modeling and fast prototyping for early-stage design space exploration, using wirelength distribution models is widely and frequently used because the models are simple, fast, sufficiently accurate, and easy to use.

Among several representative wirelength distribution models, Davis' model for 2-D ICs in [3] have been extended to predict the quality of 3-D ICs in many papers [4]–[8]. According to those papers, 3-D ICs have much shorter wirelength, smaller delay, and lower power consumption than 2-D ICs. In addition, stacking more dies can decrease the total wirelength, delay, and power consumption further. However, most of the 3-D wirelength distribution models ignore the impact of TSV insertion, which in fact has significant effects on the quality of 3-D ICs. For example, Fig. 1 shows area overhead caused by TSV insertion, which increases the footprint area and the average distance between two gates. In addition, the number of TSVs also affects the quality of 3-D ICs because the total area occupied by TSVs is actually determined by the area of a TSV multiplied by the TSV count. Therefore, 3-D wirelength distribution models ignoring TSV insertion, especially TSV size and count, overestimate the amount of the benefits of 3-D ICs and do not predict the negative impacts of TSV insertion.

In [1], we derived TSV-aware 3-D wirelength distribution models by extending Davis' model and taking TSV size into account, and in [2], we applied fixed-distance buffer insertion schemes to the models to predict delay distribution and power consumption of 3-D ICs. However, the fixed-distance buffer insertion schemes are not optimal, so the results do not accurately predict the quality of 3-D ICs optimized by optimal buffer insertion algorithms. In this paper, we apply an optimal buffer insertion algorithm to the TSV-aware 3-D wirelength distribution models and predict delay distribution and power consumption of 3-D ICs. We also present the impact of TSV size and the die count on the delay and power consumption of 3-D ICs. Since the quality of 3-D ICs is affected by not only TSV properties such as TSV size and capacitance but also transistor properties such as transistor size and strength, we also study the impact of transistor and TSV scaling on the quality of 3-D ICs.

The rest of this paper is organized as follows. Section II briefly introduces 3-D integration and reviews previous works on the wirelength distribution of 2-D and 3-D ICs. In Section III, we review the TSV-aware 3-D wirelength distribution models presented in [1], validate the models, and present a few important prediction results. In Section IV, we predict delay distribution and power consumption of 3-D ICs using our models with dynamic-programming-based optimal buffer insertion. In Section V, we study the impact of transistor (from 130 to 11 nm) and TSV (from 5 um-width TSVs to 0.1 um-width TSVs) scaling on the quality of 3-D ICs and cross-compare the 2-D and 3-D ICs built by various combinations of 2-D and 3-D technologies. Then, we discuss

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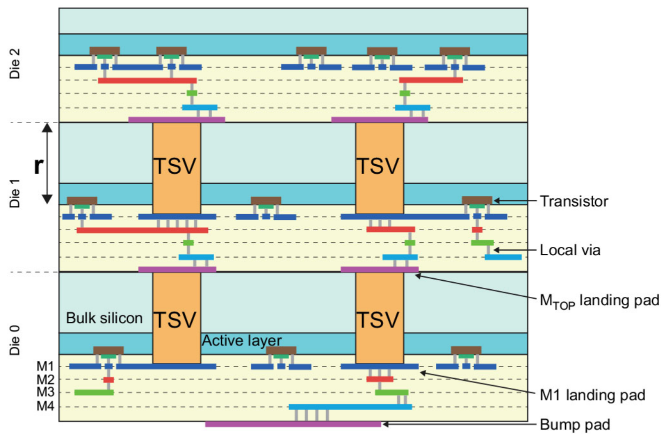

Fig. 1. 3-D integration using face-to-back bonding and through-silicon vias.

the applicability of the 3-D wirelength distribution models in Section VI and conclude in Section VII.

II. Preliminaries and Related Work

In this section, we give a brief overview of 3-D integration and review previous work on 2-D and 3-D wirelength distribution models.

A. 3-D Integration

3-D integration stacks multiple dies and fabricates interlayer vias (ILVs) for electrical connections among transistors placed in multiple dies as shown in Fig. 1. A representative technology for ILVs is the through-silicon via (TSV), which is created in the bulk silicon. Fig. 1 shows via-first TSVs.

3-D integration provides numerous benefits. First of all, 3-D integration enables much wider interchip (interdie) bandwidth than connecting multiple chips by the PCB trace on a PCB because the size of a TSV is much smaller than that of a PCB trace. Depending on the TSV fabrication technology, 3-D integration enables millions of connections between two dies [9]. 3-D integration also provides much faster signal transfer between two dies than the PCB trace because the capacitance of a TSV is much smaller than that of a PCB trace. Therefore, 3-D integration is considered a technology that can resolve various issues such as the memory bottleneck between a core chip and a memory chip in modern computer systems [10].

3-D integration also shortens interconnections among logic gates when the gates are placed in multiple dies in a 3-D IC. Since the interconnection in the modern VLSI chips is one of the most influential factor determining the performance, 3-D integration is also considered a very promising technology that can improve the performance of the chips by shortening interconnections. Similarly, shorter interconnections reduce dynamic power consumption, so 3-D integration can reduce the chip power while increasing the chip performance.

B. Wirelength Distribution Models for 2-D and 3-D ICs

Prediction of the wirelength distribution of a given circuit enables fast estimation of wiring requirements, clock frequency, dynamic power consumption, chip size, optimal multilevel interconnect structures, and so on [3], [11], [12]. The two representative wirelength distribution models developed for 2-D ICs are Donath's model in [13] and Davis' model in [3]. Due to its accuracy and simplicity, Davis' model has been used in various research since its development [12], [14].

Wirelength distribution models for 3-D ICs have also been developed by many researchers [4]–[8], [15]–[17]. These models naturally extend Davis' model to 3-D by counting the number of gate pairs and computing the probability that two gates at a distance of l are connected in 3-D. While some of these works assume that a vertical pitch is the same as a gate pitch, [5], [16] introduce and use a new parameter, r, to incorporate the die-to-gate-pitch ratio. If r is 40, for example, the die height (and the TSV height) is 40 times greater than the unit gate pitch. Since the TSV height varies in a wide range depending on the TSV manufacturing technology, incorporating the die-to-gate-pitch ratio has a significant importance in the prediction of the wirelength distribution of 3-D ICs.

Although the TSV size keeps shrinking, the width of the state-of-the-art TSVs is still nonnegligible. When the TSV size is nonnegligible, TSV insertion negatively affects the quality of 3-D ICs. Above all, TSV insertion increases the die area, which spreads gates out, thereby decreasing the amount of wirelength reduction obtainable by 3-D integration. In addition, TSVs have nonnegligible capacitance, which degrades timing and dynamic power consumption. Therefore, considering the TSV size and the TSV capacitance in wirelength and delay distribution models is very critical for the accurate prediction of the quality of 3-D ICs. However, none of the wirelength prediction models for 3-D ICs listed above considers the nonnegligible TSV size (especially, TSV width). Therefore, their prediction results are too optimistic and should be considered ideal cases.[1]

Focusing on the negative effects of TSVs, we derived wirelength distribution models considering the TSV size for 3-D ICs in [1], [18]. Based on the more accurate wirelength distribution models with simple buffer insertion strategies, we predicted TSV-aware delay distribution and power consumption of 3-D ICs in [2]. In addition, since the relative size between gates and TSVs determines the amount of the impact of TSVs on the quality of 3-D ICs, we explored the impact of transistor and TSV scaling on the quality of 3-D ICs in [19].

In this paper, we apply an optimal buffer insertion based on dynamic programming to the TSV-aware 3-D wirelength distribution models presented in [1] to predict delay distribution and power consumption of 3-D ICs more accurately. We also apply the models to various combinations of process and TSV technologies and predict delay and power consumption of current and future 3-D ICs.

III. Review of the TSV-Aware 3-D Wirelength Distribution Models

In this section, we review the TSV-aware 3-D wirelength distribution models presented in [1], show more validation results, and present some important prediction results.

[1]Monolithic 3-D integration uses very small ILVs, so the nonTSV-aware prediction models could be suitable for monolithic 3-D ICs.

TABLE I
VALIDATION OF OUR GATE-LEVEL 3-D WIRELENGTH DISTRIBUTION MODEL AGAINST [20]. TSV CELL WIDTH: 2.47 UM. # DIES: 4

Circuit	# gates	Wirelength (um)		Dif.
		Layout [20]	Prediction	
AL1	15K	243,610	223,529 (p=0.75)	-8.2%
AL2	30K	499,660	440,986 (p=0.70)	-11.7%
AL3	77K	1,256,812	1,273,580 (p=0.70)	1.3%
AL4	109K	1,462,919	1,353,450 (p=0.65)	-7.5%
AL5	324K	9,065,222	9,952,990 (p=0.75)	9.8%
AL6	445K	11,060,988	10,895,300 (p=0.70)	-1.5%
AL7	661K	18,873,297	17,749,000 (p=0.70)	-6.0%
			Geo. mean	-3.6%
			Geo. mean of |Dif.|	5.0%
MP1	16K	218,719	204,019 (p=0.75)	-6.7%
MP2	20K	310,355	276,932 (p=0.75)	-12.1%
MP3	88K	1,722,149	1,717,480 (p=0.75)	-0.3%
MP4	104K	1,702,177	1,737,010 (p=0.75)	2.0%
MP5	169K	2,729,148	2,768,850 (p=0.75)	1.5%
			Geo. mean	-3.0%
			Geo. mean of |Dif.|	2.4%

TABLE II
VALIDATION OF OUR BLOCK-LEVEL 3-D WIRELENGTH DISTRIBUTION MODEL AGAINST [21]. TSV CELL WIDTH: 5.0 UM. # DIES: 4

Circuit	# gates	Wirelength (um)		Dif.
		Layout [21]	Prediction	
C1	75K	1,167,650	1,223,400 (p=0.70)	4.8%
C2	92K	1,389,600	1,514,220 (p=0.70)	9.0%
C3	278K	8,643,000	8,296,370 (p=0.70)	-4.0%
C4	566K	18,624,000	19,211,530 (p=0.70)	3.2%
			Geo. mean	3.1%
			Geo. mean of |Dif.|	4.8%

TABLE III
COMPARISON BETWEEN NONTSV-AWARE [16] AND OUR TSV-AWARE WIRELENGTH DISTRIBUTION MODELS (TSV WIDTH = 0.001 UM)

# gates	# dies	Max. diff (%)	# gates	# dies	Max. diff (%)
10M	2	0.00745	40M	2	0.00772
	3	0.00813		3	0.00844
	4	0.00864		4	0.00899
	5	0.00904		5	0.00944
	6	0.00937		6	0.00982

A. Review and Validation of the TSV-Aware 3-D Wirelength Distribution Models

The TSV-aware 3-D wirelength distribution model for gate-level 3-D integration in [1] is derived as follows. TSV insertion affects the layout in two ways. First, TSVs occupy silicon area. Second, TSVs and gates do not overlap, i.e., gates cannot be placed on TSVs. The former results in larger footprint area in the model and the latter changes the total number of gate socket pairs at a distance. These two changes (footprint area and the number of gate socket pairs) lead to two noticeable results in the 3-D wirelength distribution. First, the number of short-distance gate socket pairs in the TSV-aware wirelength distribution model becomes smaller than that in the nonTSV-aware wirelength distribution model. Second, larger footprint area in the TSV-aware wirelength distribution model leads to longer average wirelength than the nonTSV-aware wirelength distribution model. Intuitively speaking, if larger TSVs are inserted, the footprint area will increase, so the average wirelength will go up. This phenomenon is observed only by TSV-aware 3-D wirelength distribution models and we explain more details on this in Section III-C.

B. Validation of the TSV-Aware 3-D Wirelength Distribution Models

In this section, we validate the TSV-aware gate- and block-level 3-D wirelength distribution models against 3-D layouts. We use $\alpha = 0.75$ and $k = 4.0$ for Rent's parameters and slightly adjust p for each benchmark.

Table I compares the wirelength of the layouts of the 12 benchmark circuits designed by [20] and the wirelength predicted by our TSV-aware gate-level 3-D wirelength distribution model. As the table shows, the maximum difference is 12.1%, but the average difference for the arithmetic circuits (AL1–AL7) is −3.6% and that for the microprocessor circuits (MP1–MP5) is −3.0%.[2]

[2] MP4 and MP5 consist of a few sub-designs. Therefore, instead of obtaining their prediction results directly from their input data, we divide the number of gates by the number of the sub-designs, obtain the wirelength of each sub-design, and multiply it by the number of the sub-designs.

Table II compares the wirelength of the layouts of the four benchmark circuits designed by [21] and the wirelength predicted by our TSV-aware block-level 3-D wirelength distribution model. The maximum difference is 9.0% and the average difference is 3.1%, which are acceptable as a prediction result in early design stages.

C. Prediction Results

In this section, we show a few important wirelength prediction results using our TSV-aware 3-D wirelength distribution models. The default values of the Rent's parameters, α, k, and p, are 0.75, 4.0, and 0.7, respectively.

1) Comparison of 3-D Wirelength Distribution Models: The first simulation compares the nonTSV-aware 3-D wirelength distribution model presented in [16] and our TSV-aware gate-level 3-D wirelength distribution model. By this comparison, we show the difference between ignoring and considering TSV size in the 3-D wirelength distribution models.

1) *Zero TSV Size:* Wirelength distribution models compute the number of wires at each wirelength (e.g., ten 300 um wires). In order to show that our TSV-aware wirelength distribution model approaches the nonTSV-aware model as the TSV size goes to zero, we set the TSV width to 0.001 um in our model and compare the number of wires of the two models at each wirelength. Table III shows the maximum difference of the number of wires at each wirelength. As the table shows, the maximum difference is negligible in all the test cases.
2) *Nonzero TSV Size:* Fig. 2(a) shows 3-D wirelength distributions when the TSV size is zero and 1.37 um. When the size is taken into account, the number of very short wires whose length is shorter than approximately 2 gate socket pitches decreases. The reason is because gates cannot be placed in the gate sockets occupied by TSVs, so the number of gate socket pairs at a short distance decreases. On the other hand, the number of wires whose length is longer than 2 gate socket pitches increases

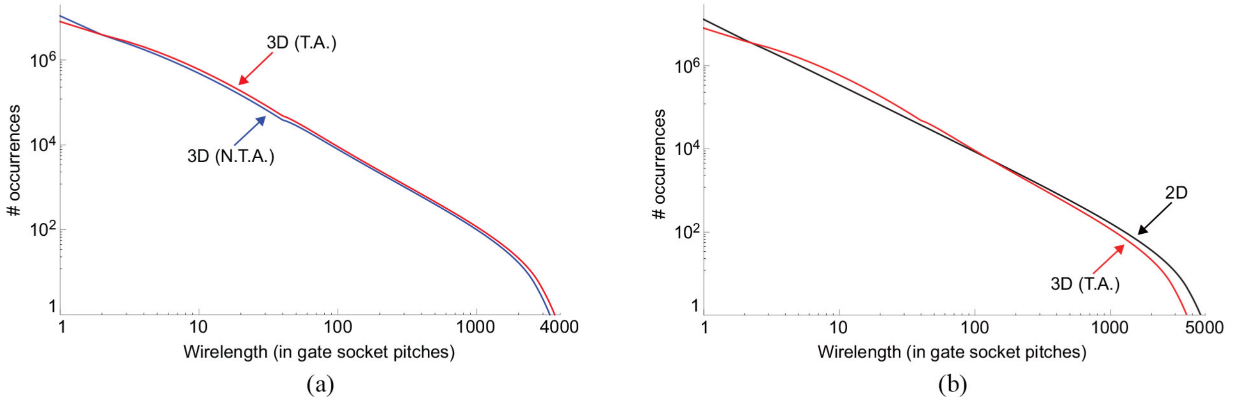

Fig. 2. (a) Wirelength distribution of the TSV-aware (T.A.) and nonTSV-aware (N.T.A.) 3-D wirelength distribution models. # gates: 10 M. # dies: 2. TSV width: 1.37 um. The average wirelength of the T.A. and N.T.A. models are 17.00 and 17.96 gate pitches, respectively. (b) Wirelength distribution of a 2-D and a 3-D designs.

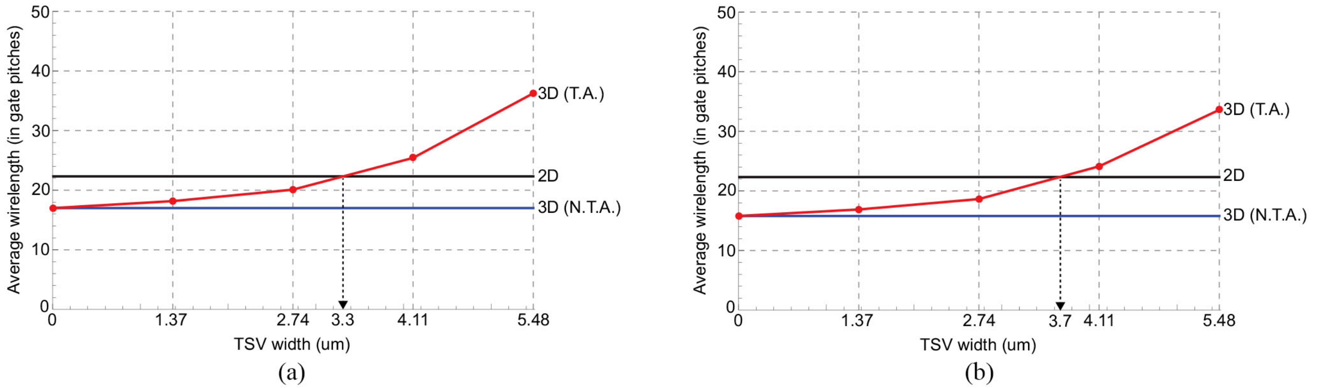

Fig. 3. Average wirelength versus TSV width plots of the TSV-aware (T.A.) and nonTSV-aware (N.T.A.) 3-D wirelength distribution models. (a) # gates: 10 M. # dies: 2. (b) # gates: 10 M. # dies: 4.

because of the area overhead caused by TSV insertion. Similarly, the longest wire of the TSV-aware model is longer than that of the nonTSV-aware model (3500 pitches versus 3200 pitches) due to the area overhead. Fig. 2(b) compares the wirelength distribution of 2-D and 3-D designs. The 3-D design has fewer short (shorter than three gate socket pitches) wires than the 2-D design because the 3-D design has fewer gate socket pairs at a distance of 1 or 2 gate socket pitches. The longest wire of the 3-D design is shorter than that of the 2-D design (about 3500 pitches versus 4600 pitches). However, the 3-D design has more medium-length wires than the 2-D design.

3) *Average Wirelength:* Fig. 3 compares the average wirelength of the nonTSV-aware and TSV-aware 3-D wirelength distribution models when the TSV width varies. It also shows the average wirelength of the 2-D design. In the figure, when the TSV width is zero, the wirelength of the 3-D design is approximately −24% shorter than that of the 2-D design. However, this amount of wirelength reduction decreases as the TSV width goes up. As shown in the figure, the average wirelength of the 2-D and 3-D designs becomes almost the same when the TSV width is about 3.3 um in the two-die case and 3.7 um in the four-die case. This threshold TSV width beyond which the average wirelength of the 3-D design becomes longer than that of the 2-D design strongly depends on the ratio between the TSV width and the average gate size.

TABLE IV
IMPACT OF TSV WIDTH ON THE WIRELENGTH, SILICON AREA, AND FOOTPRINT AREA (FP). # GATES = 40 M. GATE WIDTH = 1.37 UM. WE SHOW RATIOS BETWEEN 3-D AND 2-D DESIGNS

		TSV width / Gate width					
		0.5	1.0	1.5	2.0	2.5	3.0
# Dies=2	Wirelength	0.78	0.79	0.82	0.84	0.88	0.93
	Area	1.01	1.03	1.06	1.11	1.18	1.27
	FP	0.50	0.51	0.54	0.56	0.59	0.63
# Dies=4	Wirelength	0.72	0.75	0.77	0.80	0.83	0.89
	Area	1.01	1.05	1.15	1.24	1.38	1.55
	FP	0.25	0.26	0.28	0.32	0.35	0.39

2) Impact of TSV Size: In this simulation, we vary the TSV size and observe the change of the wirelength, total silicon area, and footprint area. Table IV shows the ratio of the three metrics between 3-D and 2-D designs. As the TSV width goes up, all the metrics monotonically increase. When the TSV width is half of the gate width, area overhead is almost negligible, so the total silicon area is almost equal to 1 and we achieve the largest wirelength reduction. On the other hand, when the TSV width is 3 × larger than the average gate width,

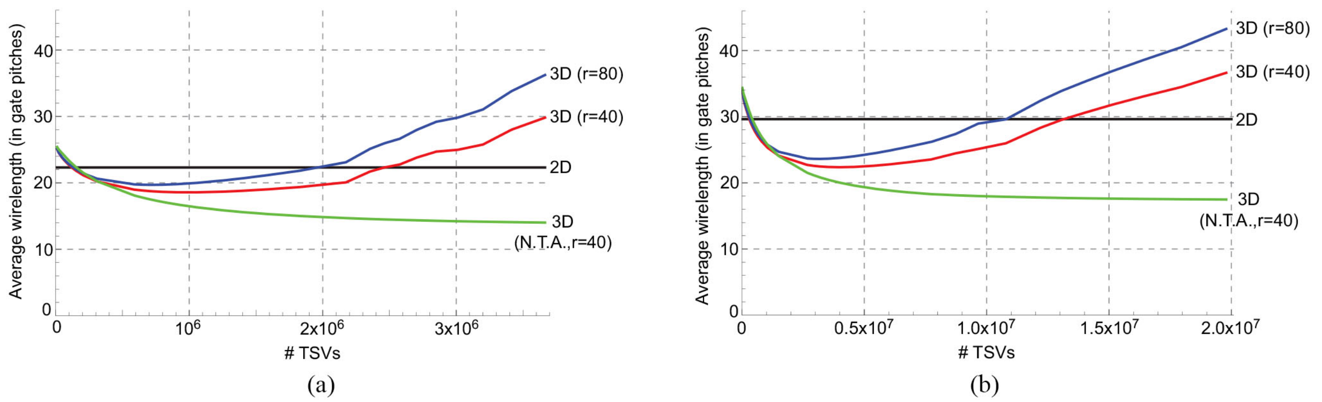

Fig. 4. Impact of the number of TSVs on the wirelength. "N.T.A." shows the average wirelength of the nonTSV-aware wirelength distribution model. (a) # gates: 10 M. # dies: 4. (b) # gates: 40 M. # dies: 4.

TABLE V
IMPACT OF THE DIE COUNT ON THE WIRELENGTH, SILICON AREA, FOOTPRINT AREA (FP), AND # TSVS. WE SHOW RATIOS BETWEEN 3-D AND 2-D DESIGNS. $r = 40$

		# Dies					
		2	3	4	5	6	7
# Gates=10M	Wirelength	0.90	0.85	0.84	0.84	0.84	0.85
	Area	1.20	1.30	1.38	1.45	1.50	1.54
	FP	0.59	0.44	0.35	0.29	0.26	0.23
	# TSVs ($x10^5$)	6.8	10.5	13.1	15.3	17.2	18.6
# Gates=40M	Wirelength	0.86	0.79	0.77	0.75	0.75	0.75
	Area	1.21	1.33	1.42	1.49	1.55	1.60
	FP	0.60	0.45	0.36	0.29	0.26	0.23
	# TSVs ($x10^5$)	7.2	11.2	14.1	16.6	18.7	20.4

the area overhead of the 3-D design is about 25% and 50% in the two-die and the four-die cases, respectively as shown in the table. However, the wirelength of the 3-D design is still shorter than that of the 2-D design.

3) Impact of the Die Count: In this simulation, we vary the number of dies and compare area, footprint area, wirelength, and the number of TSVs. Table V shows the impact of the die count on those metrics.

As shown in Table V, as more dies are stacked, more vertical connections are needed, so the TSV count and the total silicon area go up. The average wirelength initially decreases as more dies are stacked, but saturates when the die count is around five. The wirelength eventually goes up as shown in the 10-M-gate case because stacking more dies requires more TSVs. From the table, we predict that three or four is the best die count that sufficiently reduces the wirelength with a reasonable amount of area overhead.[3]

4) Impact of # TSVs: In this simulation, we vary the number of TSVs by changing r and observe the average wirelength. Fig. 4 shows the average wirelength when the TSV count varies. As the TSV count increases from zero, the wirelength of the 3-D designs begins to decrease. However, as the TSV count increases further, the wirelength starts increasing. The reason is because inserting too many TSVs causes serious area overhead, so the average gate-to-gate distance eventually increases. Fig. 4 also shows that the wirelength of the nonTSV-aware wirelength distribution model monotonically decreases as the TSV count goes up. This is because the nonTSV-aware prediction model does not consider the area overhead due to TSV insertion.

[3]Other types of 3-D ICs could still benefit from stacking more dies. For instance, stacking more memory dies in core-to-memory stacking increases the total memory. Similarly, integrating more processing elements in the additional dies increases the computation capacity.

IV. TSV-AWARE PREDICTION OF DELAY AND POWER CONSUMPTION OF 3-D ICS

Prediction of delay and power consumption of 3-D ICs using wirelength distribution models have been presented in various works [2], [6]–[8], [14]–[16]. However, all of them except [2] are based on nonTSV-aware wirelength distribution models, so their models cannot reflect the negative effects of the TSV size and the results are optimistic. On the other hand, [2] uses TSV-aware wirelength distribution models, but the buffering algorithm that the work uses is not optimal, so their buffering schemes and prediction results are pessimistic.

In this section, we predict delay and power consumption of 3-D ICs using our TSV-aware wirelength distribution models and an optimal buffer insertion algorithm based on dynamic programming. We also vary the TSV capacitance to investigate the impact of TSV capacitance on delay and power of 3-D ICs.

A. Preliminaries

1) TSV Resistance and Capacitance: The resistance of a TSV consists of material resistance ($= \rho \cdot \frac{l}{S}$) of the TSV itself and contact resistance between the TSV and a landing pad at both ends of the TSV. The material resistance is relatively small compared to wire resistance. For instance, when a TSV is made of tungsten and its width and height are 2 um and 20 um, respectively, the material resistance is just 280 mΩ, which is similar to the resistance of a 0.1 um-long wire at 45 nm technology. Contact resistance is dependent on the process technology and also quite small (a few milli ohms to one ohm). Therefore, TSV resistance has negligible impact on the delay of the RC tree of a given net. On the other hand, TSV capacitance varies in a wide range from a few femto farads to tens of femto farads depending on the TSV width, height, and the liner thickness. Therefore, TSV capacitance has a great impact on the delay and dynamic power consumption

of 3-D nets. In our simulation, we vary the TSV capacitance and investigate the impact of TSVs on the delay and dynamic power consumption of 3-D ICs.

2) Dynamic Programming-Based Buffer Insertion: Reference [22] proposed an optimal buffer insertion algorithm based on dynamic programming. It uses the Elmore delay model for delay calculation and optimally solves buffer insertion problems for single nets. The idea of the paper is to build a candidate tree starting from the sinks of a given net and traversing toward the driver. Although the candidate tree grows exponentially, the algorithm prunes inferior candidates by comparing load capacitance and required arrival time. For a two-pin net, therefore, the number of candidates increases linearly. Even when it considers multiple buffers at each candidate location, the solution space increases linearly.

B. Analysis of the Wirelength Distribution of 3-D ICs

The wirelength distribution of a 3-D design consists of two sub-distributions, one for 2-D nets and the other for 3-D nets. Fig. 5 shows the breakdown of the wirelength distribution of a 10 M-gate two-die 3-D design. The curve denoted as 3-D is the wirelength distribution of the 3-D design and the two curves denoted as SC1 and SC2 are the breakdown of it. SC1 shows the number of 2-D (planar) nets and SC2 shows the number of 3-D nets (having a TSV).[4] Since the TSV height is 40 um in this simulation, all the nets shorter than 40 um are 2-D nets.

The wirelength distribution of the 2-D nets (SC1) of the 3-D design is monotonically decreasing similarly as the wirelength distribution of the 2-D design. However, the wirelength distribution of the 3-D nets (SC2) is Λ-shaped. A simple example explains this phenomenon as follows. The number of nets of length l is proportional to the product of $I_{\exp}[l]$ (# interconnects between two gate pairs separated by l gate pitches) and $M_t[l]$ (# gate pairs separated by l gate pitches in 3-D). Comparing the number of 40 um-long and 41 um-long 3-D nets, $I_{\exp}[41 - um]$ is almost the same as $I_{\exp}[40 - um]$, but $M_t[41 - um]$ is greater than $M_t[40um]$. Therefore, the number of 3-D nets of length l longer than 40-um initially increases. However, as the wirelength increases, $I_{\exp}[l]$ becomes a dominant factor and $M_t[l]$ becomes monotonically decreasing after a certain wirelength value, so the number of 3-D nets eventually decreases as shown in Fig. 5. Although the 2-D nets dominate the wirelength distribution of the 3-D design, 3-D nets have nonnegligible (or dominant) impact on the delay and power consumption of the 3-D design depending on the TSV capacitance as shown in the next section.

C. Delay Distribution and Power Consumption of 3-D ICs

Our simulation setting for delay distribution and power consumption of 3-D ICs is as follows. The average gate width is 1.37 um, which is similar to the width of a two-input NAND gate in 45 nm technology. The default width of a TSV cell is also 1.37 um. TSV height is 40 um. We use 10 fF and

[4]A 3-D net in a 3-D design built in D dies can have maximum $D - 1$ TSVs in the wirelength distribution model. Therefore, a 3-D net in Fig. 5 has one TSV.

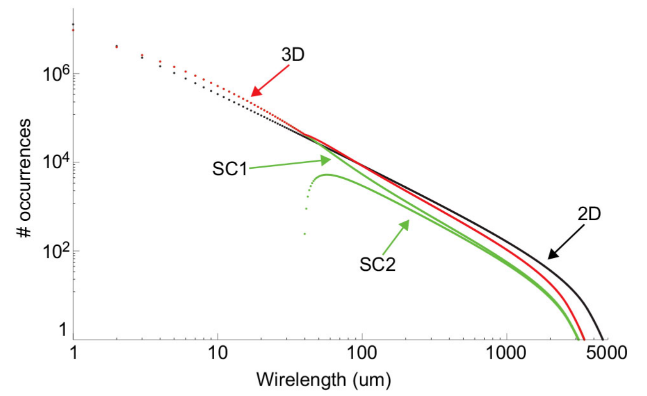

Fig. 5. Wirelength distribution of 2-D and 3-D designs. # gates: 10M. # dies: 2. Average gate width: 1.37 um. TSV width: 1.37 um. TSV height: 40 um. SC1 and SC2 are the wirelength distributions of the 2-D and 3-D nets, respectively, of the 3-D design.

50 fF for TSV capacitance. In our buffer insertion, we use three buffer sizes, 1×, 5×, and 20×. The wire resistance and capacitance are 3.31Ω/um and 0.171 fF/um, respectively. The average gate switching activity is 0.3 and the supply voltage is 1 V.

1) Delay Distribution of 3-D ICs: Fig. 6 shows the delay distribution of 2-D, two-die 3-D, and four-die 3-D designs having ten million gates when TSV capacitance is (a) 10 fF and (b) 50 fF. The delay distribution of the 2-D design monotonically decreases as the delay goes up.[5] The reason is because the wirelength distribution monotonically decreases as the wirelength goes up as shown in Fig. 5. For 2-D nets, longer nets always have longer delay than shorter nets (for both before and after optimal buffer insertion). Therefore, the delay distribution of the 2-D design is very similar to its wirelength distribution.

On the other hand, 3-D designs have quite different delay distribution. In general, the delay distribution of the 3-D designs also monotonically decreases. However, we observe discontinuities at some points. For example, discontinuities exist around 200 ps in Fig. 6(a) and around 20, 150, and 200 ps in Fig. 6(b). To further investigate the discontinuities in the delay distribution of the 3-D designs, we group the nets into D sets where D is the number of dies and the nets in each set has the same number of TSVs (0, ..., $D - 1$). Fig. 6(c) and (d) shows the delay distribution of each set. In the delay distribution of the two-die 3-D design, we observe two different curves. The monotonically decreasing curve in the upper region comes from the 2-D nets (SC1) shown in Fig. 5, whereas the Λ-shaped curve in the lower region comes from the 3-D nets (SC2) having a TSV in Fig. 5. Similarly, the delay distribution of the four-die 3-D design consists of four curves. The monotonically decreasing curve comes from the 2-D nets, whereas the three Λ-shaped curves in the lower region come from the 3-D nets. Specifically, the topmost, the middle, and the bottommost Λ-shaped curves come from the 3-D nets having one, two, and three TSVs, respectively. We observe similar trends when TSV capacitance is 50 fF as shown in Fig. 6(d).

[5]The side branches around the main distribution curve are due to round-off errors.

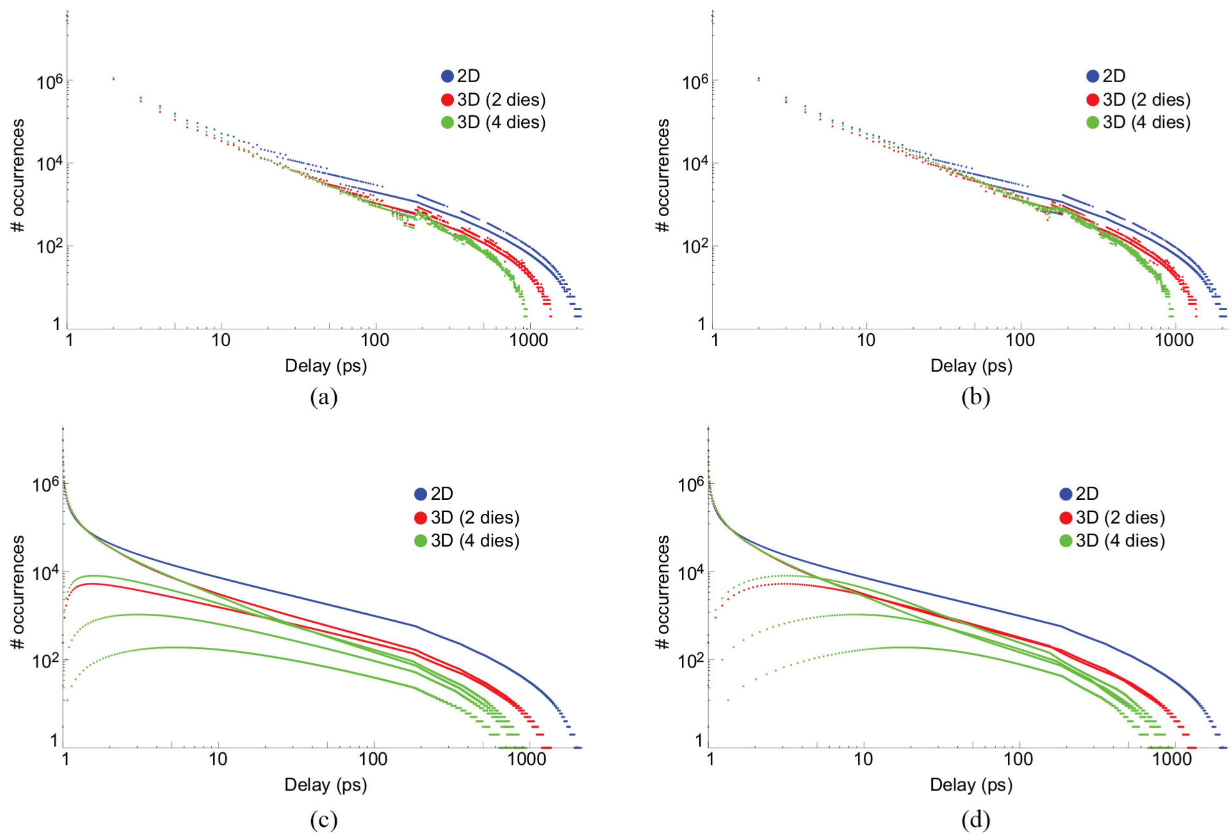

Fig. 6. Delay distribution of 2-D, two-die 3-D, and four-die 3-D ICs. # gates: 10M. TSV width: 1.37 um. (a) TSV capacitance: 10 fF. Max. delay: 1.55 ns (2-D), 1.00 ns (two-die), 0.70 ns (four-die). (b) TSV capacitance: 50 fF. Max. delay: 1.55 ns (2-D), 1.00 ns (two-die), 0.71 ns (four-die). (c) Breakdown of the delay distribution of (a). (d) Breakdown of the delay distribution of (b).

The only difference is that higher TSV capacitance increases the delay of 3-D nets. Therefore, when the TSV capacitance increases from 10 fF to 50 fF, the delay distribution of the 3-D nets moves to the right.

In spite of the increased delay of the 3-D nets, the worst net delay remains almost the same. For instance, the worst delay of the two-die 3-D designs is 1 ns and that of the four-die 3-D designs is 0.7 ns when the TSV capacitance is 10 fF or 50 fF. The reason is because wire capacitance is much more dominant than the TSV capacitance in the longest net. However, notice that higher TSV capacitance will result in higher power consumption.

2) Impact of TSV Width on Delay and Power: In this simulation, we vary the TSV width and observe the ratio of the wirelength, worst delay, and total power consumption between 2-D and 3-D designs. Table VI shows the three metrics when the die count is two and four.

When the TSV width increases, area overhead due to TSV insertion also goes up, so the average and the longest wirelength increases too, which results in the increase of the worst signal delay as shown in Table VI. When the die count is two, using 2× and 3× TSVs causes 7% and 25% delay overhead, respectively, as compared to the 1× TSV case. Similarly, when the die count is four, using 2× and 3× TSVs causes 10% and 25% delay overhead, respectively, as compared to the 1× TSV case.

TABLE VI
IMPACT OF TSV WIDTH ON THE WIRELENGTH, WORST DELAY (D), AND POWER (P) OF 3-D ICS. ALL THE VALUES ARE NORMALIZED TO THE VALUES OF 2-D ICS. N_D IS THE NUMBER OF DIES AND C_T IS THE TSV CAPACITANCE. A UNIT GATE PITCH: 1.37 UM

		TSV width(um)					
		0.5	1.0	1.5	2.0	2.5	3.0
N_D: 2	Wirelength	0.778	0.797	0.821	0.849	0.882	0.922
	D (C_T=10fF)	0.625	0.634	0.646	0.661	0.679	0.701
	D (C_T=50fF)	0.625	0.634	0.646	0.661	0.679	0.701
	P (C_T=10fF)	0.784	0.791	0.800	0.811	0.824	0.839
	P (C_T=50fF)	0.873	0.881	0.890	0.901	0.914	0.929
N_D: 4	Wirelength	0.722	0.740	0.763	0.789	0.819	0.853
	D (C_T=10fF)	0.433	0.439	0.450	0.464	0.482	0.504
	D (C_T=50fF)	0.438	0.445	0.455	0.470	0.488	0.509
	P (C_T=10fF)	0.766	0.773	0.782	0.792	0.803	0.816
	P (C_T=50fF)	0.948	0.955	0.964	0.974	0.985	0.998

Power consumption of the 3-D designs also goes up as the TSV width increases. Since larger TSV width results in longer average wirelength, the increase of the total power consumption is primarily due to the increase of the interconnect power. For further investigation, we show the breakdown of the total power consumption in Table VII. In the table, we observe that as the TSV width goes up, the portion of the interconnect and buffer power increases whereas the portion of the gate and TSV power decreases. The buffer count also increases because the average wirelength goes up as the TSV width increases. However, its impact on power is very small because the gate,

TABLE VII
BREAKDOWN OF THE TOTAL POWER CONSUMPTION SHOWN IN TABLE VI. INT. DENOTES INTERCONNECT POWER AND C_T IS THE TSV CAPACITANCE. N_D IS THE NUMBER OF DIES

		TSV width(um)					
		0.5	1.0	1.5	2.0	2.5	3.0
N_D: 2, C_T=10fF	Gate	61.1%	60.5%	59.8%	59.0%	58.1%	57.0%
	Int.	34.7%	35.3%	36.0%	36.8%	37.7%	38.7%
	TSV	2.8%	2.8%	2.8%	2.7%	2.7%	2.6%
	Buffer	1.4%	1.4%	1.4%	1.5%	1.5%	1.7%
N_D: 2, C_T=50fF	Gate	54.8%	54.3%	53.8%	53.1%	52.4%	51.5%
	Int.	31.2%	31.7%	32.4%	33.1%	34.0%	35.0%
	TSV	12.7%	12.6%	12.4%	12.3%	12.1%	11.9%
	Buffer	1.3%	1.4%	1.4%	1.5%	1.5%	1.6%
N_D: 4, C_T=10fF	Gate	62.4%	61.9%	61.2%	60.4%	59.6%	58.6%
	Int.	31.0%	31.6%	32.3%	33.1%	34.0%	34.9%
	TSV	5.9%	5.8%	5.8%	5.7%	5.6%	5.5%
	Buffer	0.7%	0.7%	0.7%	0.8%	0.8%	1.0%
N_D: 4, C_T=50fF	Gate	50.5%	50.1%	49.7%	49.1%	48.6%	48.0%
	Int.	25.0%	25.5%	26.1%	26.9%	27.7%	28.6%
	TSV	23.7%	23.6%	23.4%	23.1%	22.8%	22.5%
	Buffer	0.8%	0.8%	0.8%	0.9%	0.9%	0.9%

interconnect, and TSV power dominates the total power consumption of the 3-D designs. We find similar trends in the four-die 3-D design as shown in Table VII. Since four-die stacking uses more TSVs than two-die stacking, the portion of the TSV power in the four-die 3-D design is greater than that in the two-die 3-D design.

3) Impact of # Dies on Delay and Power: In this simulation, we vary the die count and observe the delay and power of 3-D designs. Table VIII shows ratios of the worst delay and total power between ten-million-gate 2-D and 3-D designs when the die count varies from two to ten. As the die count increases, the worst delay of the 3-D design monotonically decreases. When the die count is two and four, the worst delay of the 3-D design is about 65% and 45% of that of the 2-D design, respectively. In addition, if the die count is less than seven, the TSV capacitance does not affect the worst delay because wire capacitance dominates the total capacitance of the longest net in those cases. However, when the TSV capacitance is 50 fF, the worst delay of the 3-D design saturates if the die count is greater than six. On the other hand, when the TSV capacitance is 10 fF, the worst delay of the 3-D design keeps decreasing as the die count goes up although it will eventually saturate. We find similar trends for forty-million-gate 2-D and 3-D designs as shown in Table VIII.

Power consumption shows a similar trend as the worst delay, but we observe more clear power overhead. When the gate count is ten million and the TSV capacitance is 10 fF, the total power remains almost the same (80% of the 2-D design) regardless of the die count as shown in Table VIII. However, if the TSV capacitance is 50 fF, the total power starts increasing when more than two dies are stacked. Moreover, if more than five dies are stacked, the total power of the 3-D design becomes greater than that of the 2-D design. We find similar trends when the gate count is forty million as seen in Table VIII. This power overhead is primarily due to the power consumption driving TSVs. For more in-depth analysis, we show the breakdown of the total power in Table IX for the ten-million- and forty-million-gate designs,

TABLE VIII
IMPACT OF THE DIE COUNT ON THE WIRELENGTH, WORST DELAY (D), AND POWER (P). #G IS THE NUMBER OF GATES AND C_T IS THE TSV CAPACITANCE. TSV WIDTH: 1.37 UM. A UNIT GATE PITCH: 1.37 UM

		# Dies					
		2	3	4	5	6	7
#G=10M	Wirelength	0.814	0.770	0.757	0.754	0.756	0.760
	D (C_T=10fF)	0.642	0.522	0.447	0.398	0.360	0.331
	D (C_T=50fF)	0.642	0.528	0.452	0.404	0.368	0.339
	P (C_T=10fF)	0.798	0.783	0.779	0.780	0.782	0.785
	P (C_T=50fF)	0.887	0.926	0.961	0.993	1.020	1.044
#G=40M	Wirelength	0.774	0.714	0.689	0.679	0.475	0.674
	D (C_T=10fF)	0.654	0.535	0.463	0.413	0.375	0.346
	D (C_T=50fF)	0.654	0.538	0.466	0.416	0.377	0.348
	P (C_T=10fF)	0.746	0.720	0.710	0.707	0.706	0.707
	P (C_T=50fF)	0.827	0.849	0.875	0.901	0.925	0.947

TABLE IX
BREAKDOWN OF THE TOTAL POWER CONSUMPTION SHOWN IN TABLE VIII. INT. DENOTES INTERCONNECT POWER AND C_T IS THE TSV CAPACITANCE

		# Dies					
		2	3	4	5	6	7
#G=10M, C_T=10fF	Gate	60.0%	61.1%	61.4%	61.3%	61.2%	60.9%
	Int.	35.8%	33.4%	32.1%	31.3%	30.8%	30.5%
	TSV	2.9%	4.5%	5.8%	6.7%	7.5%	8.2%
	Buffer	1.3%	1.0%	0.7%	0.7%	0.5%	0.4%
#G=40M, C_T=50fF	Gate	53.9%	51.7%	49.8%	48.2%	46.9%	45.8%
	Int.	32.2%	28.2%	26.0%	24.6%	23.6%	22.9%
	TSV	12.5%	19.1%	23.4%	26.5%	28.9%	30.7%
	Buffer	1.4%	1.0%	0.8%	0.7%	0.6%	0.6%
#G=10M, C_T=10fF	Gate	53.6%	55.6%	56.3%	56.6%	56.6%	56.6%
	Int.	40.9%	37.9%	36.2%	35.1%	34.4%	33.9%
	TSV	2.6%	4.4%	5.7%	6.8%	7.7%	8.4%
	Buffer	2.9%	2.1%	1.8%	1.5%	1.3%	1.1%
#G=40M, C_T=50fF	Gate	48.4%	47.1%	45.7%	44.4%	43.3%	42.3%
	Int.	37.0%	32.2%	29.4%	27.6%	26.3%	25.3%
	TSV	12.0%	18.7%	23.3%	26.6%	29.2%	31.3%
	Buffer	2.6%	2.0%	1.6%	1.4%	1.2%	1.1%

respectively. As the die count increases, the number of 2-D nets decreases and more 3-D nets are generated. Therefore, the total TSV count goes up, so does the power consumed to drive TSVs. As seen in the table, 10 fF TSV capacitance does not cause serious power overhead for both ten-million- and forty-million-gate designs. However, 50 fF TSV capacitance leads to serious (greater than 20%) power overhead and the TSV power reaches approximately 35% of the total power as the die count increases.

Although 10 fF capacitance causes little power overhead, delay reduction and power overhead/saving depend on the die count and the relative size between TSV parameters (width, height, capacitance) and circuit/device parameters (average gate width, wire resistance and capacitance, transistor driving strength, and so on). Therefore, more advanced technology nodes should use smaller TSVs having lower capacitance to obtain the same amount of delay reduction and power saving.

V. IMPACT OF TRANSISTOR AND TSV SCALING

As the previous sections show, TSV size and capacitance have negative effects on the quality of 3-D ICs. Since large TSVs cause more serious area overhead and generally have higher capacitance, TSVs have been downsized from a few micro-meter width to submicrometer width.

TABLE X
PARAMETERS OF EACH PROCESS TECHNOLOGY USED IN OUR TRANSISTOR AND TSV SCALING SIMULATIONS. L_{gate}, D_{buf}, R_{buf}, AND C_{buf} DENOTE AVERAGE GATE WIDTH, BUFFER DELAY, BUFFER OUTPUT RESISTANCE, AND BUFFER INPUT CAPACITANCE, RESPECTIVELY, OF A 20× BUFFER. P_{gate} IS THE AVERAGE GATE POWER, R_{wire} IS THE UNIT WIRE RESISTANCE, AND C_{wire} IS THE UNIT WIRE CAPACITANCE

Process	L_{gate} (um)	D_{buf} (ps)	R_{buf} (Ω)	C_{buf} (fF)	P_{gate} (uW)	R_{wire} (Ω/um)	C_{wire} (fF/um)	V_{DD} (V)
130 nm	2.26	137	150	3.00	16.22	1.69	0.171	1.25
90 nm	1.92	109	195	2.43	12.46	2.11		1.20
65 nm	1.64	88	220	1.94	9.14	2.65		1.10
45 nm	1.37	70	305	1.55	6.65	3.31		1.00
32 nm	1.07	56	360	1.24	5.05	4.14		0.95
22 nm	0.78	45	425	1.00	3.83	5.17		0.90
16 nm	0.62	36	500	0.80	2.89	6.46		0.85
11 nm	0.45	29	590	0.64	2.18	8.08		0.80

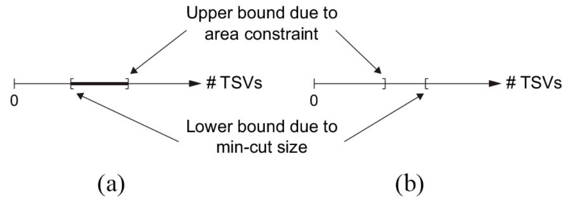

Fig. 7. Relationship between the lower and the upper bounds of the TSV count in physically feasible/infeasible designs. (a) Physically realizable designs. (b) Physically unrealizable designs.

However, transistors have also been downsized following Moore's law [23]–[26]. Therefore, various combinations of TSV and process technologies exist for building 3-D ICs and the impact of TSVs on the quality of 3-D ICs is actually determined by the technology combination as a layout-based study shows in [27]. In this section, we investigate the quality of 3-D ICs built by various combinations of TSV and process technologies.

A. Physical Realizability of 3-D ICs

In the previous sections, we assumed that any number of TSVs could be used in 3-D ICs. In reality, however, lower and upper bounds on the number of TSVs exist. The lower bound is determined by the minimum cut size, which can be estimated by multiway min-cut partitioning tools. On the other hand, The upper bound is determined by area constraints, which specify the maximum additional area for TSV insertion.

Once we obtain the lower and the upper bounds on the TSV count, we can determine whether a given design is physically realizable or not under the given area constraints. Fig. 7 shows two examples. In Fig. 7(a), the lower bound is smaller than the upper bound, so the number of available TSVs lies between the bounds and the design is physically realizable at least in terms of the TSV count. In Fig. 7(b), however, the lower bound is greater than the upper bound, so the design is physically unrealizable. If a design is physically unrealizable under given constraints, we can make it physically realizable by using smaller TSVs, alleviating the area constraints, or reducing the die count, which leads to the use of fewer TSVs.

In the following sections, we obtain the average wirelength for each combination of a process and a TSV technologies and analyze the impact of the process and TSV scaling. We use 10% for the area constraint and 0.002·(n − 1)·(# nets) for the lower bound of the TSV count for n-die 3-D ICs. To determine the lower bound on the TSV count, we performed multiway min-cut partitioning using hMetis [28] on various circuits and obtained loose criteria on the minimum number of TSVs. Table X shows the parameters at each process technology used in our paper.

B. Average Wirelength

Fig. 8(a) and (b) shows the average wirelength of 2-D and 3-D ICs built with various technology combinations when the gate count is 40 M and the die count is two and four, respectively. The dashed lines and the solid lines are the average wirelength of 2-D and 3-D ICs, respectively. The disconnection of the solid lines in the lower-left region in the figures is due to the physical unrealizability.

In this simulation, we observe two important prediction results. First, each process technology has a threshold TSV size that determines the physical realizability. For instance, the maximum TSV width to satisfy the 10% area constraint for two-die 3-D ICs built with 22 nm process technology is approximately 2.0 um. If the TSV size is greater than 2.0 um in this case, it is likely that the 3-D ICs cannot satisfy the given area constraint. Of course, using smaller TSVs is always preferred to reduce the wirelength.

Second, 3-D ICs built with a process technology and extremely small (almost zero width) TSVs, which is an extreme case, could have longer wirelength than 2-D ICs built with a more advanced process technology. For instace, a two-die 3-D IC built with 65 nm process technology and 0.1 um TSVs has longer average wirelength than a 2-D IC built with 32 nm process technology in Fig. 8(a). This observation means that not only the 3-D integration but also process scaling have a big impact on the wirelength reduction. From Fig. 8(a) and (b), we predict that the wirelength of two-die and four-die 3-D ICs built with a process technology and TSVs of almost zero width is very similar to that of 2-D ICs built with a process technology approximately two generations and three generations ahead, respectively.

C. Worst Delay

Fig. 9(a) and (b) show the worst delay of 2-D and 3-D ICs built with various technology combinations when the gate count is 40 M and the die count is two and four, respectively. The dashed lines and the solid lines are the worst delay of 2-D and 3-D ICs, respectively.

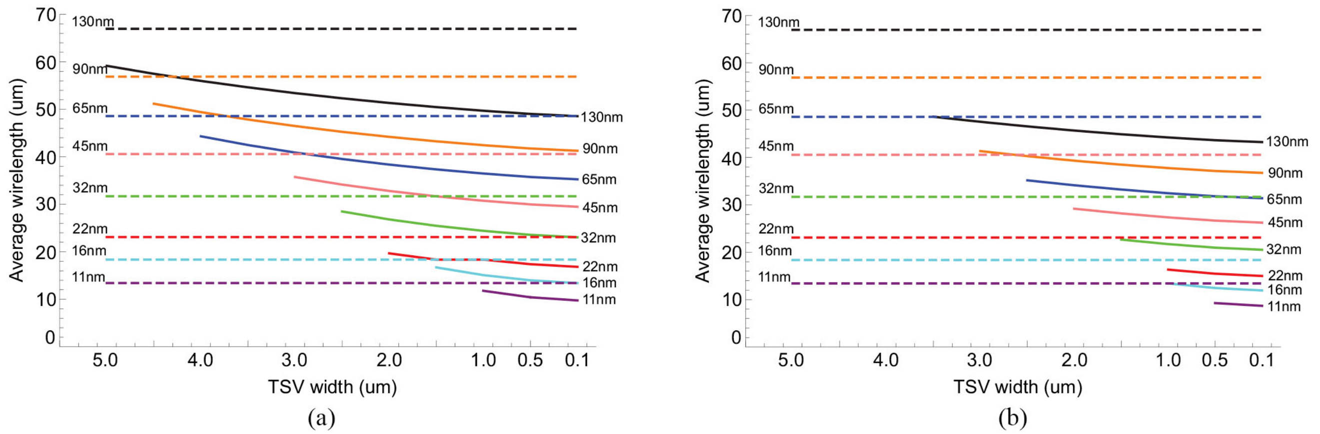

Fig. 8. Comparison of the average wirelength of 2-D and 3-D ICs built with various combinations of 2-D and 3-D technologies. Dashed lines: average wirelength of 2-D ICs. Solid lines: average wirelength of 3-D ICs. (a) # gates: 40 M. # dies: 2. (b) # gates: 40 M. # dies: 4.

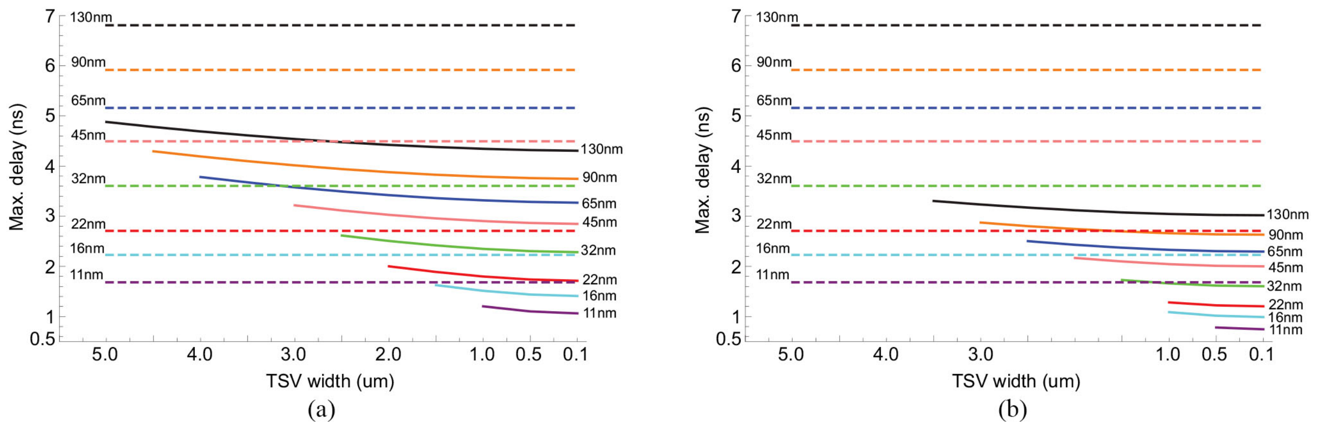

Fig. 9. Comparison of the worst delay of 2-D and 3-D ICs built with various combinations of 2-D and 3-D technologies. TSV capacitance: 10 fF. Dashed lines: worst delay of 2-D ICs. Solid lines: worst delay of 3-D ICs. (a) # gates: 40 M. # dies: 2. (b) # gates: 40 M. # dies: 4.

As Fig. 9 shows, the worst delay result looks similar to the average wirelength result. However, we observe greater benefits in the worst delay than the average wirelength. For example, the 3-D IC built with 130 nm technology and 5 um-width TSVs has longer wirelength than the 2-D IC built with 90 nm technology in Fig. 8(a), but the 3-D IC has the smaller worst delay even than the 2-D IC built with 65 nm technology in Fig. 9(a). We observe similar trends in the four-die cases as shown in Figs. 8(b) and 9(b).

In Fig. 9(a), we observe that the worst delay of two-die 3-D ICs built with a process technology is similar to that of 2-D ICs built with a process technology approximately two to three generations ahead. In Fig. 9(b), the generation gap goes up to four because stacking more dies generally reduces the wirelength further.

D. *Power Consumption*

Fig. 10(a) and (b) shows the total power consumption of 2-D and 3-D ICs built with various technology combinations when the gate count is 40 M and the die count is two and four, respectively. The dashed lines and the solid lines are the power consumption 2-D and 3-D ICs, respectively.

As Fig. 10(a) shows, the power consumption of two-die 3-D ICs built with a process technology is comparable to that of 2-D ICs built with a one-generation-ahead process technology. However, we observe that the power consumption of four-die 3-D ICs is greater than that of two-die 3-D ICs. Therefore, the power consumption of four-die 3-D ICs built with a process technology is greater than that of 2-D ICs built with a one-generation-ahead process technology. Note that 3-D ICs built with a process technology have higher power consumption than 2-D ICs built with the same process technology in Fig. 10(b) because we use a single TSV value for all the simulation. Since smaller TSVs likely have lower TSV capacitance, the power consumption of the 3-D ICs will have lower power consumption than the 2-D ICs if TSV capacitance is also scaled down.

VI. Discussion

In this section, we discuss how our prediction models can be applied to nonplanar transistor technologies, layout proximity effects, and monolithic 3-D integration.

A. *Nonplanar Transistor Technologies*

The most important input parameters to the wirelength distribution models are the number of gates, die area (or utilization), the average gate size, and Rent's parameters. Therefore, even if the shape of the transistors changes, it does

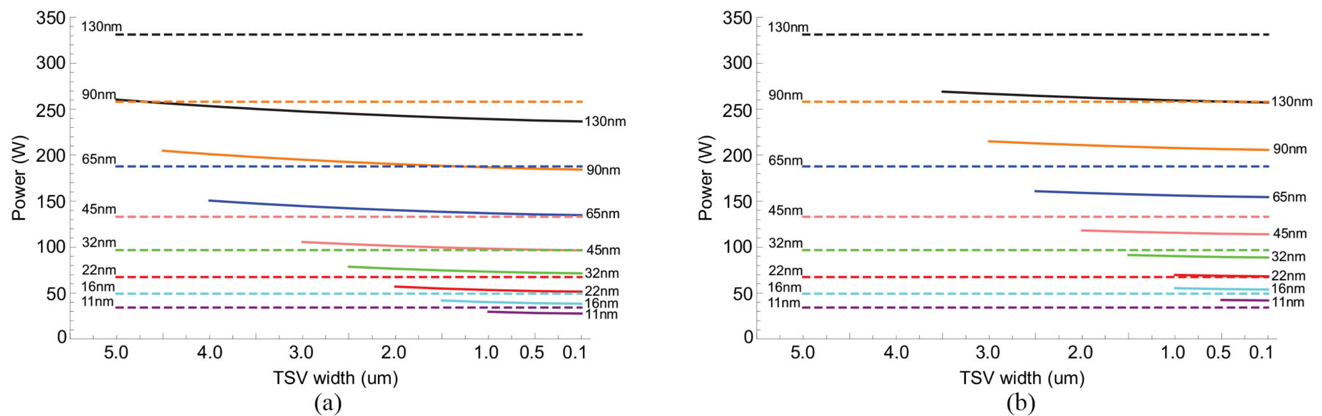

Fig. 10. Comparison of the power consumption of 2-D and 3-D ICs built with various combinations of 2-D and 3-D technologies. TSV capacitance: 10 fF. Dashed lines: power consumption of 2-D ICs. Solid lines: power consumption of 3-D ICs. (a) # gates: 40 M. # dies: 2. (b) # gates: 40 M. # dies: 4.

not affect the derivation of the wirelength distribution models, but the average gate size might change. In other words, L_{gate} in Table X for the sub-30 nm technologies might increase (or decrease) if we consider the characteristics of the nonplanar transistors such as FinFETs more accurately. Similarly, we can predict the wirelength distribution of the circuits built with other types of transistors such as gate-all-around FETs without significant modification of the wirelength distribution models.

B. Layout Proximity Effects

Various design methodologies and optimization algorithms have been proposed to minimize layout proximity effects. For instance, enforcing minimum keep-out zone from well implant edges reduces well proximity effects, thereby minimizing variation of devices, and optical proximity correction and phase-shift masks improve the printability. Integrating these design methodologies and optimization algorithms into the wirelength distribution models requires abstraction of the characteristics of the methodologies and algorithms. For example, enforcing the minimum keep-out zone slightly increases the width of standard cells, which can be modeled by adjusting L_{gate} in Table X.

C. Monolithic 3-D ICs

Monolithic 3-D integration builds more than one silicon dies sequentially and electrically connects them by very small monolithic interdie vias, thereby enabling ultrahigh-density integration. Since the size of a monolithic interdie via is comparable to that of a local via, monolithic 3-D integration provides a new design option, which is designing and using 3-D standard cells [29]. 3-D standard cells are 30% to 40% smaller than 2-D standard cells, so we need to change the value of L_{gate} to predict the quality of monolithic 3-D ICs. In addition, since a monolithic intervia is much smaller than a TSV used in bonding-based 3-D ICs, we should set the area of a TSV cell in [1] to that of a monolithic intertier via (or zero to simply ignore the size). An issue in the prediction of the quality of monolithic 3-D ICs, however, is routing congestion. According to [29], monolithic 3-D ICs have serious routing congestion problems, so we should increase the die area, use more routing layers, or reduce the wire width to minimize the routing congestion. Increasing the die area is modeled by increasing the footprint area of a 3-D chip ($A_{3-\text{DFP}}$) in [1]. Using more routing layers can be modeled by increasing p in Rent's parameters because p is a measure of the interconnection complexity. Reducing the wire width can be modeled by decreasing p, but the unit resistance and capacitance of the wire in Table X should be adjusted accordingly.

VII. Conclusion

Unlike other 3-D wirelength distribution models, our TSV-aware 3-D wirelength distribution models predict wirelength distribution of 3-D ICs more accurately. In this paper, we applied dynamic-programming-based optimal buffer insertion to the models and predicted delay distribution and power consumption of 3-D ICs. Since process scaling has a big impact on the quality of integrated circuits, we cross-compared the quality of 2-D and 3-D ICs built with various technology combinations. Our TSV-aware prediction models consider the negative effects of TSVs, so they provide more accurate prediction results on the quality of 3-D ICs, thereby enabling early design space exploration for the design of 3-D ICs.

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