

Guest Editors' Introduction: Advances in 3-D Integrated Circuits, Systems, and CAD Tools—Part 2

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■ **THREE-DIMENSIONAL INTEGRATION**, a breakthrough technology to achieve “More Moore and More Than Moore,” provides numerous benefits such as better performance, lower power consumption, smaller form factor, and wider bandwidth than traditional 2-D integration technology. Three-dimensional stacking of heterogeneous silicon layers also enables heterogeneous 3-D integration. Thanks to the enormous efforts put into 3-D integration in academia and industry, a few 3-D products such as 3-D field-programmable gate array (FPGA) and through-silicon-via (TSV)-based dynamic random access memory (DRAM) have finally been commercialized in the semiconductor market. Commercialization of more diverse 3-D integrated circuit (IC) products, however, still requires novel solutions for various challenging issues such as effective heat removal and lack of standards, applications, and computer-aided design (CAD) tools for design, analysis, and optimization of 3-D ICs.

The Special Issue on Advances in 3-D Integrated Circuits, Systems, and CAD Tools, published in *IEEE Design & Test* in July/August 2015 introduced seven papers to highlight recent research on 3-D integration. The papers covered a wide range of topics on 3-D ICs from 3-D IC manufacturing

process and 3-D integration technology to thermal analysis, 3-D design-for-test architectures, 3-D integration of memory and logic, test methodologies for 3-D ICs, and 3-D memory architectures. As a second part of the Special Issue on Advances in 3-D Integrated Circuits, Systems, and CAD Tools, this special issue presents four more papers that highlight recent advances in test methodologies for 3-D interconnects, modeling of TSVs and TSV channels, memory architecture optimization for 3-D stacked DRAM, and codesign of 3-D CPUs and microfluidic pin-fin cooling structures.

“Delay Characterization and Testing of Arbitrary Multiple-Pin Interconnects” by Huang et al., proposes a test methodology to detect delay faults in multipin interconnects in 3-D ICs with 10-ps resolution. The idea is to insert a multiplexer for each pitcher cell driving a 3-D interconnect and a multiplexer for each receiver cell so that a global ring structure is formed to test each 3-D interconnect. The authors also present a clock period measurement circuit to achieve a measurement accuracy of 10 ps.

“High-Frequency Temperature-Dependent Through-Silicon-Via (TSV) Model and High-Speed Channel Performance for 3-D ICs” by Lee et al., presents high-frequency temperature-dependent RLGC models for TSVs and TSV channels. The authors verify the models against measurement data and show the impact of temperature variation on noise coupling between two neighboring TSVs and between two neighboring TSV channels.

Digital Object Identifier 10.1109/MDAT.2016.2519718

Date of current version: 25 February 2016.

“Configurable Cubical Redundancy Schemes for Channel-Based 3-D DRAM Yield Improvement” by Lin et al., proposes two memory redundancy schemes to improve the yield of channel-based 3-D stacked DRAM. The first scheme uses DRAM for global redundancy, whereas the second scheme uses SRAM in a logic die for global redundancy. Simulation results show that the proposed schemes significantly outperform other redundancy architectures.

“Thermoelectric Codesign of 3-D CPUs and Embedded Microfluidic Pin-Fin Heatsinks” by Serafy et al., presents a simulation framework for design space exploration and optimization of 3-D CPUs with microfluidic pin-fin cooling. Determination of design variables such as pin diameter and pin pitch in a pin-fin structure has a significant impact on the cooling capacity and the performance of the 3-D CPU, so the authors obtain optimal designs by exhaustive simulation of all combinations of the design variables. This thermoelectric codesign approach outperforms optimizing only the cooling capacity or the performance.

We truly enjoyed working as the guest editors of this special issue. We are very grateful to the authors for their contributions and the reviewers for their time, insightful comments, and dedication to this special issue. We express our thanks to Prof. Jörg Henkel, the Editor-in-Chief of *IEEE Design & Test*, and Prof. André Ivanov, the past Editor-in-Chief of *IEEE Design & Test*, for helping us create this special issue. We would also like to thank Prof. Partha Pande, the Associate Editor-in-Chief of *IEEE Design & Test*, for his extensive help in the preparation, processing, and publication of this special issue. We also thank the editorial staffs of the IEEE Computer Society for their editing and assembling of this special issue. ■

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