EE 582
Physical Design Automation of VLSI Circuits and Systems

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Washington State University

Course Information

WASHINGTON STATE UNIVERSITY

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Course Information

- Instructor: Prof. Dae Hyun Kim
- Office: EME 504
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- Class room: Thompson Hall 105
- Class time: T/Th 12pm – 1:15pm
- Office hours: T/Th 1:30pm – 3pm
  - or by appointment

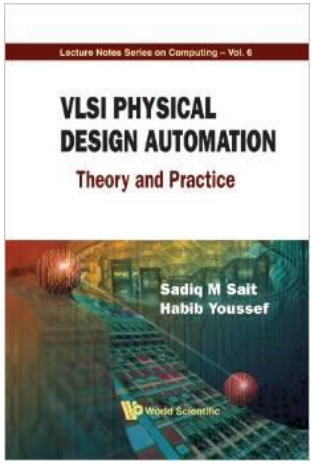
- Class webpage
  - http://daehyunkim.net/EE582

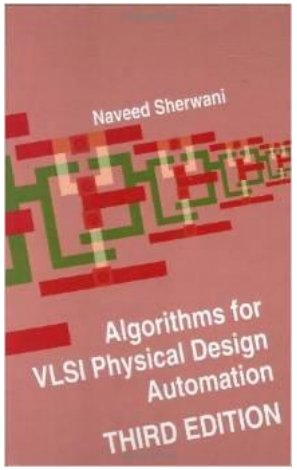
Course Information

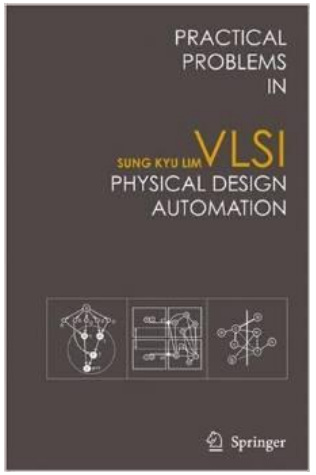
- No official prerequisites.
- Students are expected to have some knowledge of
  - Logic circuits (EE 214)
  - Linear circuit analysis (EE 261)
  - Digital system design (EE 324)
  - VLSI (EE 434 / EE 466)
  - C/C++ programming
    - Structural programming / OOP / pointer handling
  - Data structures and algorithms (CptS 122 / CptS 450)

Course Information

- Textbook
  - No required textbook.
- Recommended
  - VLSI Physical Design Automation: Theory and Practice, Sadiq M. Sait, Wspc, 1999 ($70 / $14)
  - Algorithms for VLSI Physical Design Automation, 3/E, Naveed Sherwani, Springer, 1998 ($100 / $3)
  - Practical Problems in VLSI Physical Design Automation, Sung Kyu Lim, Springer, 2008 ($127 / $32)







Course Information

- Grading
  - Assignments (#: 20~25): 40%
  - Midterm exam 1: 20%
  - Midterm exam 2: 20%
  - Final exam: 20%

- Asking for
  - Comments and feedback on my teaching

You Should Take This Course If You

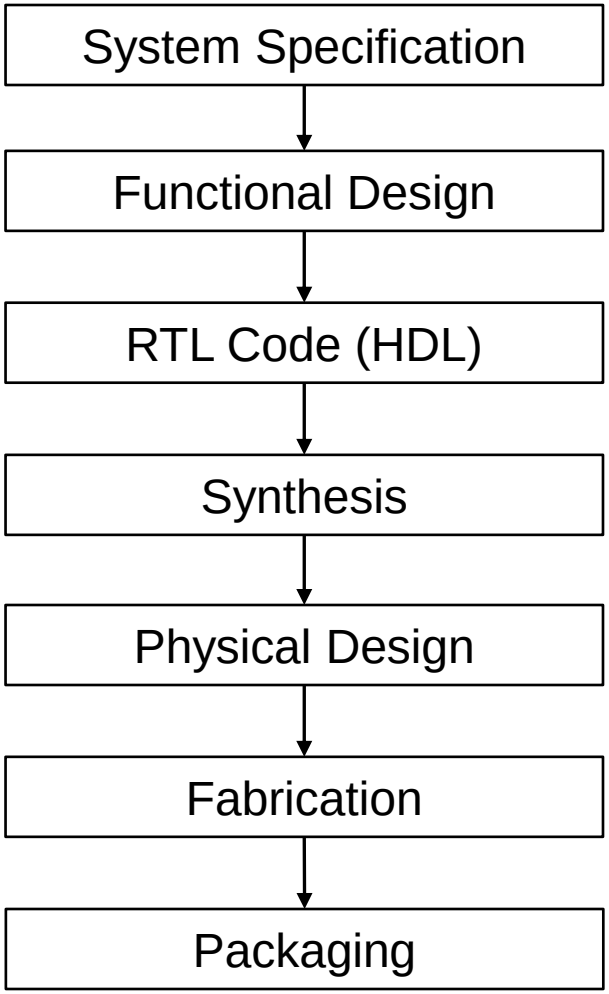
- want to learn how to design digital VLSI layouts.
- are interested in joining chip vendors such as Qualcomm, Apple, Intel, Samsung, … as a chip designer, CAD engineer, product engineer, etc.
- are interested in CAD.
- want to join CAD companies such as Cadence, Synopsys, Mentor Graphics, …
- want to become a VLSI expert.
- are interested in joining my lab.

What we will study

- Physical design automation algorithms for the design of VLSI circuits and systems.

- Questions
  - What is “physical design”?
  - What is “design automation”?

VLSI Design



Freq Area Power

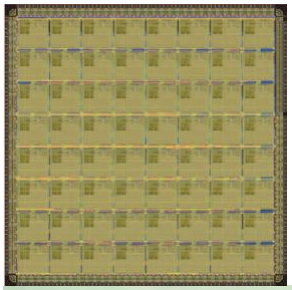
64-bit integer multiplier / 1GHz / 0.1mm^2 / 0.1mW

C/C++, Verilog, VHDL, …

```
module imul_64 (a, b, clk, out64);
input a, b, clk;  output out64; … endmodule
```

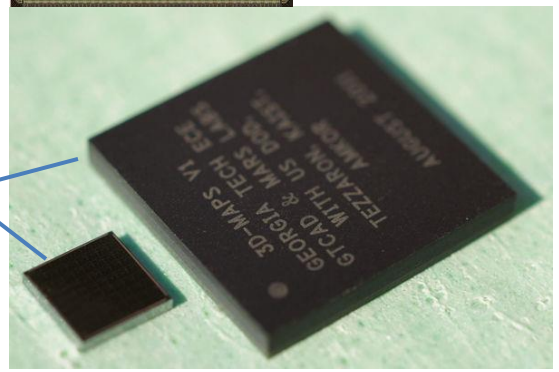
Netlist

Layout



Bare die

Chip

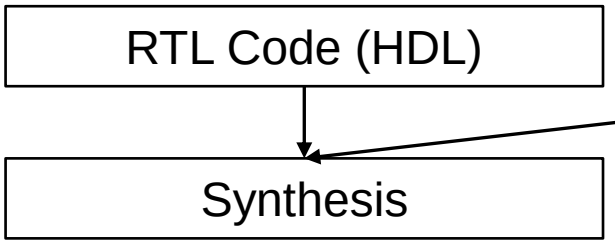


From RTL Code to a Chip

RTL Code (HDL)

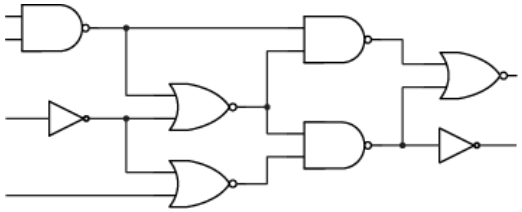
```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  reg [63:0] int_stage1;
  reg [63:0] int_stage2;

  always @ (posedge clk)
  begin
    ...
  end

endmodule
```

From RTL Code to a Chip



Tech library
(e.g., 45nm)

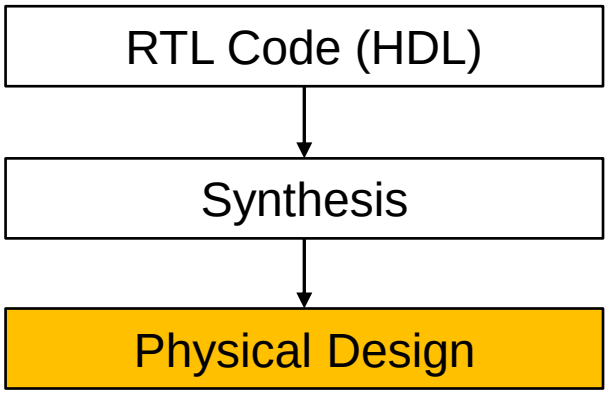
```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  reg [63:0] int_stage1;
  reg [63:0] int_stage2;

  always @ (posedge clk)
  begin
    ...
  end

endmodule
```

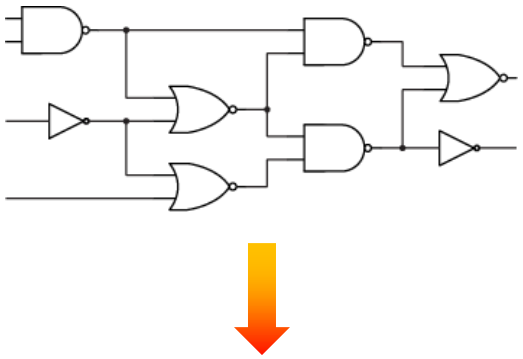


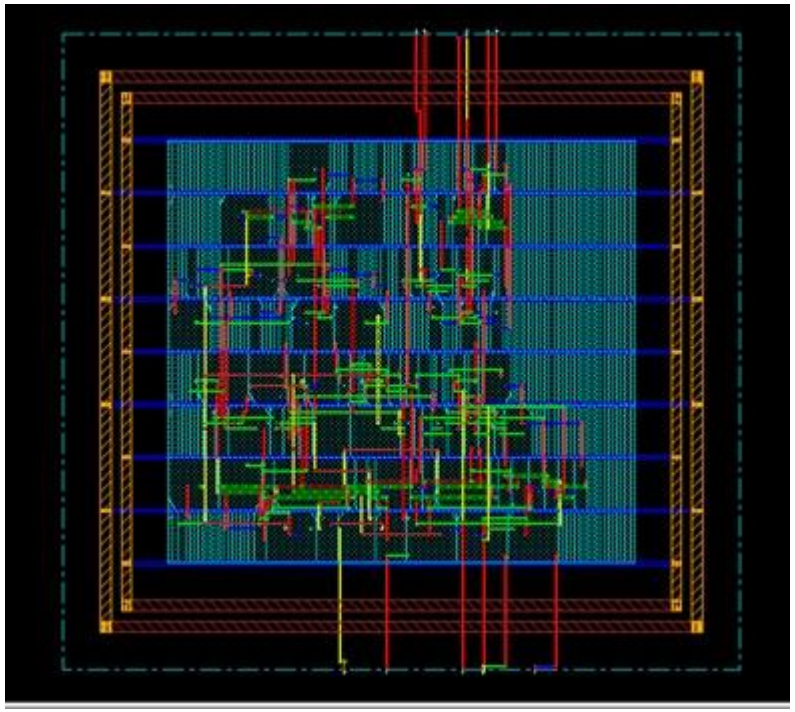
Tech-specific logic gates

```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  NAND2_X1 ( .A(in_1[0]), .B(in_2[0]), .Z(n1) );
  FA_X1 ( .A(in_1[0]), .B(in_2[0]), .CI(1'b0), .S(n2), .CO(n3) );
  ...

endmodule
```

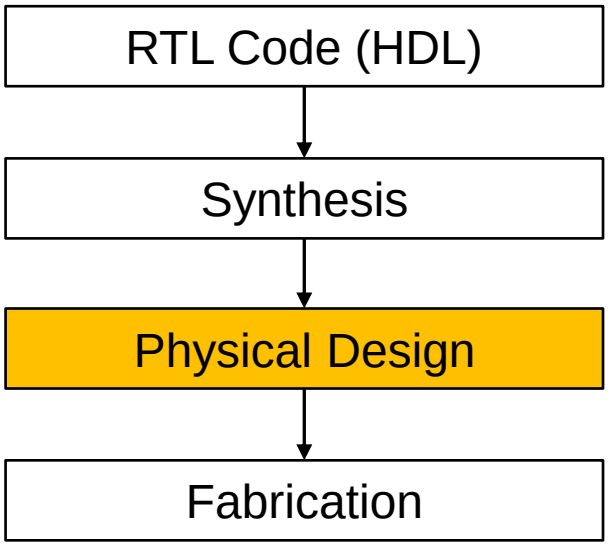
From RTL Code to a Chip

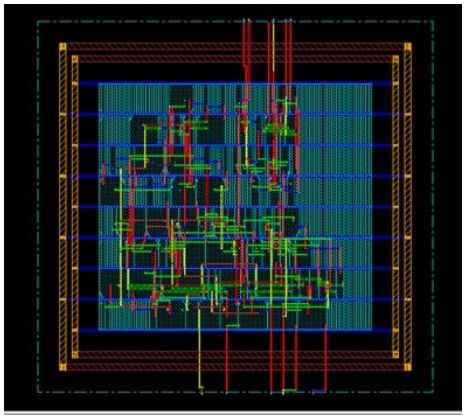


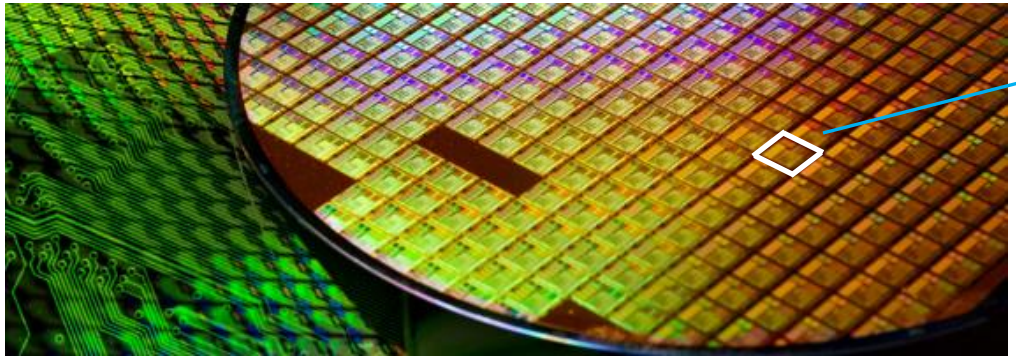


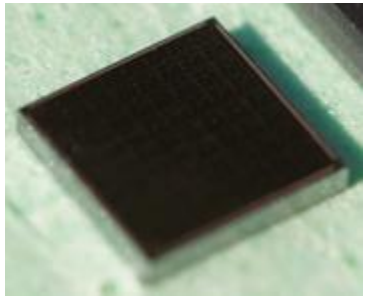


From RTL Code to a Chip

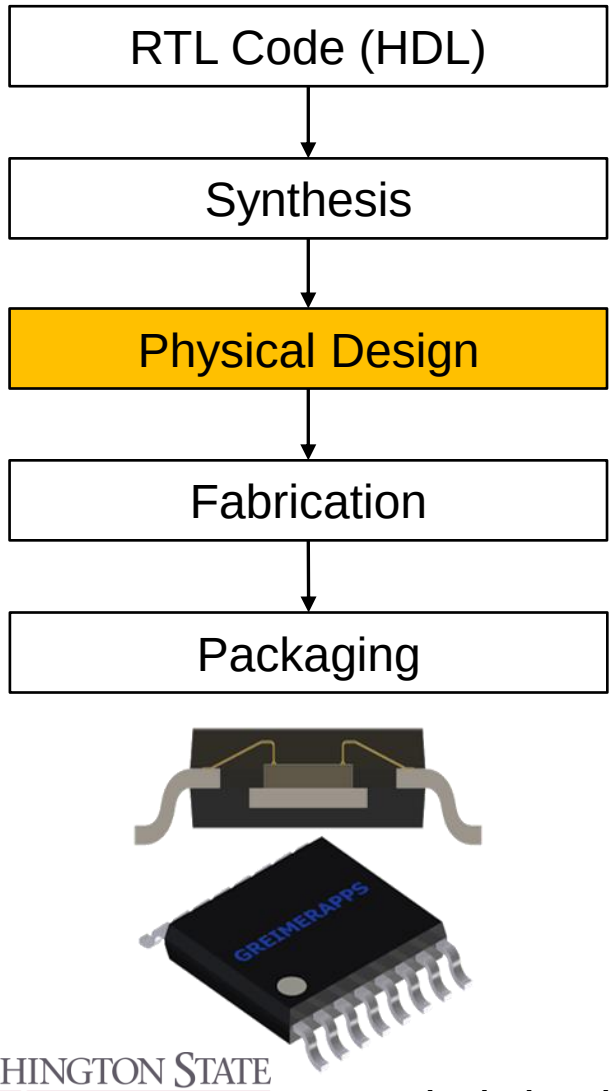


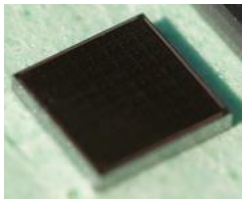


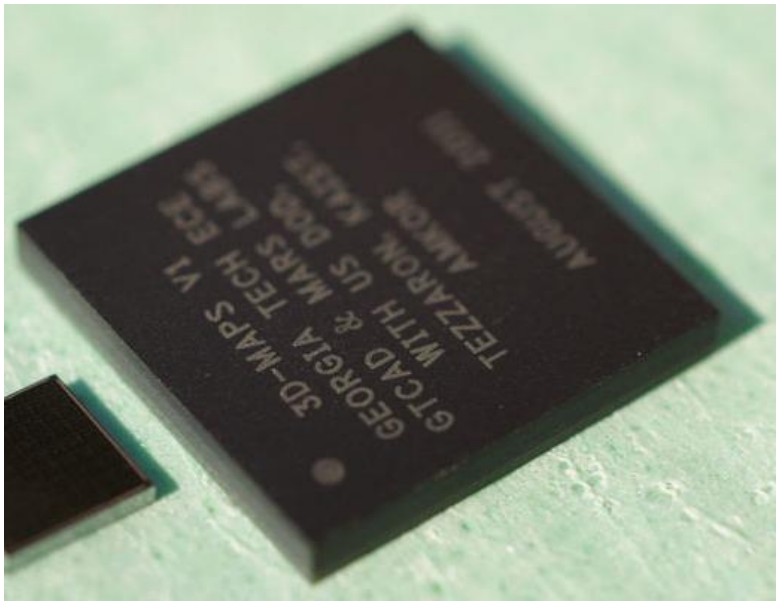




From RTL Code to a Chip

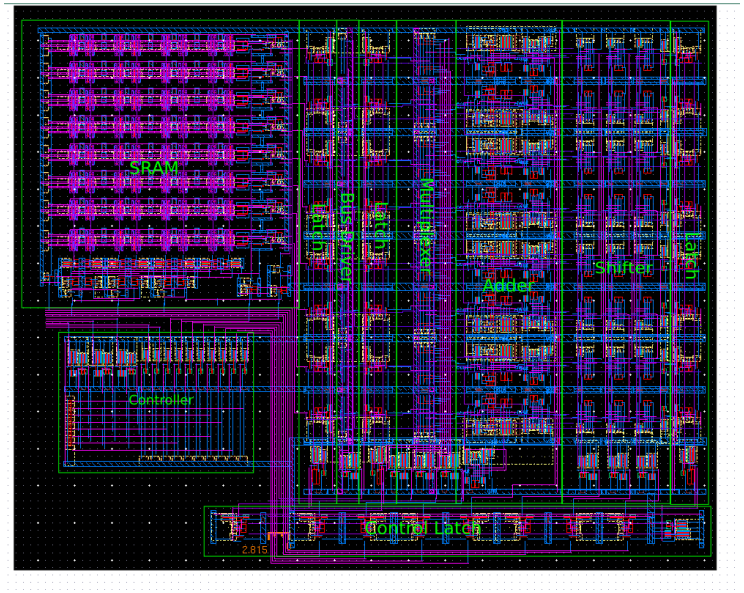


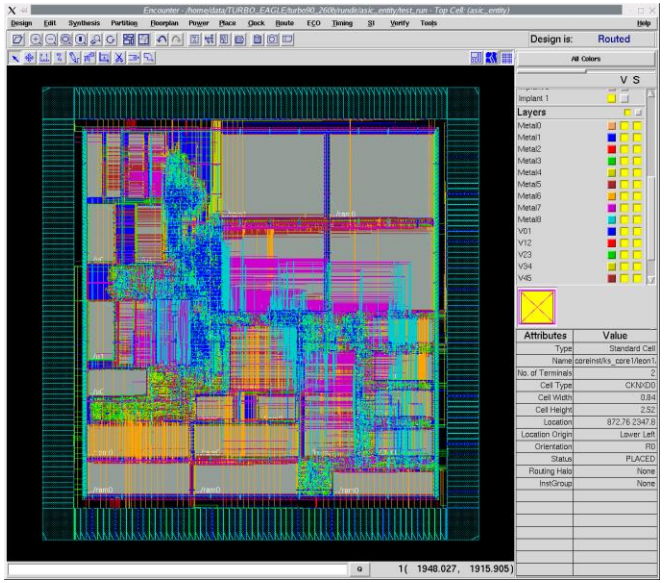




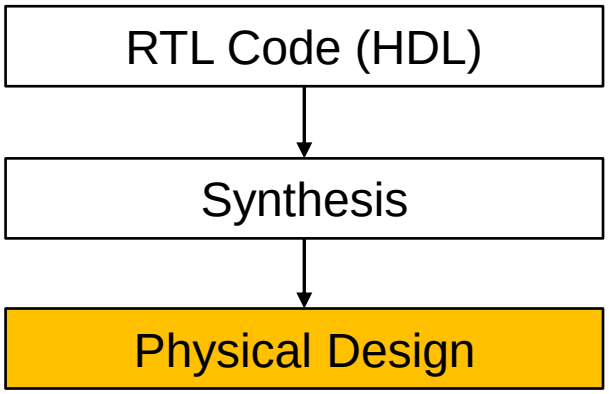
VLSI Design

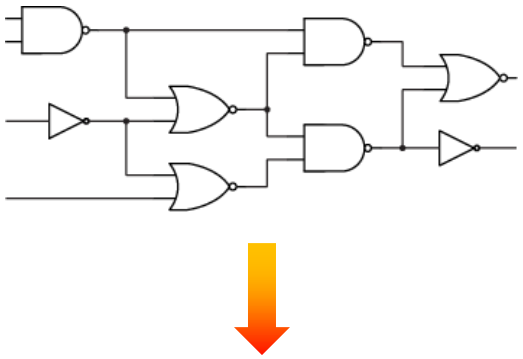
	Full custom	ASIC
Design	Manual	Automatic
TRs	Manually drawn	Standard-cell based
Placement & Routing	Custom	Automatic
Development time	Several months	A few days ~ weeks

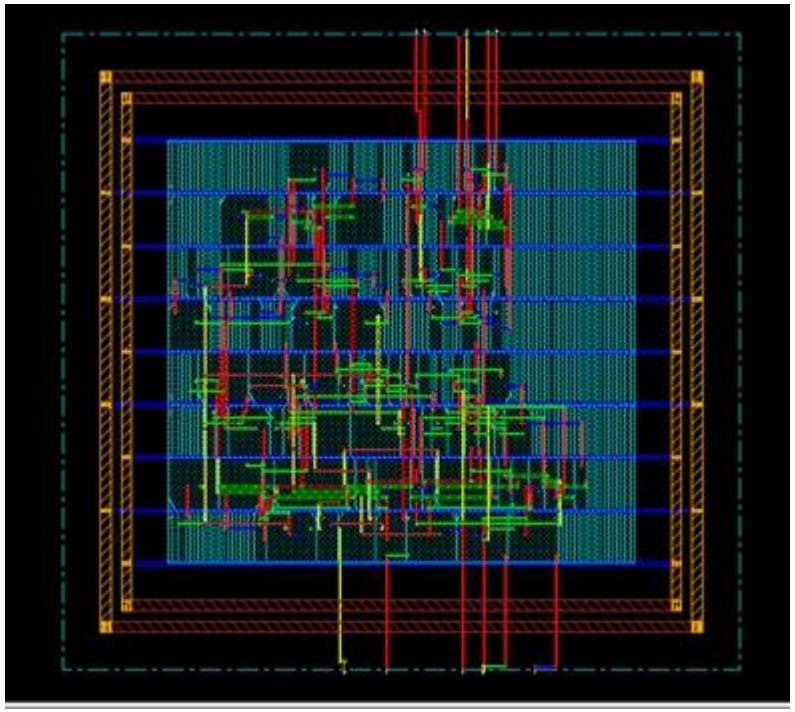




What is Done in the Physical Design







Netlist → Physical layout

Standard-Cell-Based Design

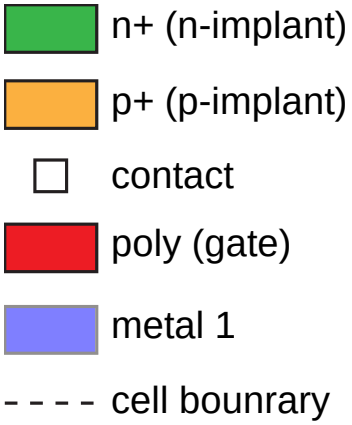
- Provides
  - good performance
  - low power
  - small area
  - …
- Other design styles
  - FPGA
  - PLA
  - …

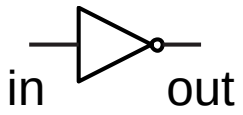
Standard-Cell-Based Design

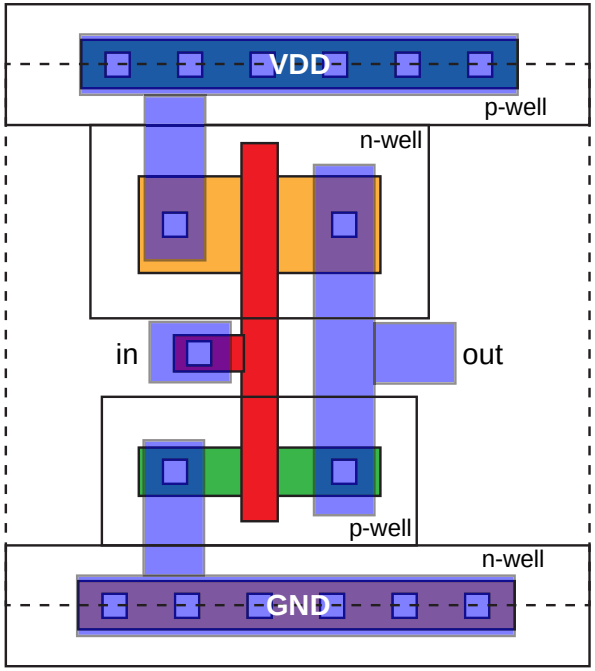
- Standard cells
  - A set of logic gates
  - Have the same height.
  - Width varies.
  - Pre-characterized for timing and power analysis.

INV NAND2

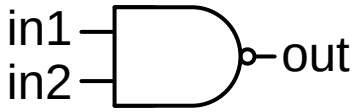
Standard Cells (Layout)

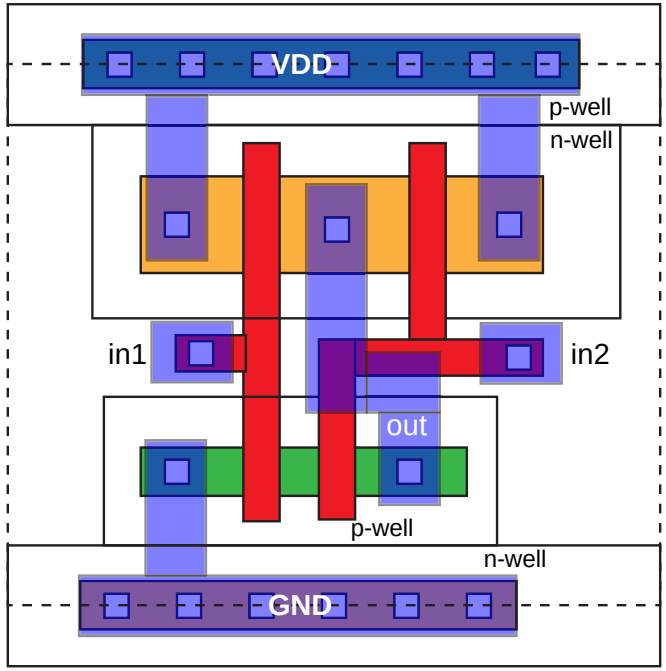






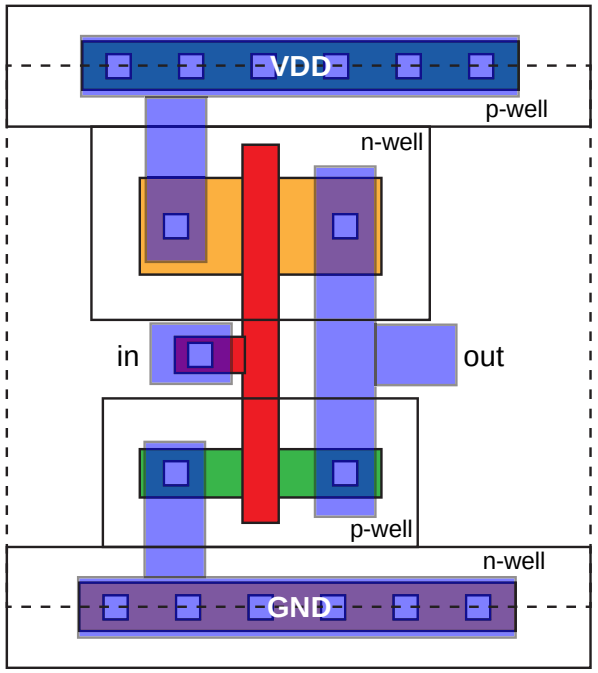
INV



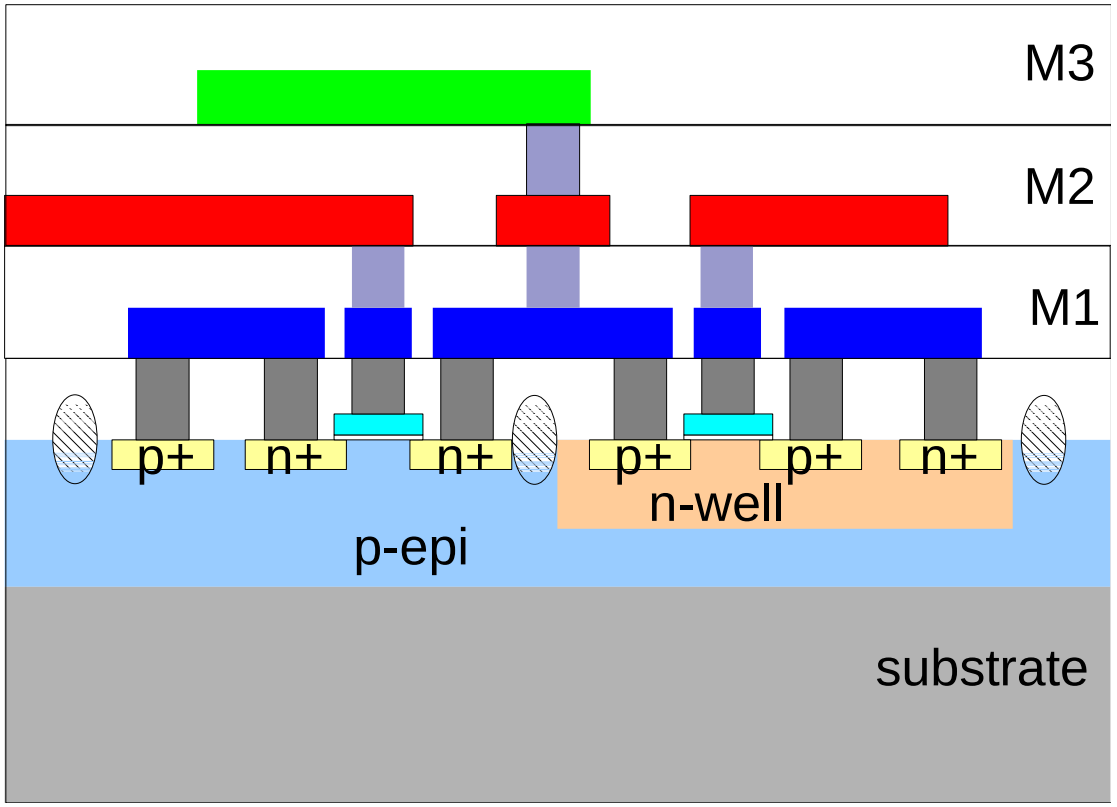


NAND2

Standard Cells (Layout)

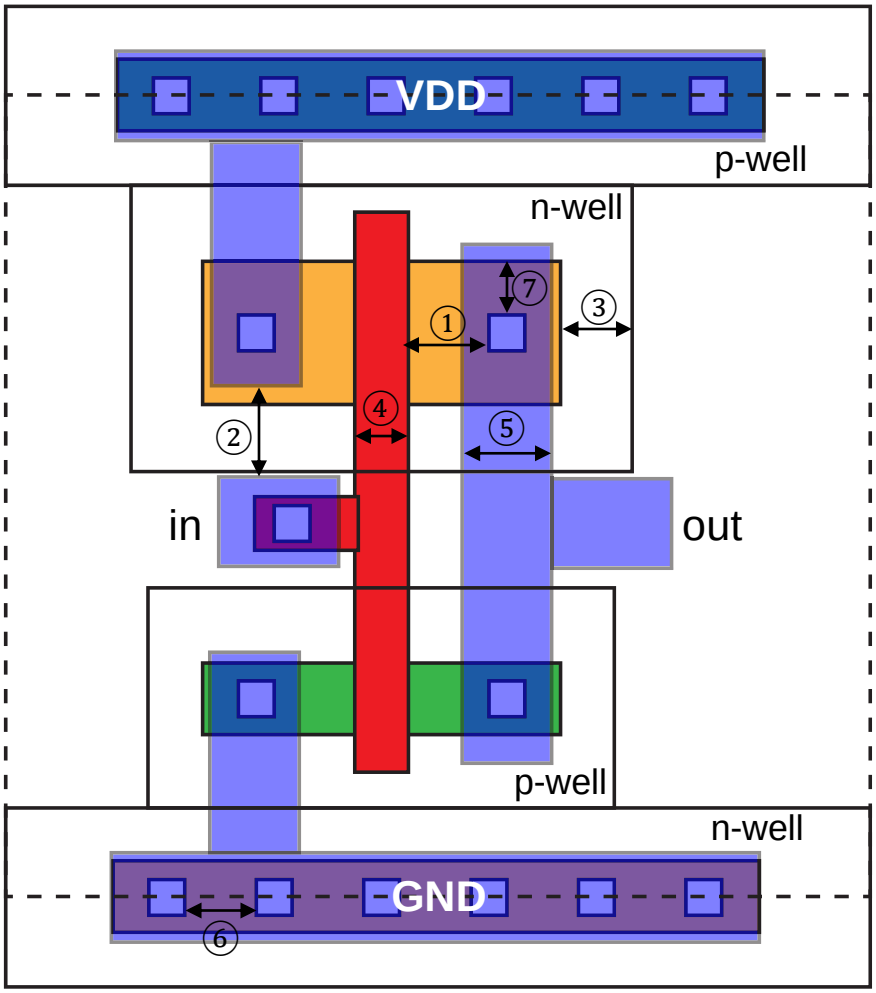


Top-down view



Side view

Design Rules



①: Min. distance (poly, contact)

②: Min. distance (metal 1)

③: Min. distance (p-active, n-well boundary)

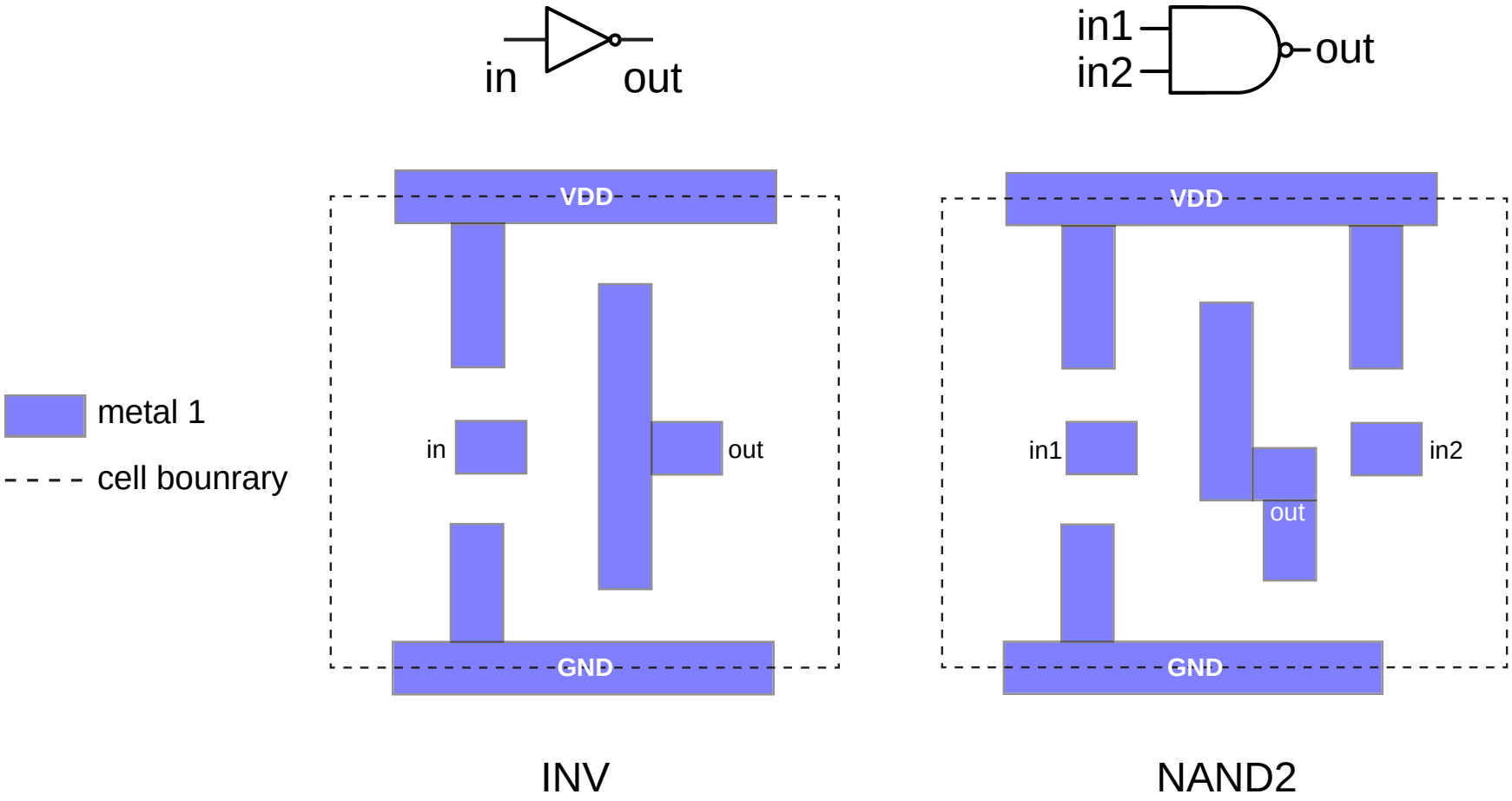
④: Min. width (poly)

⑤: Min. width (metal 1)

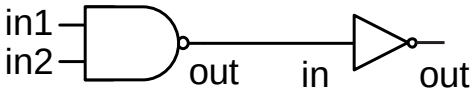
⑥: Min. distance (contact)

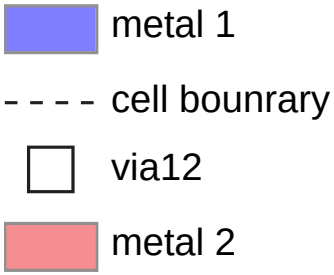
⑦: Min. distance (contact, n-well bounrary)

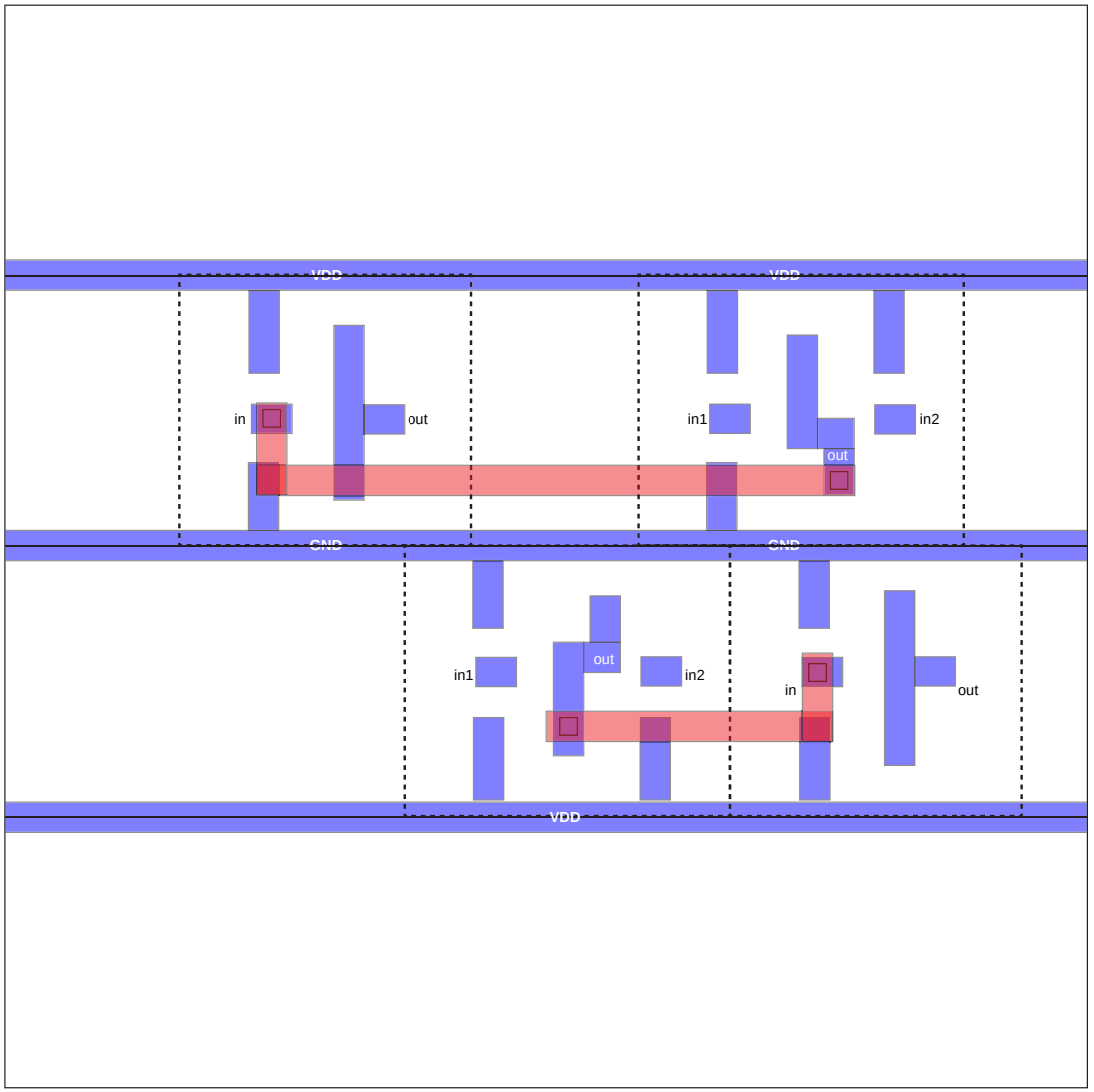
Standard Cells (Abstract)



Standard-Cell-Based Design

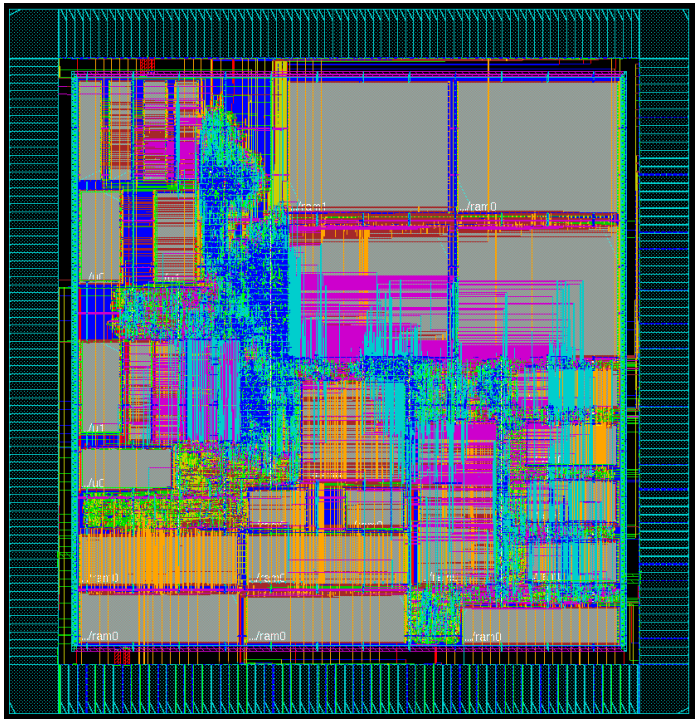






Standard-Cell-Based Design

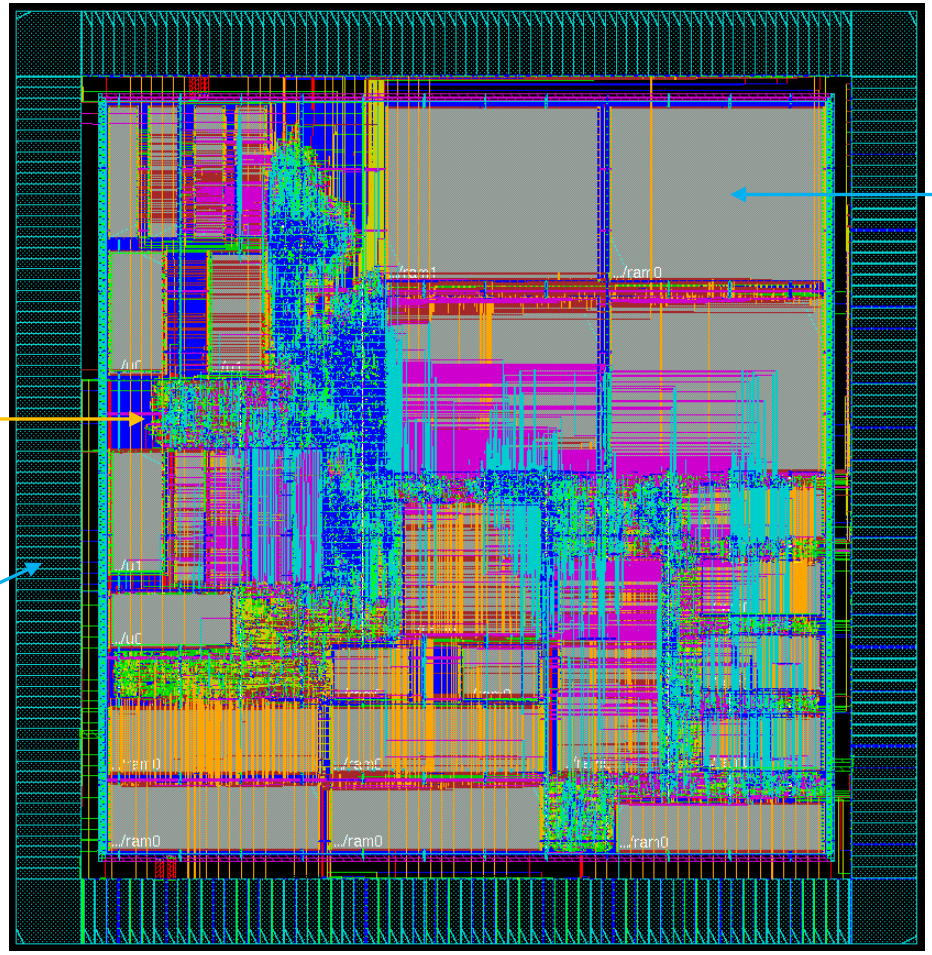
- Deal with
  - Standard cells (pre-drawn and pre-characterized)
  - Routing layers (M1, via12, M2, via23, …)



Standard-Cell-Based Design

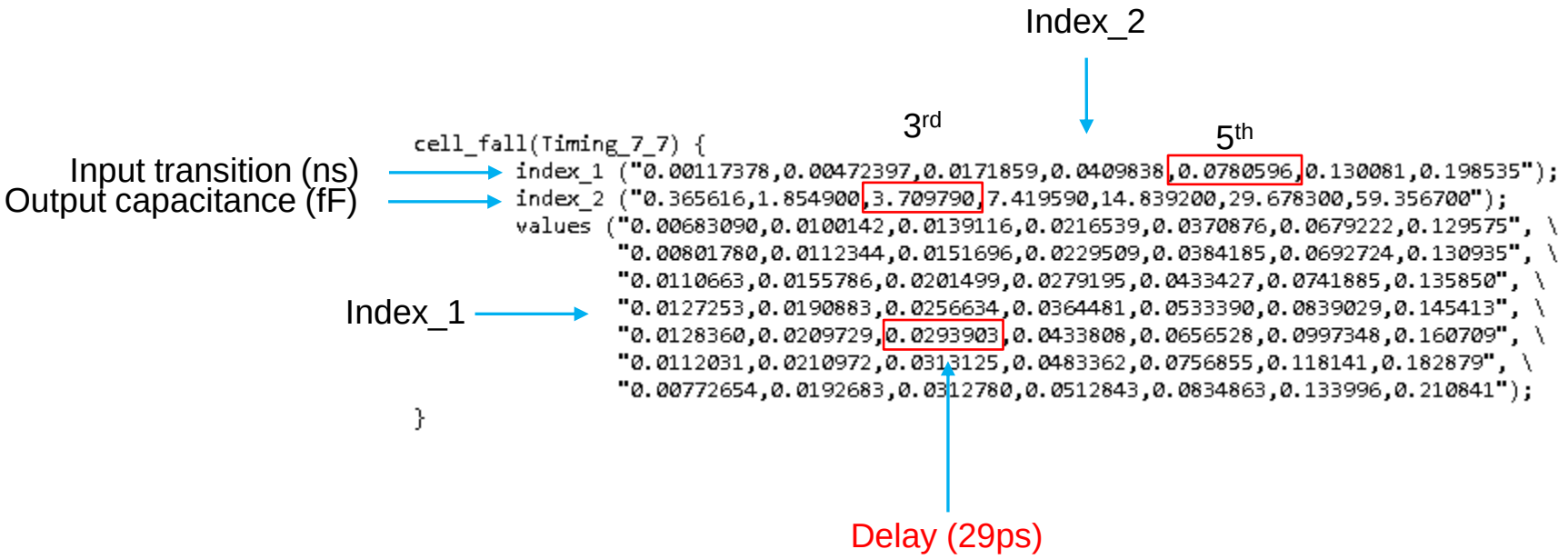
- Intellectual Property (IP) blocks
  - Pre-created blocks
    - Memory
    - Arithmetic
    - Cryptographic
    - DSP
    - Controller
    - …

Standard-Cell-Based Design



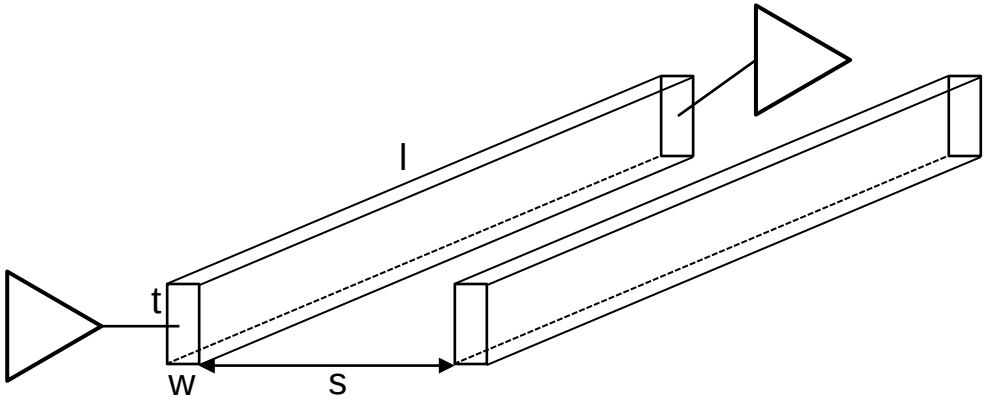
Delay Calculation & Timing Analysis

- Pre-characterized cells

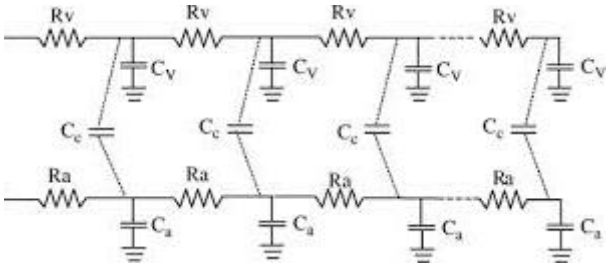


Delay Calculation

- Interconnect delay

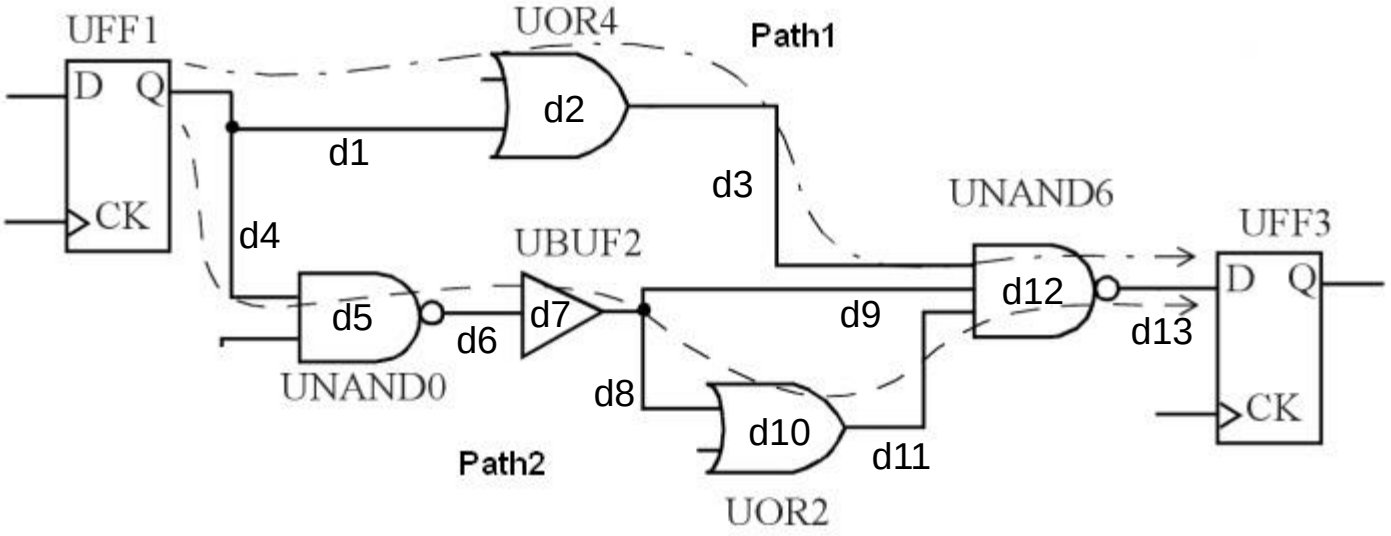


modeling



$$R = \rho \frac{l}{t \cdot w} \qquad C = \epsilon \frac{t \cdot l}{s} \qquad Delay \propto RC \propto l^2$$

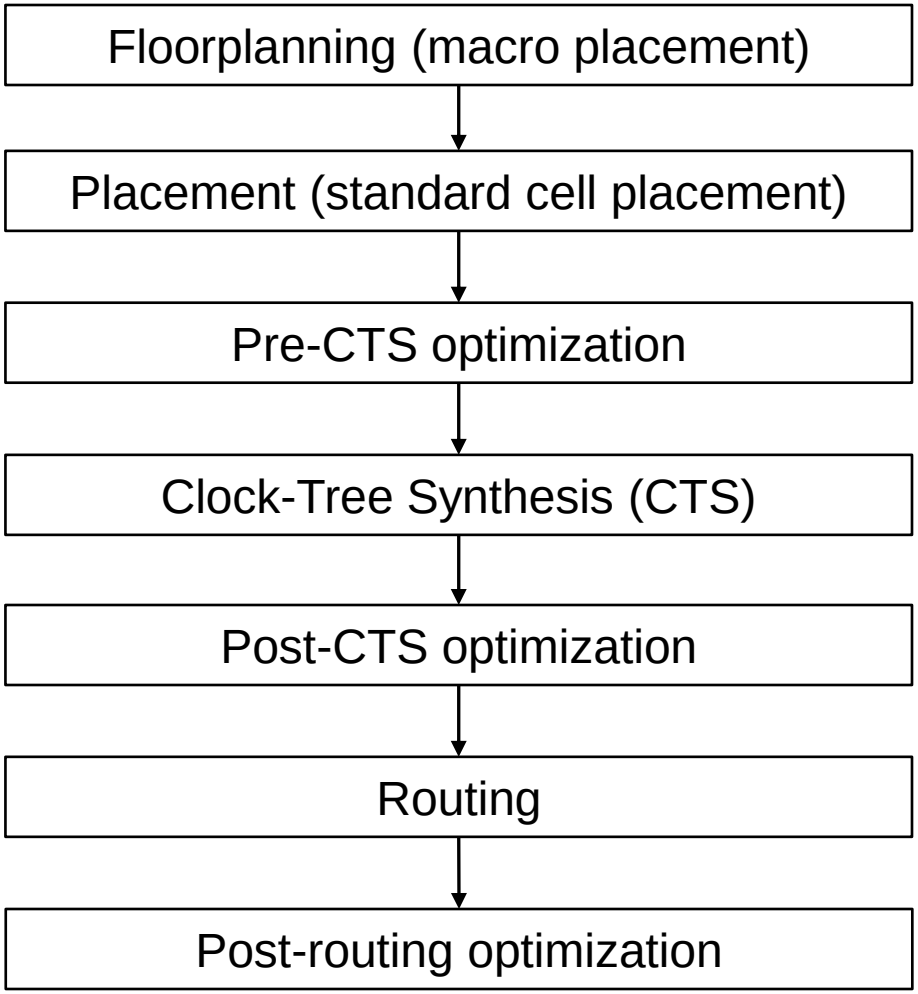
Timing Analysis



Standard-Cell-Based Design

- What should we do?
  - Find the locations of the macros.
  - Find the locations of the standard cells.
  - Route the macros and the standard cells.
    - Power/ground
    - Signal
    - Clock
    - Bus
  - Extract parasitic RC.
  - Analyze the final layout.
    - Timing (clock frequency)
    - Power consumption (dynamic / leakage)
    - Area
    - Power integrity
    - Signal integrity
    - Thermal

Standard-Cell-Based Design



What You Need to Know

- VLSI
- Graph theory
- Linear optimization
- Non-linear optimization
- Computational geometry
- Data structure and algorithms
- Programming
- …

My Research Lab

- Lab
  - CADETS (**CAD** for **E**merging **T**echnologies and **S**ystems)

- Research
  - Design and analysis of VLSI circuits and systems using emerging technologies
    - 3D ICs, CNT transistors/interconnects, nanowire transistors/interconnects, …
    - Design methodologies, techniques, optimization algorithms
    - Applications for ultra-low-power, energy-efficient, high-performance VLSI circuits and systems

CAD / EDA Conferences & Journals

- Conferences
  - Asia and South Pacific Design Automation Conference (ASPDAC)
  - Design Automation Conference (DAC)
  - Design, Automation & Test in Europe (DATE)
  - International Conference on Computer-Aided Design (ICCAD)
  - International Symposium on Physical Design (ISPD)

- Journals
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
  - ACM Transactions on Design Automation of Electronic Systems (TODAES)
  - IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)