EE434
ASIC & Digital Systems

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Lecture 2

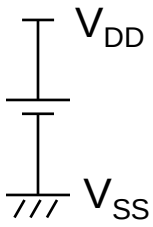
Introduction to CMOS Gates

Ref: Textbook chapter 2

Some of the slides are adopted from Digital Integrated Circuits by Jan M Rabaey

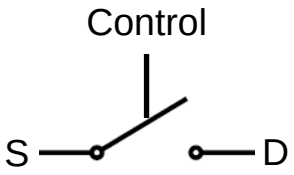
Signals

- 0 = V_{SS} = Ground = GND = Low = 0V
- 1 = V_{DD} = Power = PWR = High = 5V, 3.3V, 1.5V, 1.2V, 1.0V

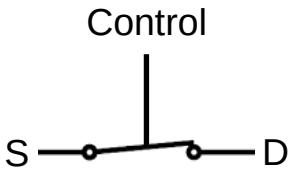


Switches

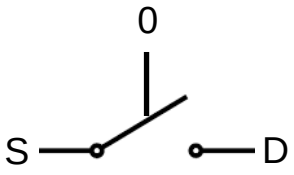
- What is a switch?



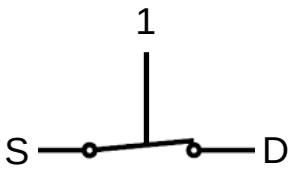
Electrically open



Electrically short



Electrically open

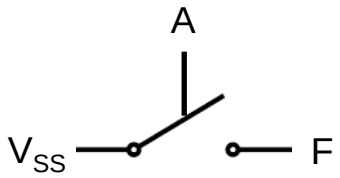


Electrically short

Switches

- Function

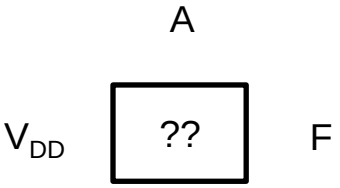
  F = $\bar{A}$ (inverter)



A	
0	1
1	0

- Two issues

  1.



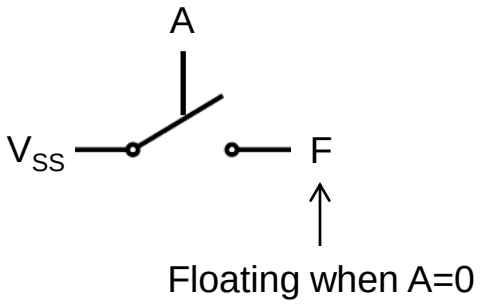
A	
0	1
1	0

  2. Electrical modeling of the operation

Static CMOS Circuit

- At every point in time (except during the switching transients), each gate output is connected to either V_{DD} or V_{SS} via a low-resistive path.

- The outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring the transient effects during switching periods).



Switches

- Two types of switches

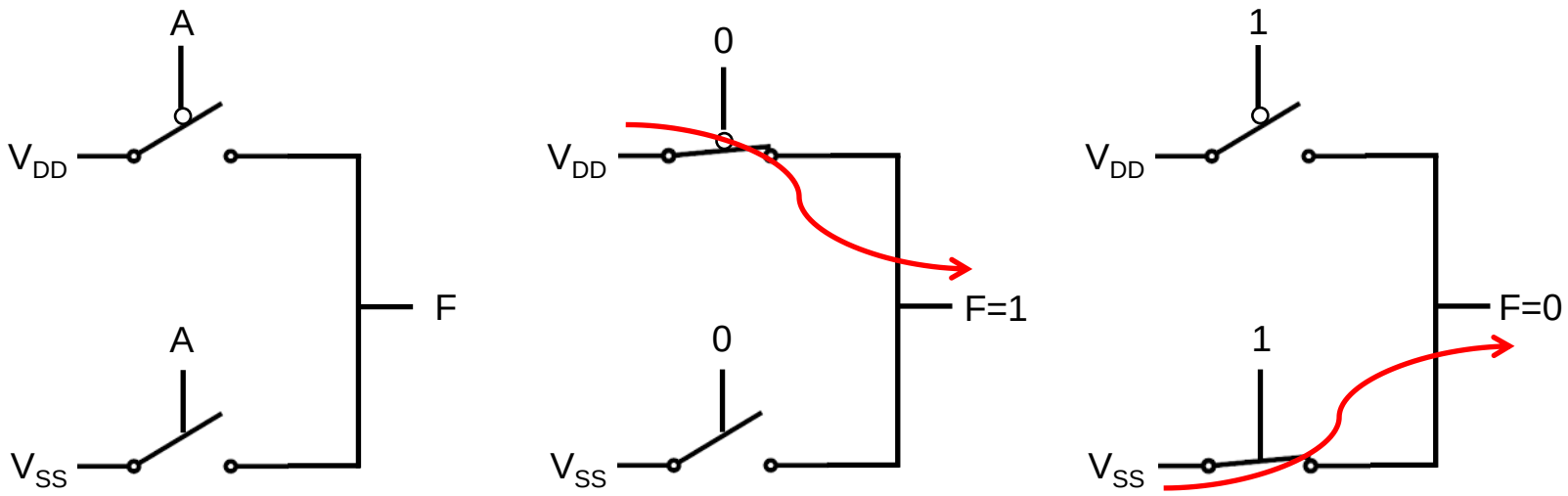
Normally open

Normally closed

Switches

- Function

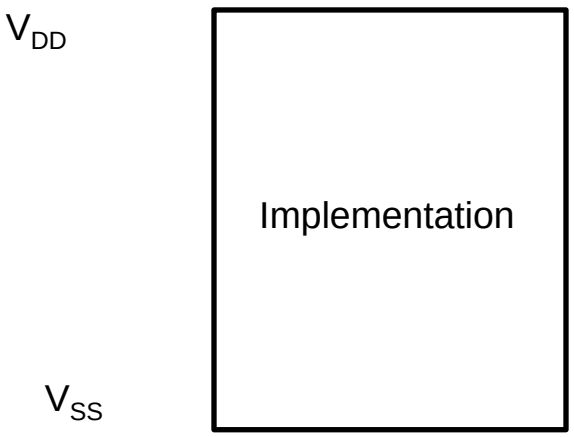
  F = $\bar{A}$ (inverter)



Switches

- Function

  F = $\overline{A \cdot B}$

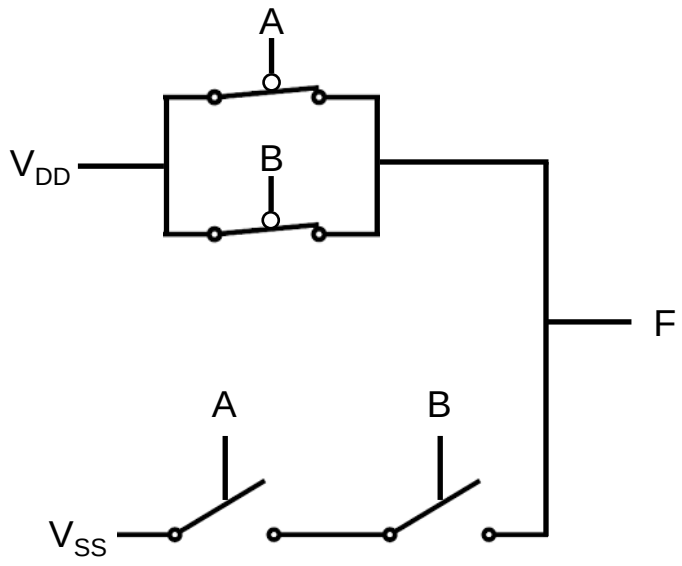


B \ A	0	1
0	1	1
1	1	0

Switches

- Function

  F = $\overline{A \cdot B}$



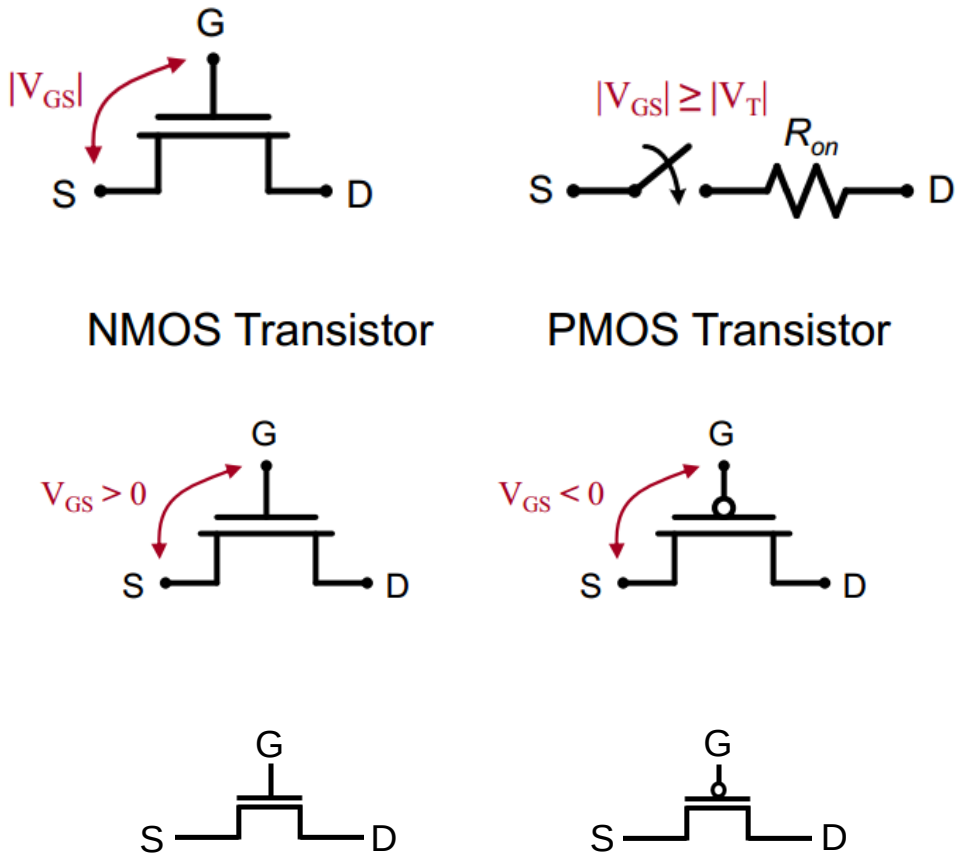
B \ A	0	1
0	1	1
1	1	0

Example

- $F = \overline{A + B}$ (NOR2)
- $F = \overline{A + B + C}$ (NOR3)

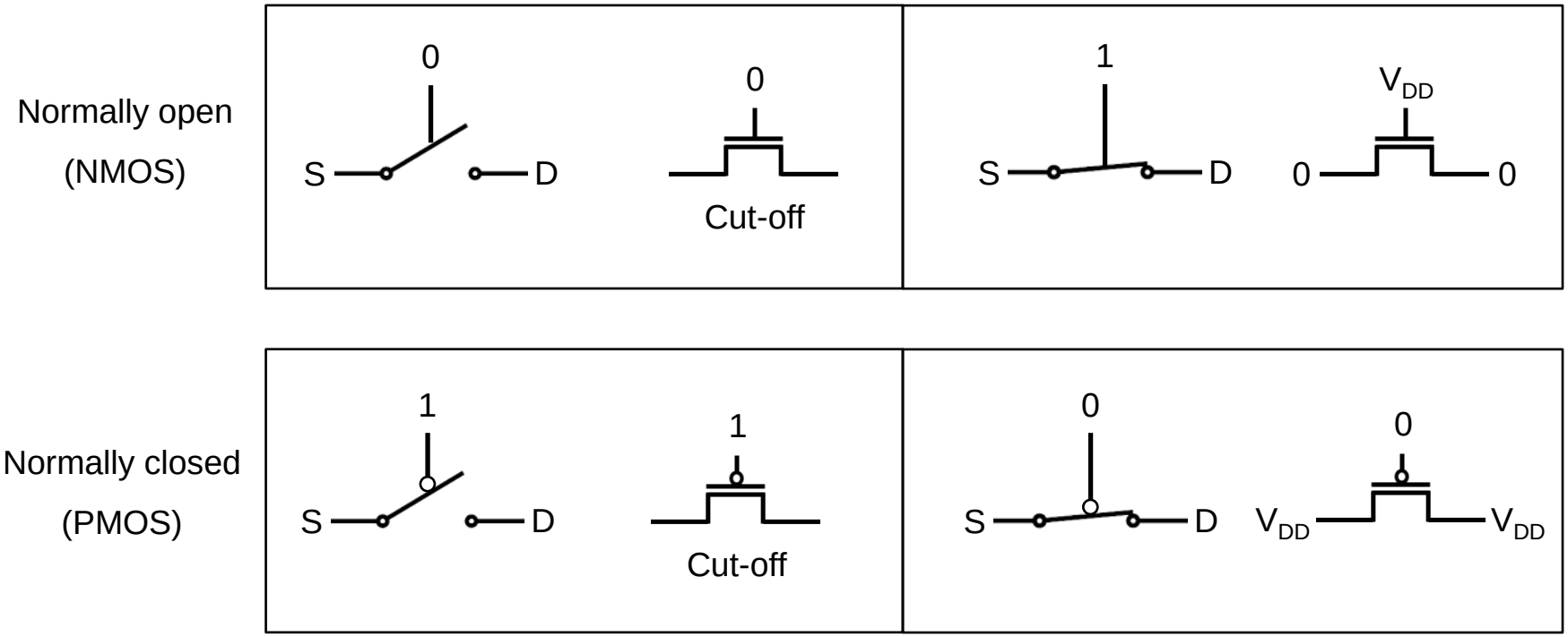
Transistors as Switches

- NMOS and PMOS



Transistors as Switches

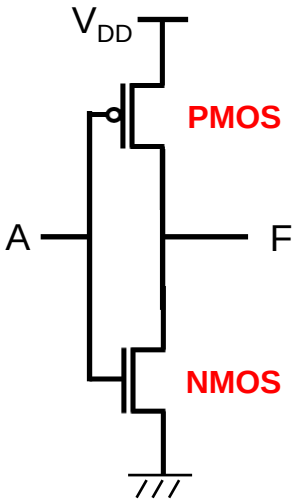
- NMOS and PMOS



CMOS Gates

- Function

  F = $\bar{A}$

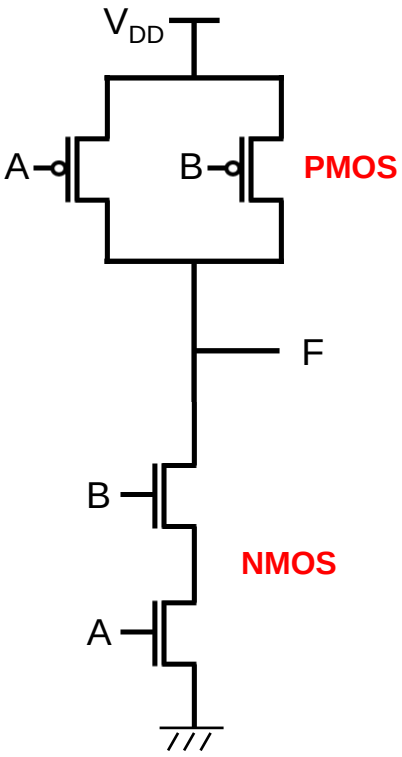


A	
0	1
1	0

CMOS Gates

- Function

  $F = \overline{A \cdot B}$

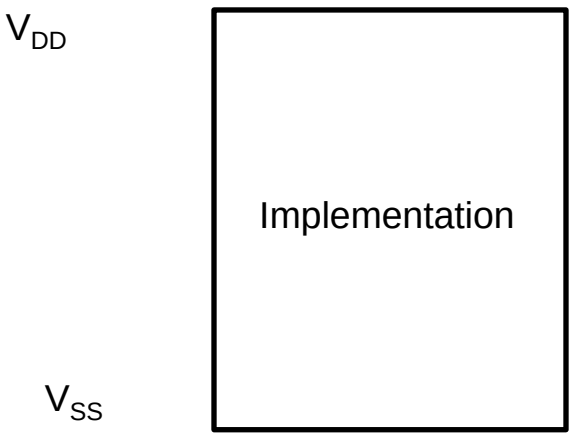


B \ A	0	1
0	1	1
1	1	0

CMOS Gates

- Function

  F = $A \cdot B$



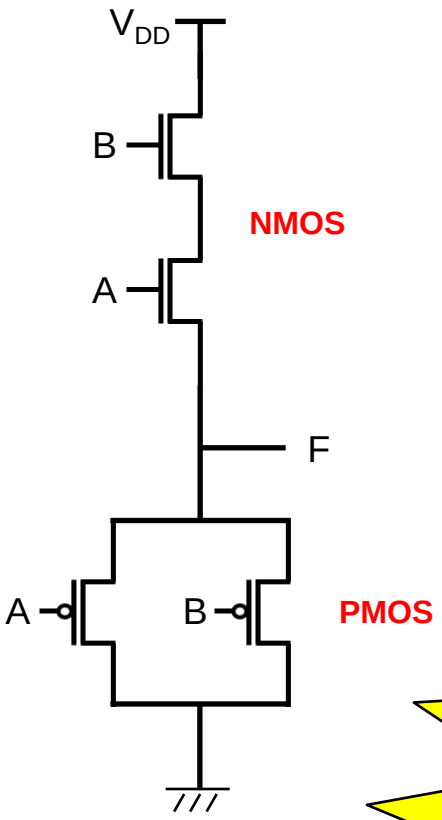
F

B \ A	0	1
0	0	0
1	0	1

CMOS Gates

- Function

  F = $A \cdot B$



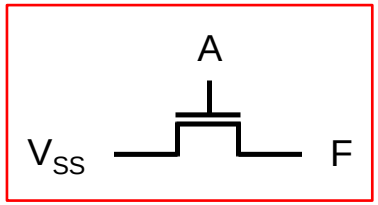
B \ A	0	1
0	0	0
1	0	1

This is not a good design.

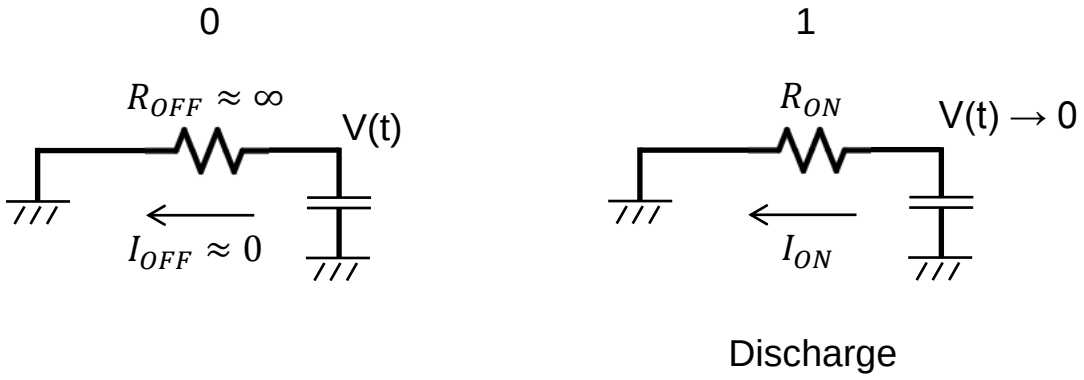
Why?

Electrical Modeling

- Ideal switch

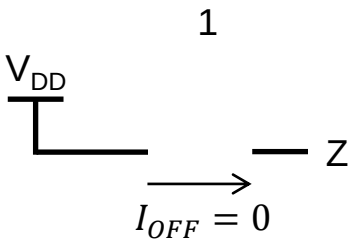


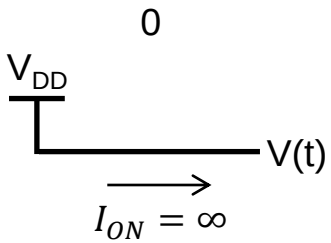
- Real switch

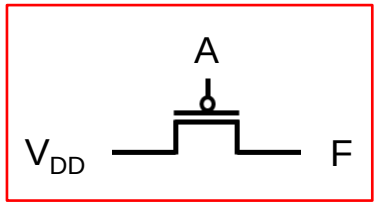


Electrical Modeling

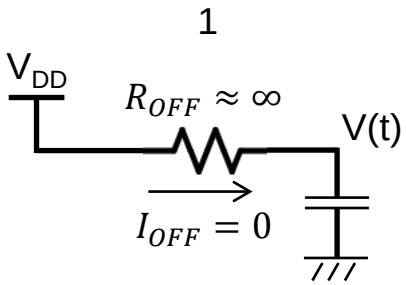
- Ideal switch

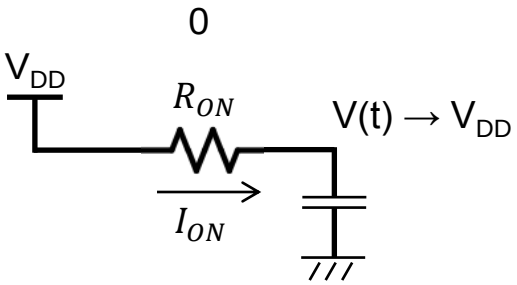






- Real switch

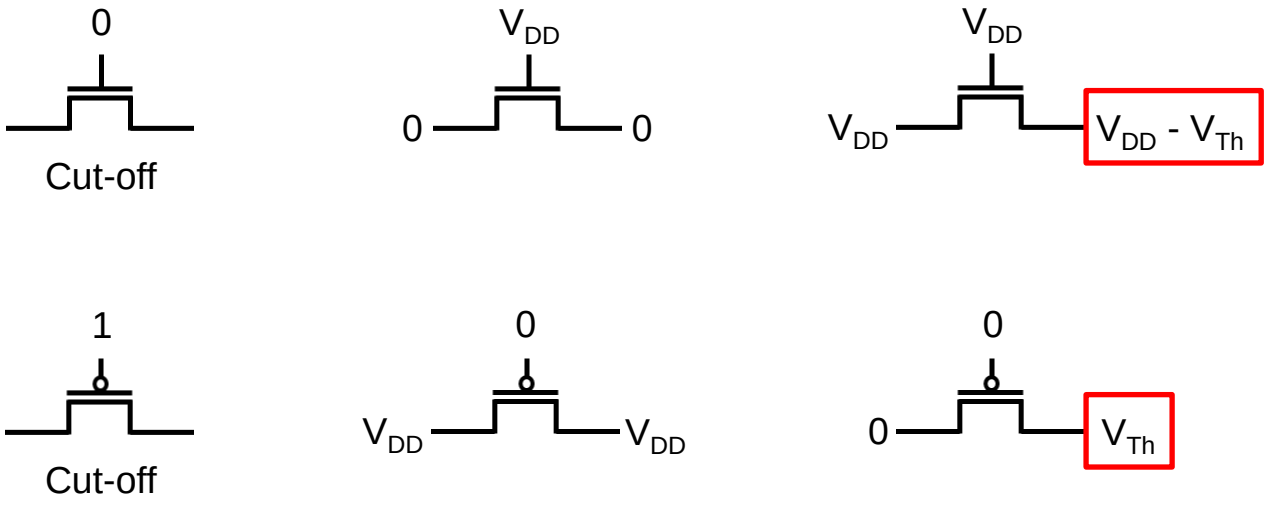




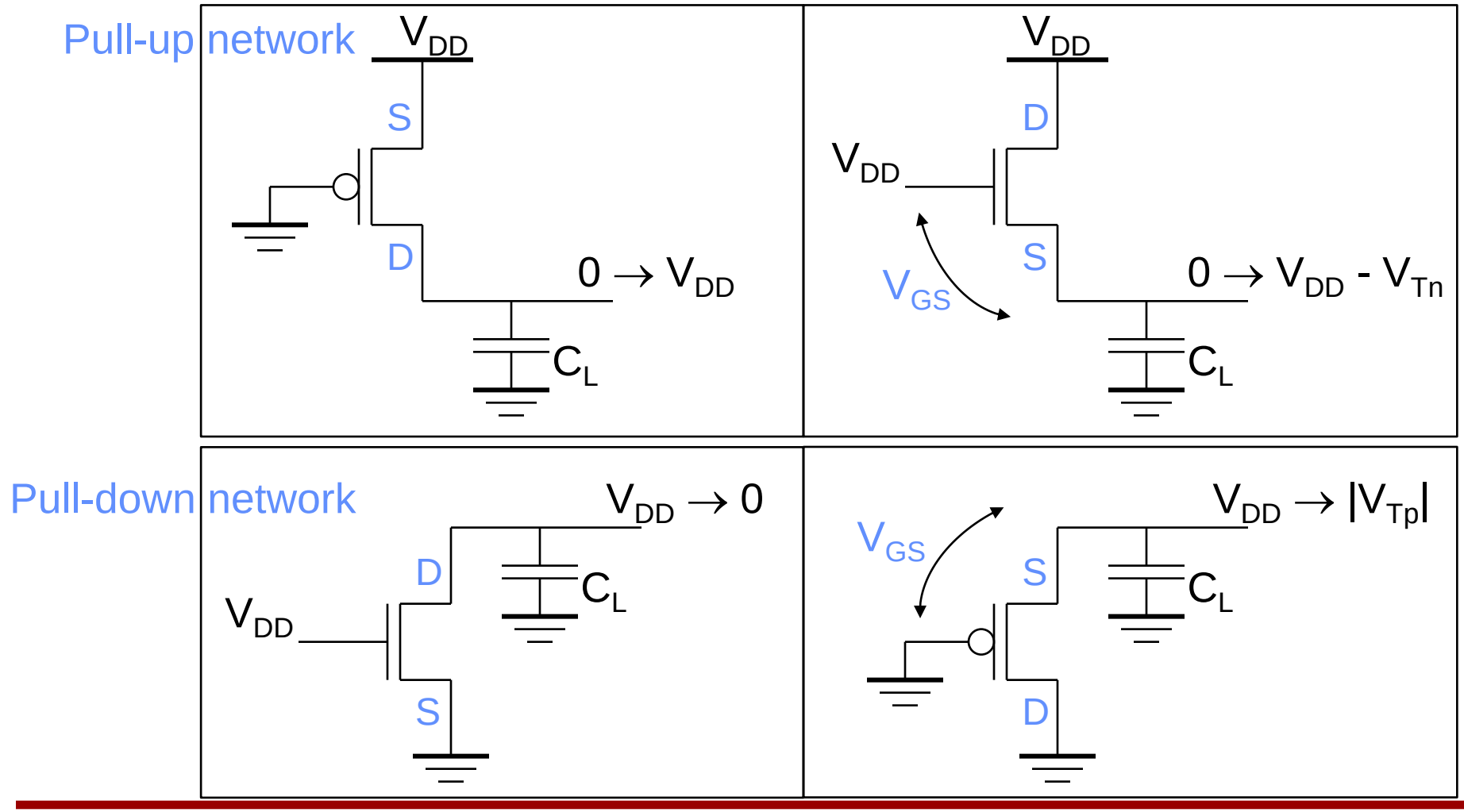
Charge

Transistors as Switches

- NMOS and PMOS



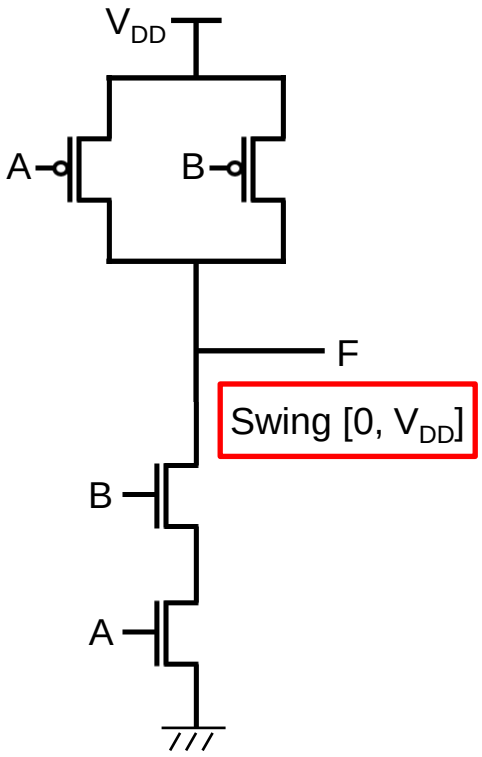
Threshold Drops



CMOS Gates

- Function

  $F = \overline{A \cdot B}$

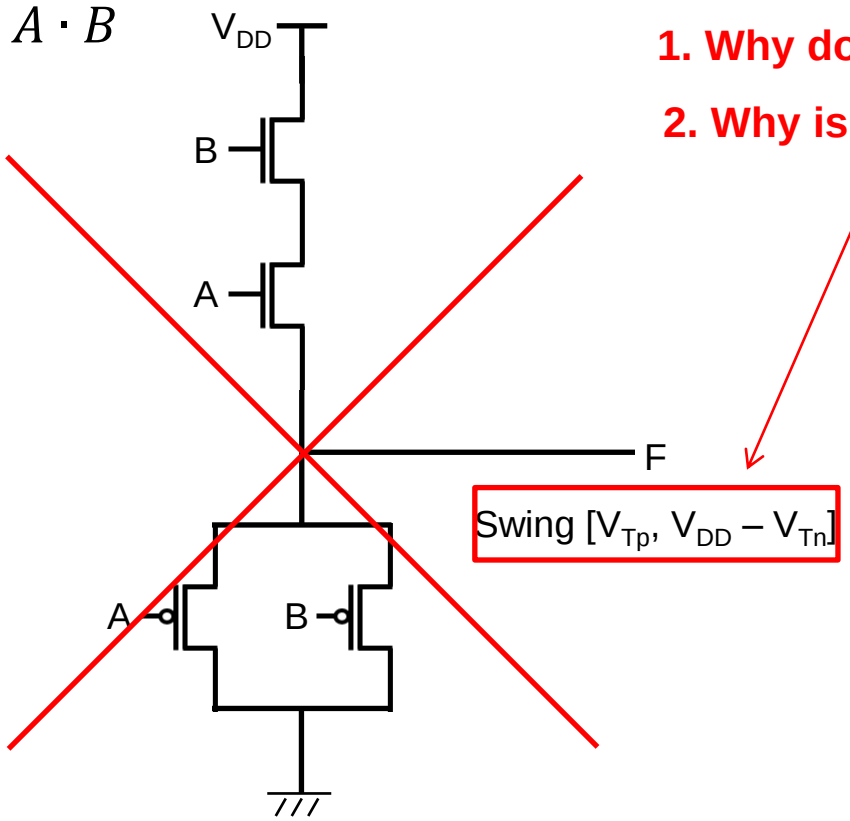


B \ A	0	1
0	1	1
1	1	0

CMOS Gates

- Function

$F = A \cdot B$



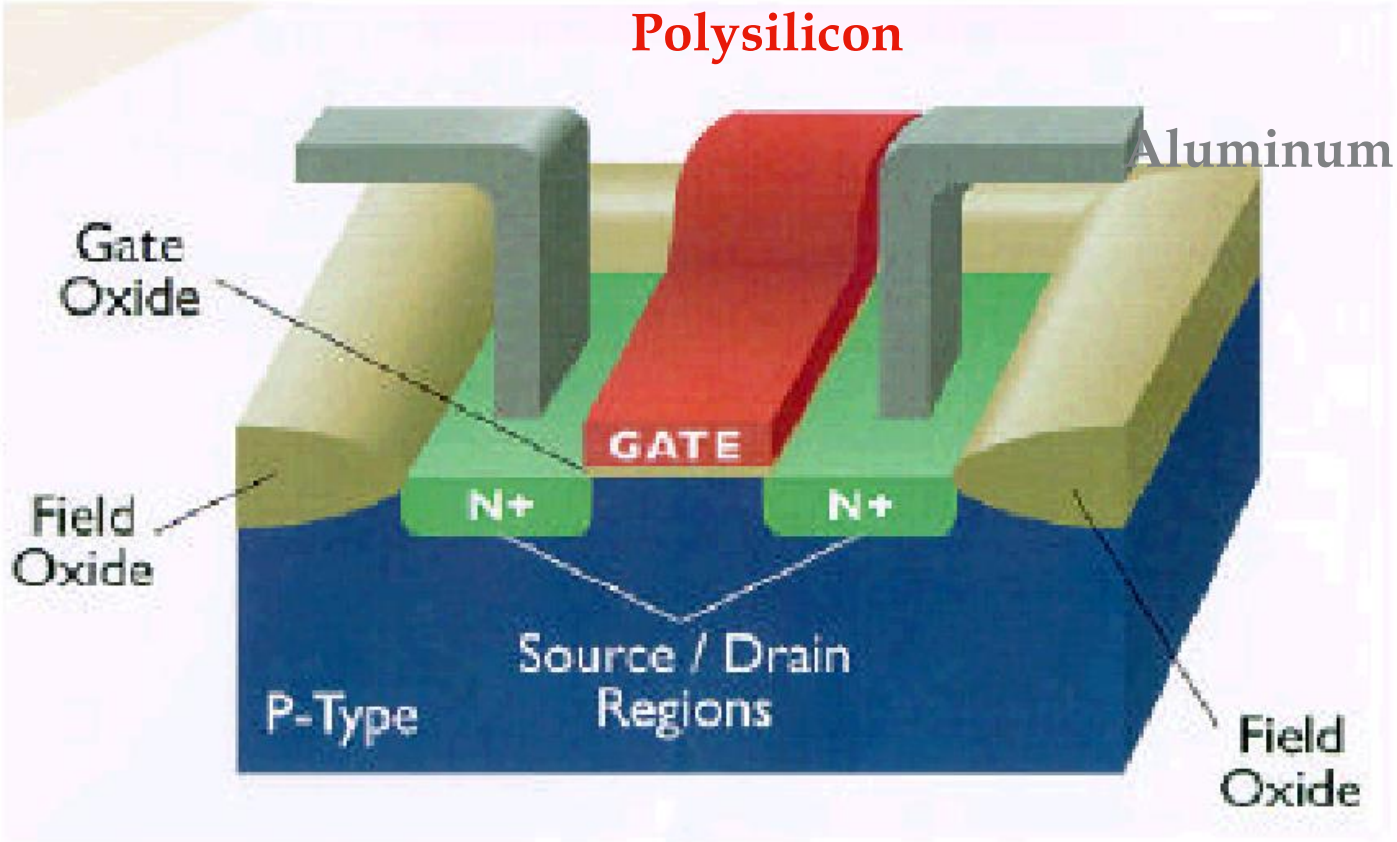
Threshold drop!

1. Why does this happen?

2. Why is this a problem?

B \ A	0	1
0	0	0
1	0	1

The MOS Transistor

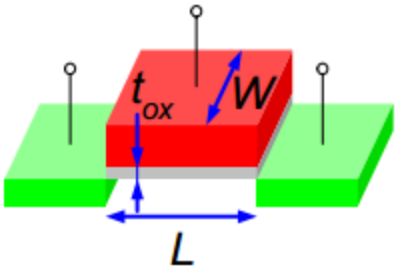


Structural Details

- Channel length L
  - Typical values of L today vary from 130nm to 22 nm
  - The dimension will continue to scale according to Moore's law

- Perpendicular to the plane of the figure is the channel width W
  - Much larger than the minimum length

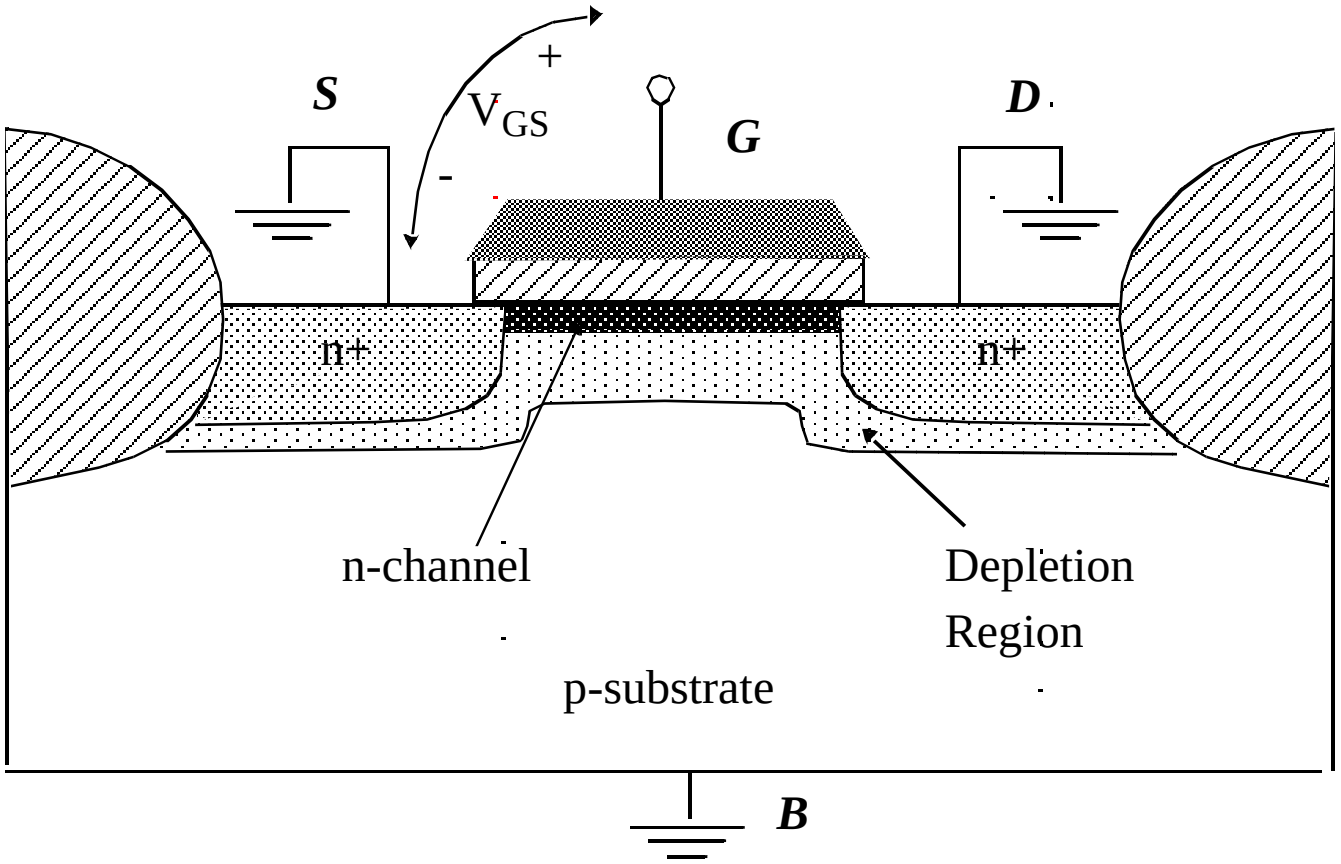
- Gate oxide thickness t_{ox}
  - Around 25 Å



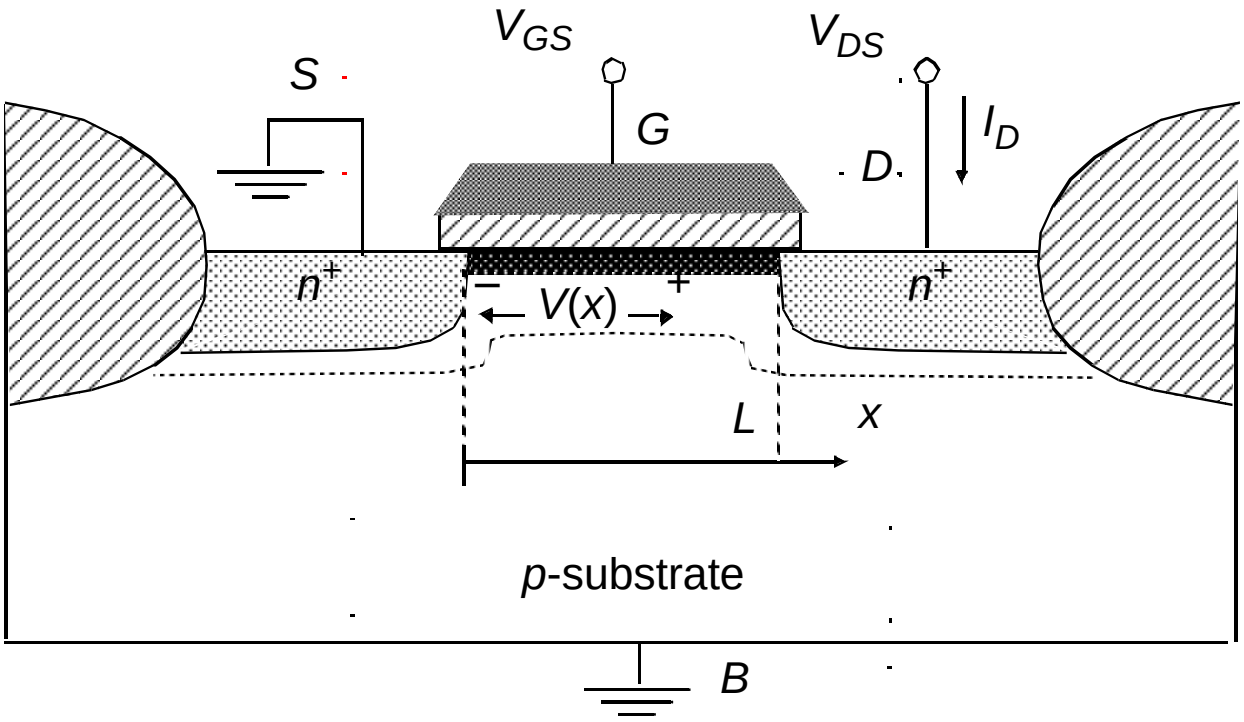
Operational Mechanism

- NMOS
  - N+ source and N+ drain regions separated by p-type material
  - The body or substrate, is a single-crystal silicon wafer
  - Suppose, source, drain and body are all tied to ground and a positive voltage applied to the gate
    - A positive gate voltage will tend to draw electrons from the substrate into the channel region
    - A conducting path is created between drain and source
    - Current will flow from drain to source in presence of a voltage difference between the source and the drain
    - The gate voltage needed to initiate formation of a conducting channel is termed as the threshold voltage Vt

Threshold Voltage: Concept

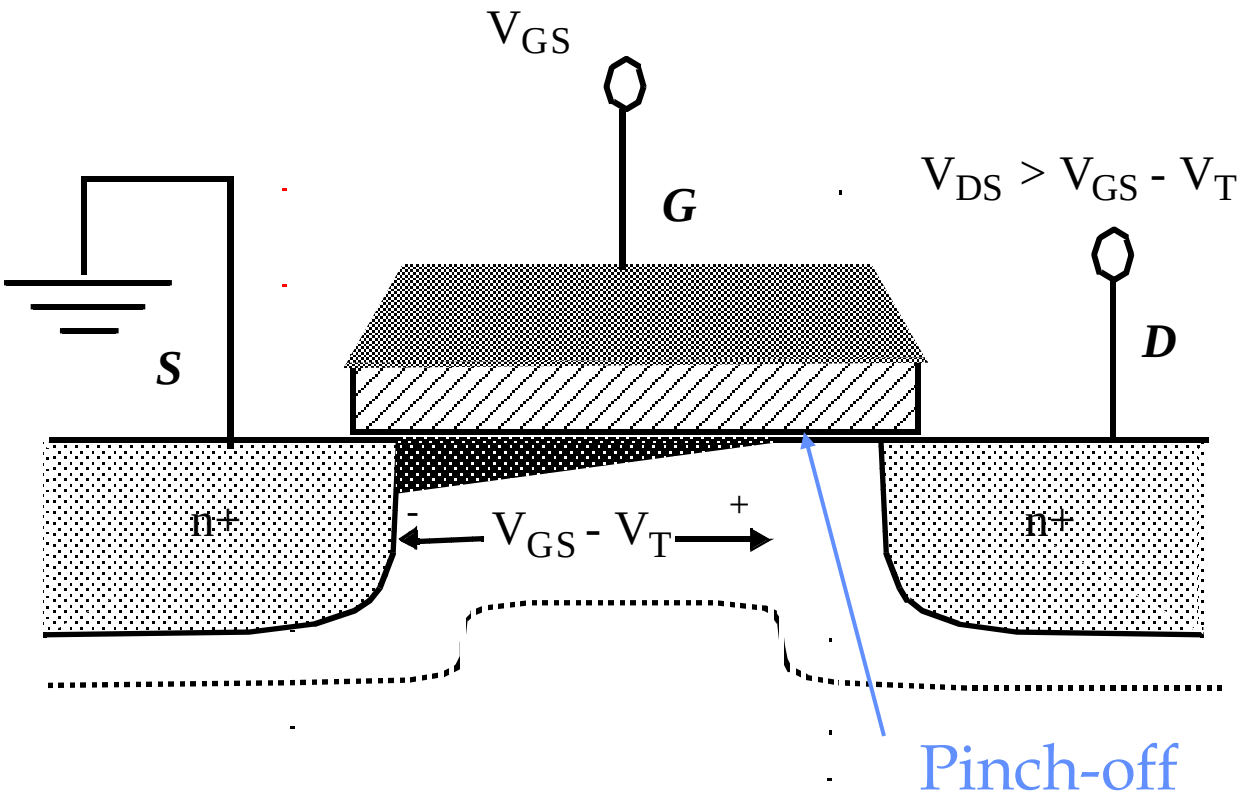


Transistor in Linear



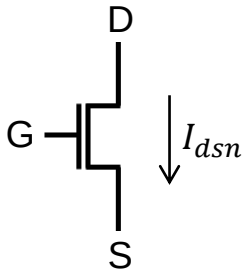
MOS transistor and its bias conditions

Transistor in Saturation



Drain Current (NMOS)

- Cut-off ($V_{gsn} - V_{tn} < 0$)
  - $I_{dsn} = 0$



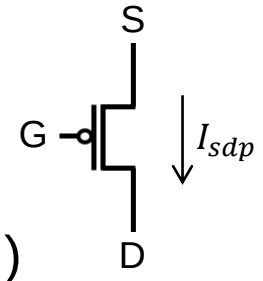
- Linear region ($V_{gsn} - V_{tn} > 0 \; and \; V_{dsn} < V_{gsn} - V_{tn}$)
  - $I_{dsn} = \beta_n \left[(V_{gsn} - V_{tn}) V_{dsn} - \frac{1}{2} {V_{dsn}}^2 \right]$

- Saturation region ($V_{gsn} - V_{tn} > 0 \; and \; V_{dsn} \geq V_{gsn} - V_{tn}$)
  - $I_{dsn} = \frac{1}{2} \beta_n (V_{gsn} - V_{tn})^2$

$$\beta_n = \mu_n c_{OX} \frac{W_n}{L_n} = \mu_n \frac{\varepsilon_{OX}}{t_{OX}} \cdot \frac{W_n}{L_n}$$

Drain Current (PMOS)

- Cut-off ($|V_{gsp}| - |V_{tp}| < 0$)
  - $I_{sdp} = 0$



- Linear region ($|V_{gsp}| - |V_{tp}| > 0 \; and \; |V_{dsp}| < |V_{gsp}| - |V_{tp}|$)
  - $I_{sdp} = \beta_p \left[\left(|V_{gsp}| - |V_{tp}| \right) |V_{dsp}| - \frac{1}{2} |V_{dsp}|^2 \right]$

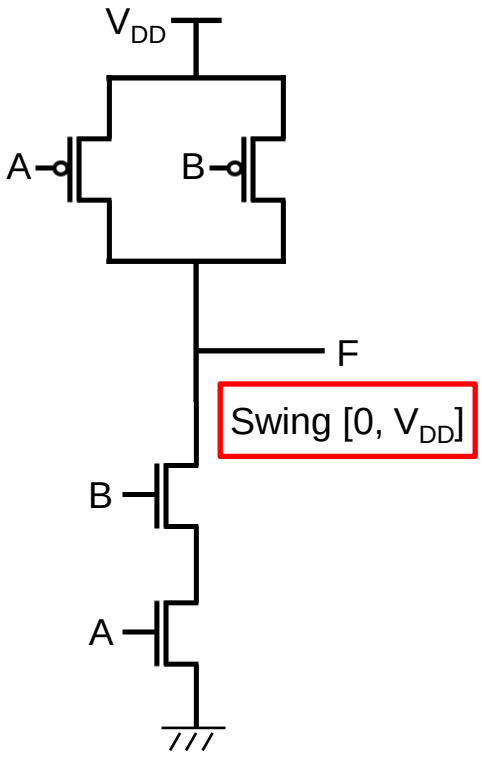
- Saturation region ($\left|V_{gsp}\right| - \left|V_{tp}\right| > 0 \; and \; \left|V_{dsp}\right| > |V_{gsp}| - |V_{tp}|$)
  - $I_{sdp} = \frac{1}{2} \beta_p (|V_{gsp}| - |V_{tp}|)^2$

$$\beta_p = \mu_p c_{OX} \frac{W_p}{L_p} = \mu_p \frac{\varepsilon_{OX}}{t_{OX}} \cdot \frac{W_p}{L_p}$$

CMOS Gates

- Function

  $F = \overline{A \cdot B}$

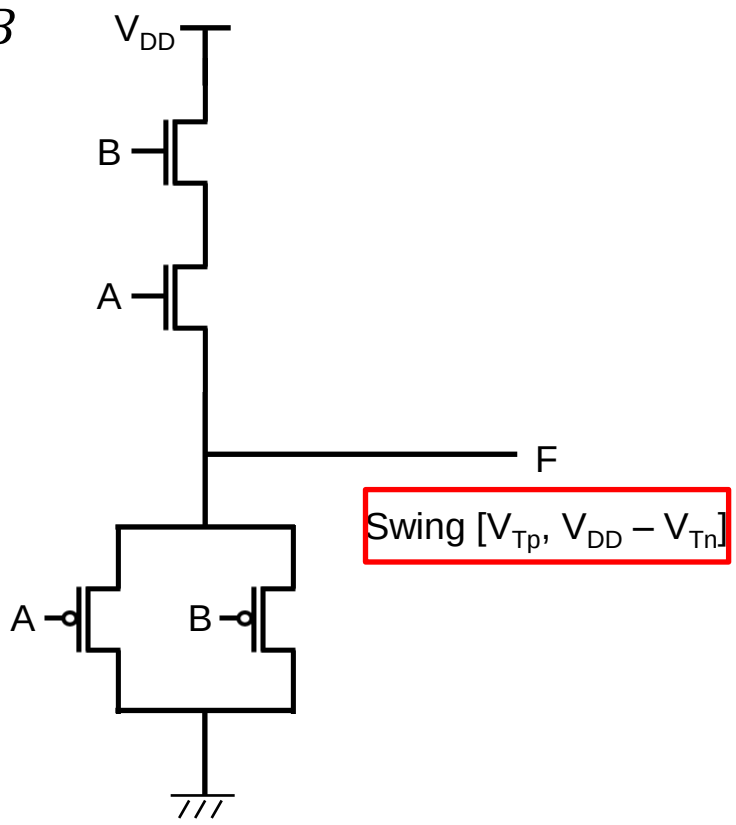


B \ A	0	1
0	1	1
1	1	0

CMOS Gates

- Function

$F = A \cdot B$

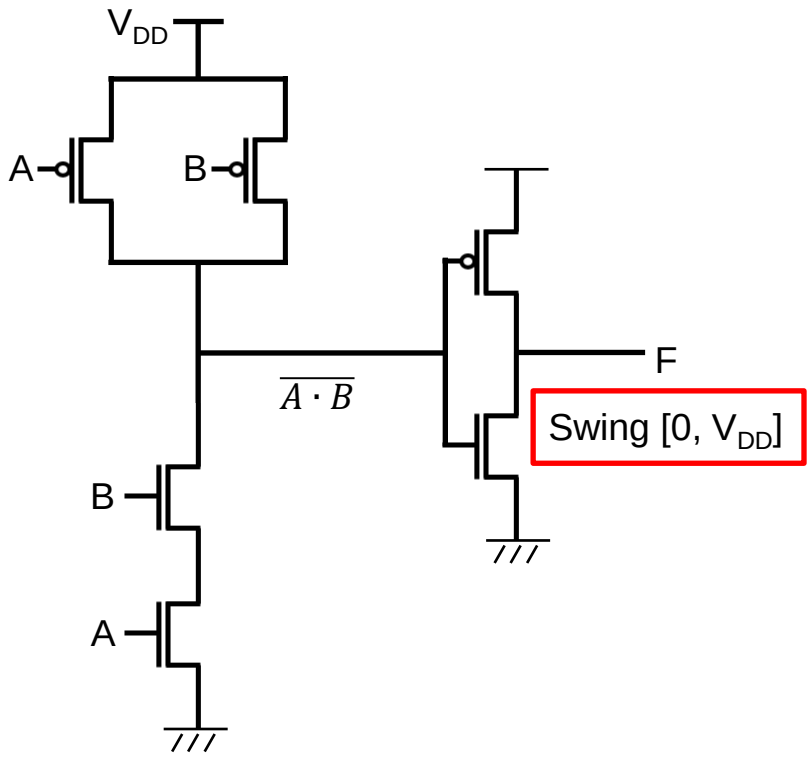


B \ A	0	1
0	0	0
1	0	1

CMOS Gates

- Function

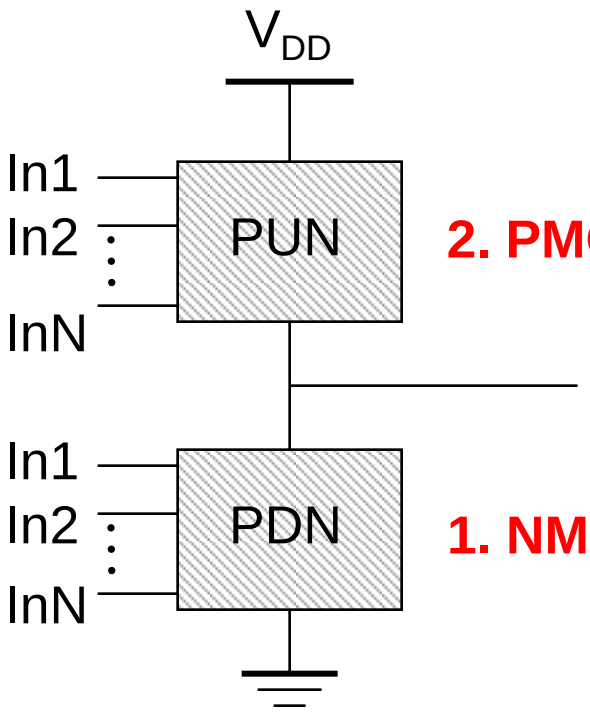
$$F = A \cdot B = \overline{\overline{A \cdot B}}$$



B \ A	0	1
0	0	0
1	0	1

How to Design CMOS Gates

- The function of the PUN is to provide a connection between the output and V_{DD} anytime the output of the logic gate is meant to be 1
- Similarly the role of the PDN is to connect the output to GND when the output is meant to be 0



2. PMOS only = Dual of PDN

1. NMOS only = $\overline{F}$

Pull-up network (PUN) and Pull-down network (PDN) are **dual** logic networks.

Dual Logic

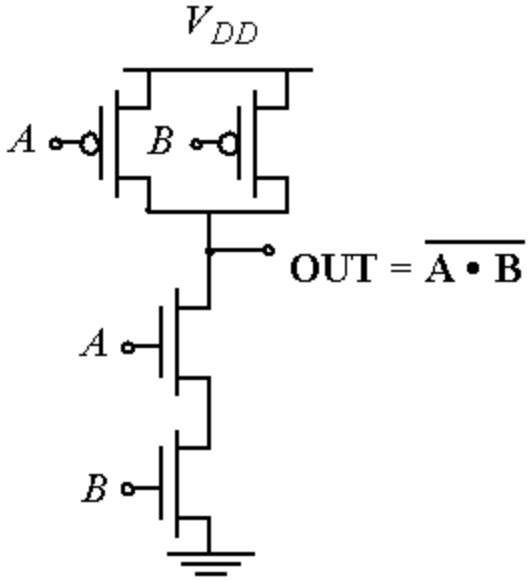
- Dual of $f(X_1, X_2, \ldots, X_n, 0, 1, \text{AND}, \text{OR})$
  $= f(X_1, X_2, \ldots, X_n, \mathbf{1}, \mathbf{0}, \mathbf{OR}, \mathbf{AND})$

- $(A \cdot B)^D = A + B$
- $(A + B)^D = A \cdot B$
- $(1 \cdot A)^D = 0 + A = A$
- $(1 + A)^D = 0 \cdot A = 0$
- $(0 \cdot A)^D = 1 + A = 1$
- $(0 + A)^D = 1 \cdot A = A$

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: G = A B $\Rightarrow$ Conduction to GND

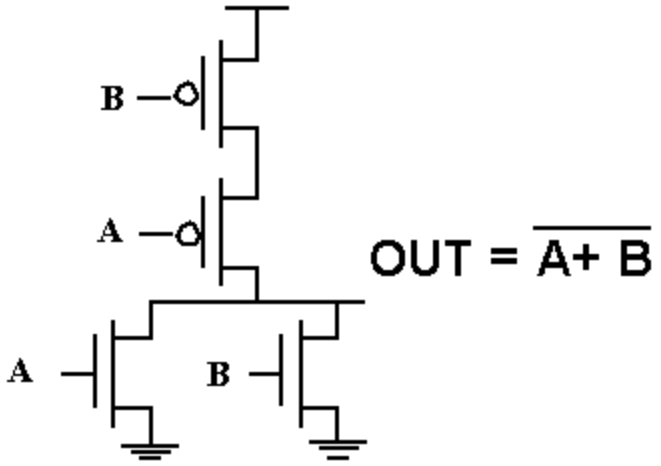
PUN: F= $\overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

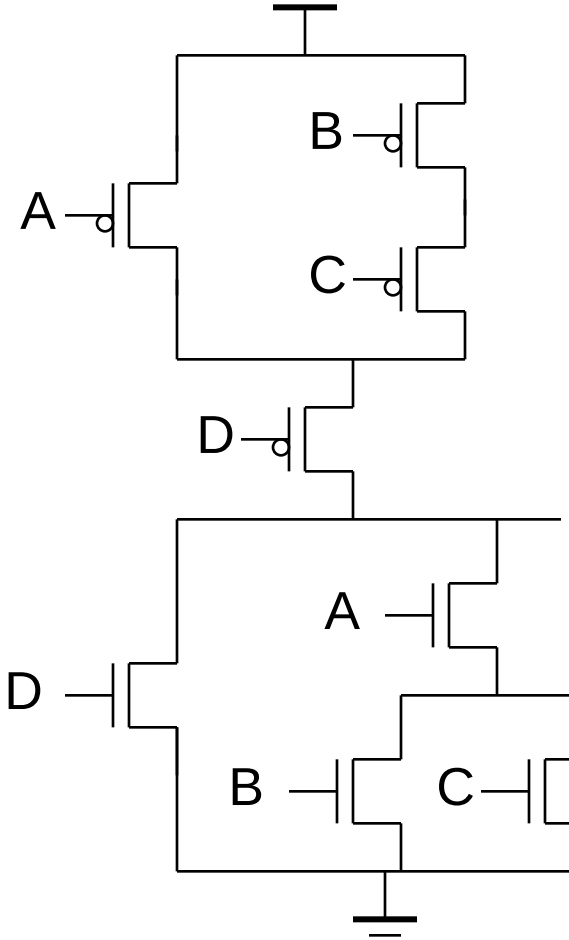
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate

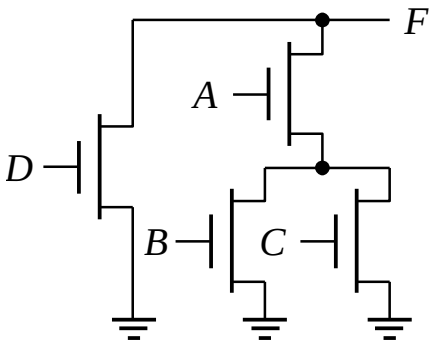


Complex CMOS Gate

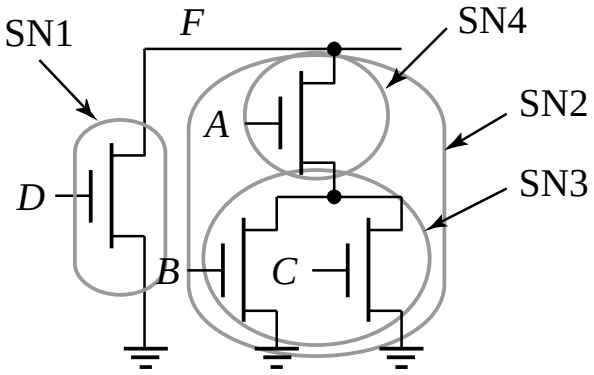


$$OUT = \overline{D + A \bullet (B + C)}$$

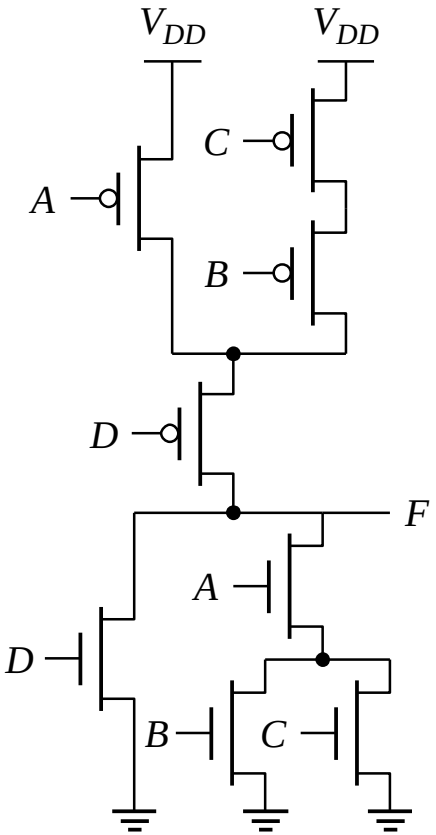
Constructing a Complex Gate



(a) pull-down network

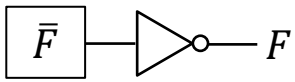


(b) Deriving the pull-up network hierarchically by identifying sub-nets



(c) complete gate

Conversion From a Boolean Equation to a Schematic

- For given F
  1. F
  2. $F = \bar{\bar{F}} =$ 

- $F = \overline{A \cdot B}$
- $F = A \cdot B$
- $F = A \cdot \bar{B}$

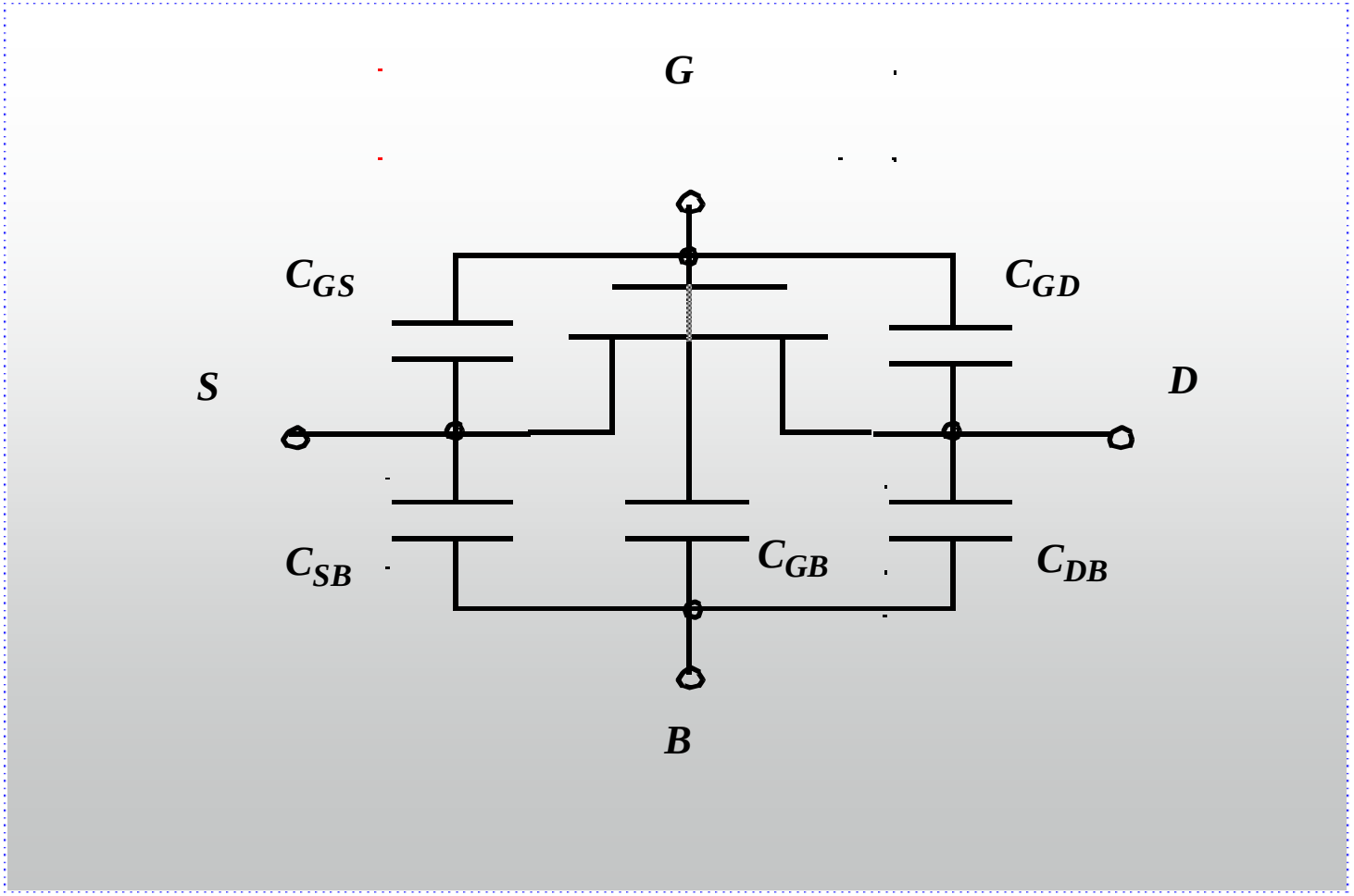
Example

- $F = \overline{A \cdot B \cdot C}$ (NAND3)
- $F = A + B + C$ (OR3)
- $F = \overline{A \cdot B + C}$ (AOI21)
- $F = A \oplus B$ (XOR2)
- $F = \overline{A \oplus B}$ (XNOR2)
- $S = A \oplus B \oplus C$ (Sum)
- $\mathrm{CO} = (A \oplus B) \cdot C + (A \cdot B)$ (Carry-out)

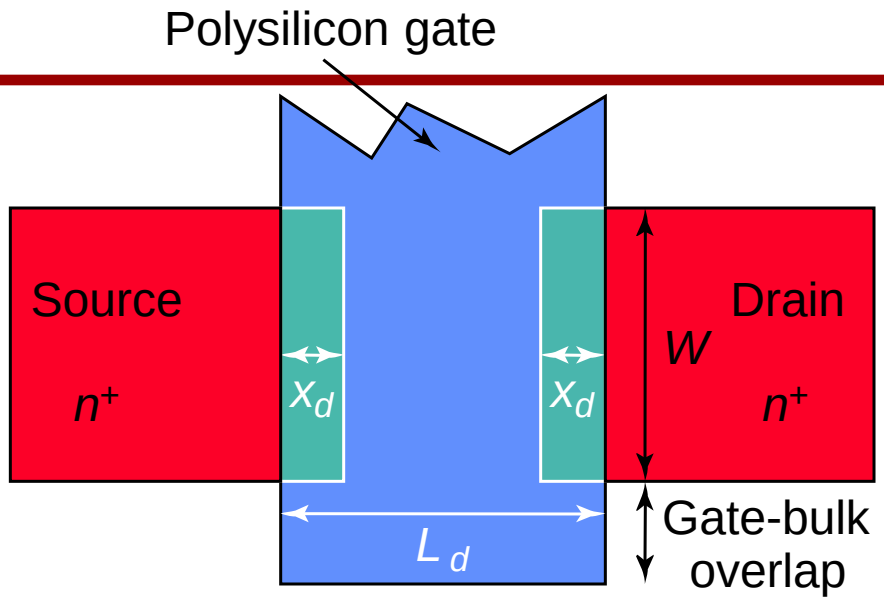
DC Characteristics of CMOS Gates

- Need to consider
  - ON resistance
  - Parasitic capacitance

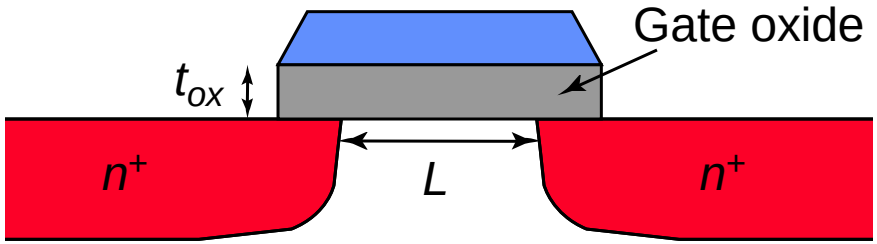
Dynamic Behavior of MOS Transistor



The Gate Capacitance



Top view

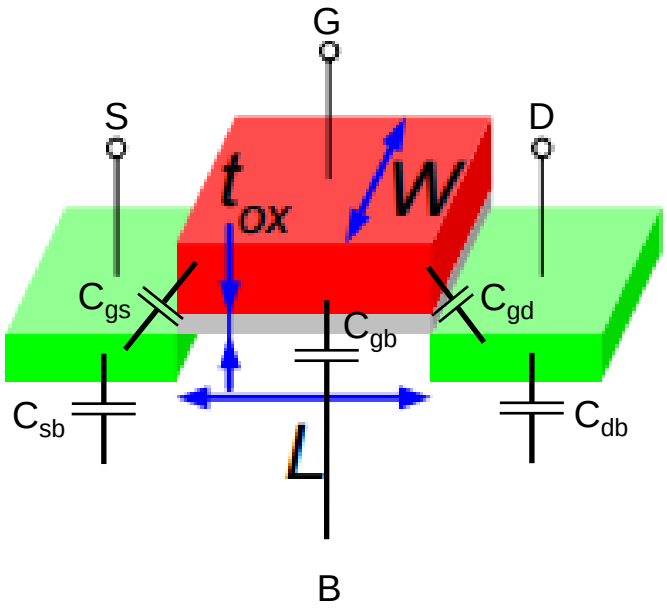


Cross section

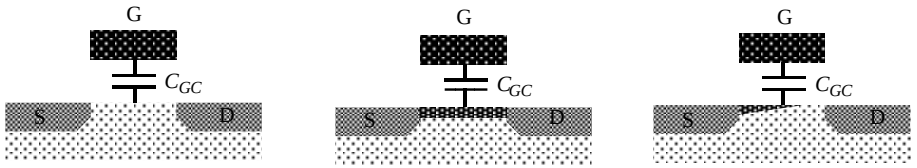
$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

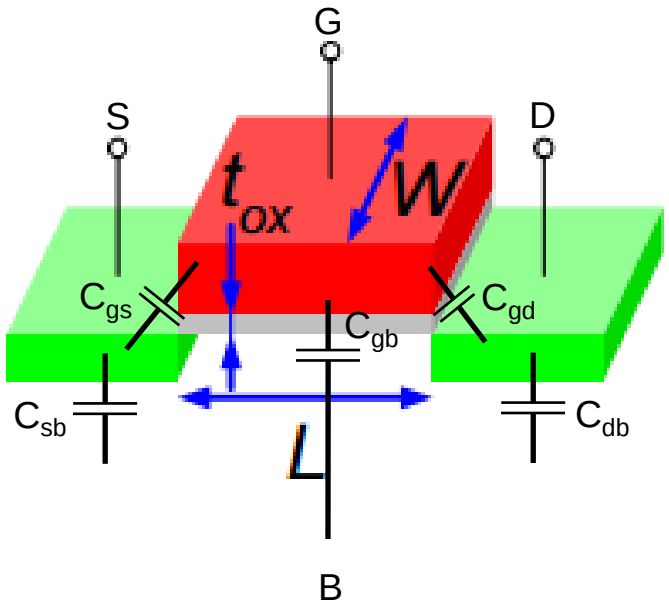
MOS Capacitance

- The source and drain regions and the substrate form pn junctions that give rise to two additional capacitances
- The capacitances Csb and Cdb are n+p source/drain junction capacitance for NMOS devices



MOS Capacitance





$$C_g = C_{gb} + C_{gs} + C_{gd}$$

Cut-off

$$C_{gs} = C_{gd} = 0$$

$$C_{gb} = \frac{C_o C_{dep}}{C_o + C_{dep}}$$

$$C_o = \frac{\varepsilon_{SiO2}\varepsilon_o}{t_{ox}} WL$$

$$C_{dep} = \frac{\varepsilon_{Si}\varepsilon_o}{d} WL$$

Linear

$$C_{gb} = 0$$

$$C_{gs} = C_{gd} = \frac{1}{2} \cdot \frac{\varepsilon_{SiO2}\varepsilon_o}{t_{ox}} WL$$

Saturation

$$C_{gb} = 0$$

$$C_{gd} = 0$$

$$C_{gs} = \frac{2}{3} \cdot \frac{\varepsilon_{SiO2}\varepsilon_o}{t_{ox}} WL$$

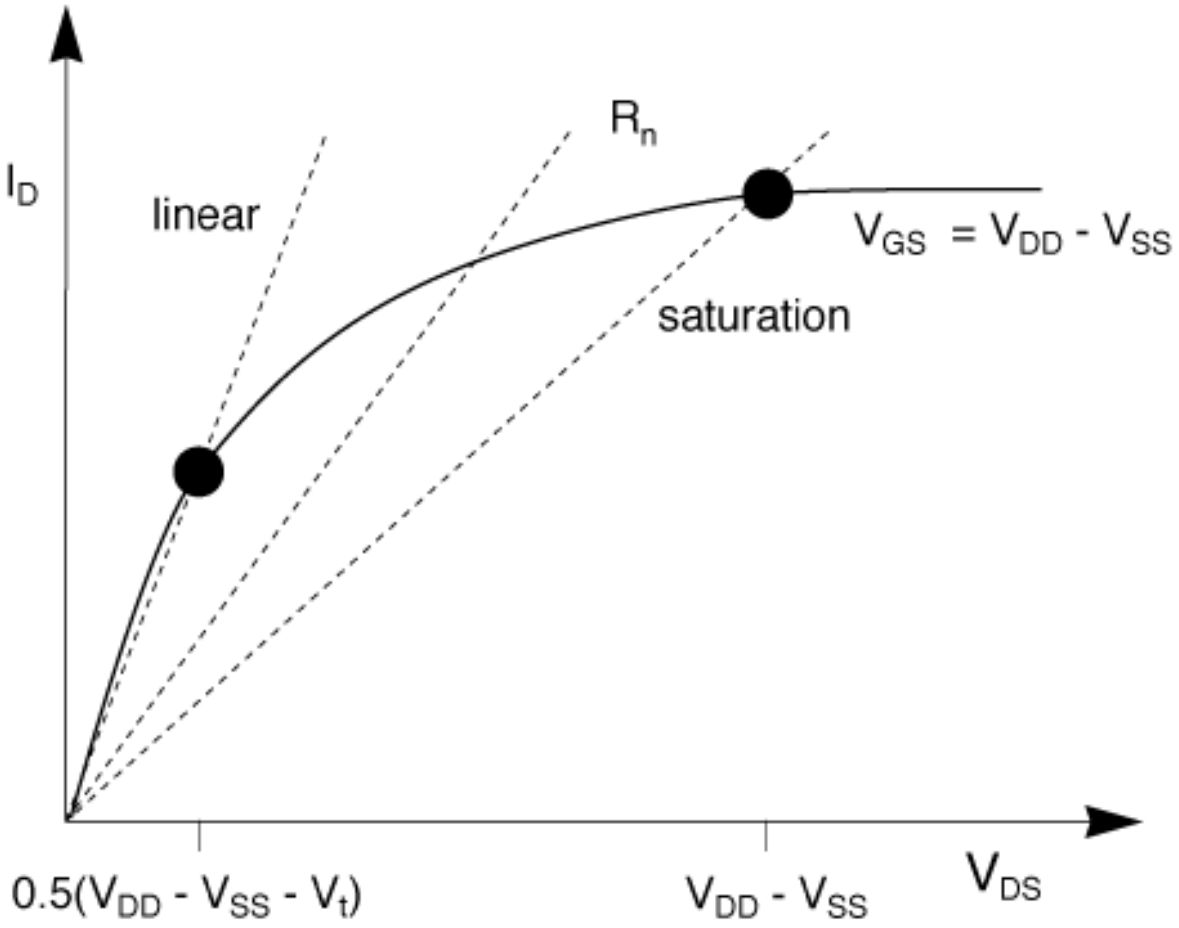
MOS Resistance

- Average V/I at two voltages:
  - maximum output voltage
  - middle of linear region

- Voltage is V_{ds}, current is given I_d at that drain voltage. Step input means that $V_{gs} = V_{DD}$ always.

Saturation: conductance = $g_m = \beta(V_{gs} - V_t)$
Linear: conductance = $g_m = \beta V_{ds}$

MOS Resistance Approximation



Example

- $F = \overline{A1 \cdot A2 \cdot A3 \cdot A4 \cdot A5 \cdot A6 \cdot A7 \cdot A8}$ (NAND8)