EE434
ASIC & Digital Systems

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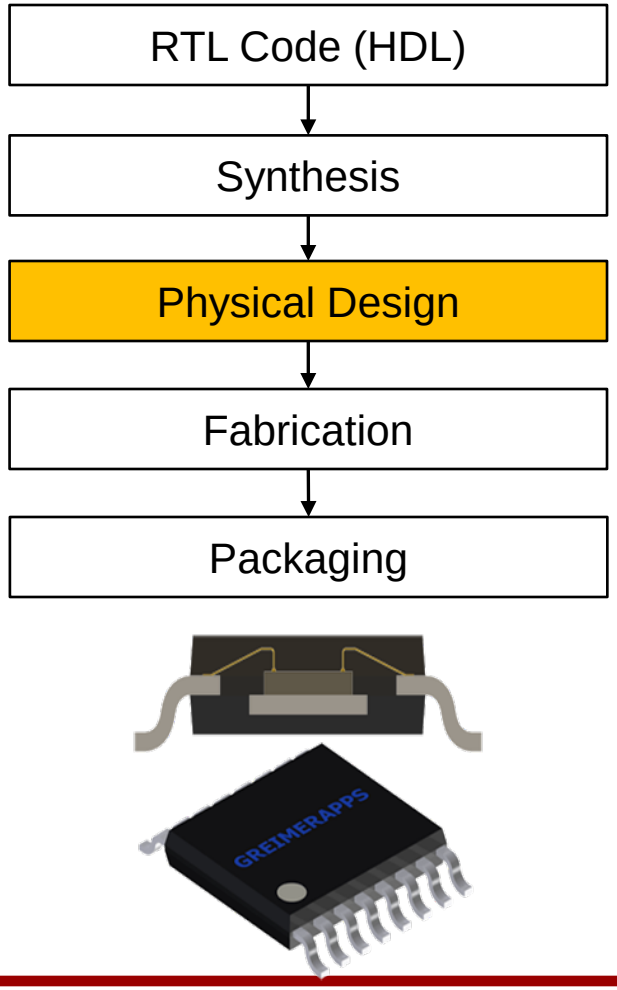
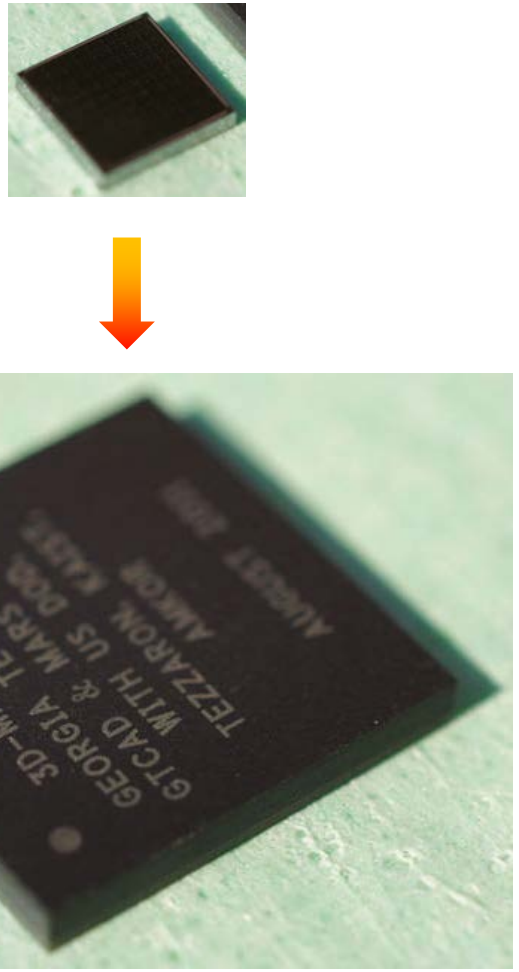
Lecture 7

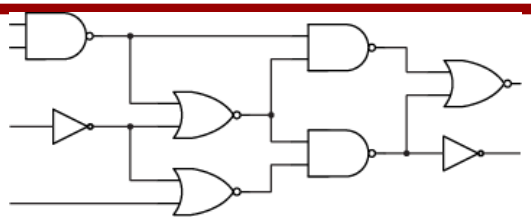
Physical Design

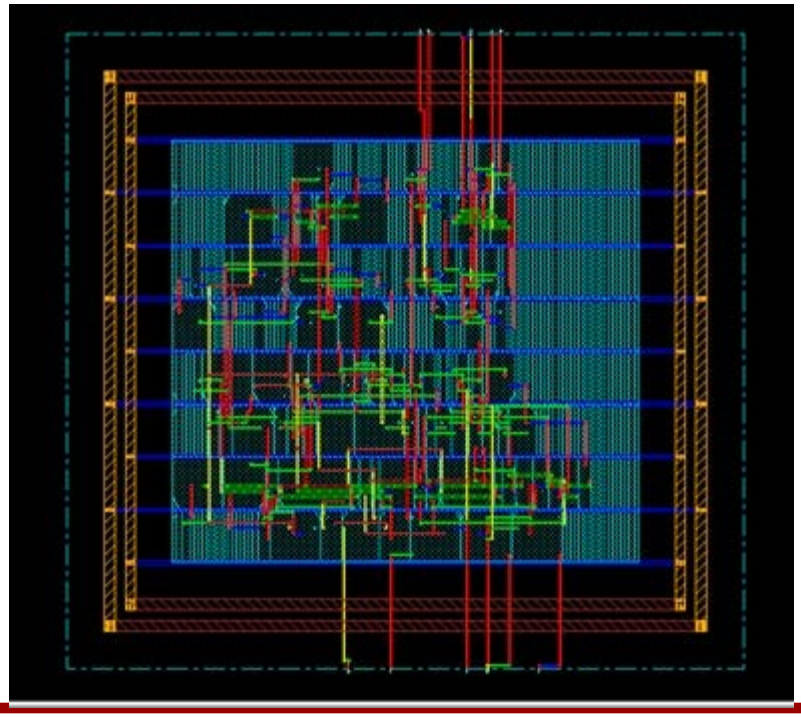
VLSI Design


RTL Code (HDL)
Synthesis
Physical Design
Fabrication
Packaging
GREIMERAPPS


3D-MAPS V1
GEORGIA TECH
GTCAD & US MARS
WITH
TEZZARON
ARMOR

Physical Design





Netlist → Physical layout

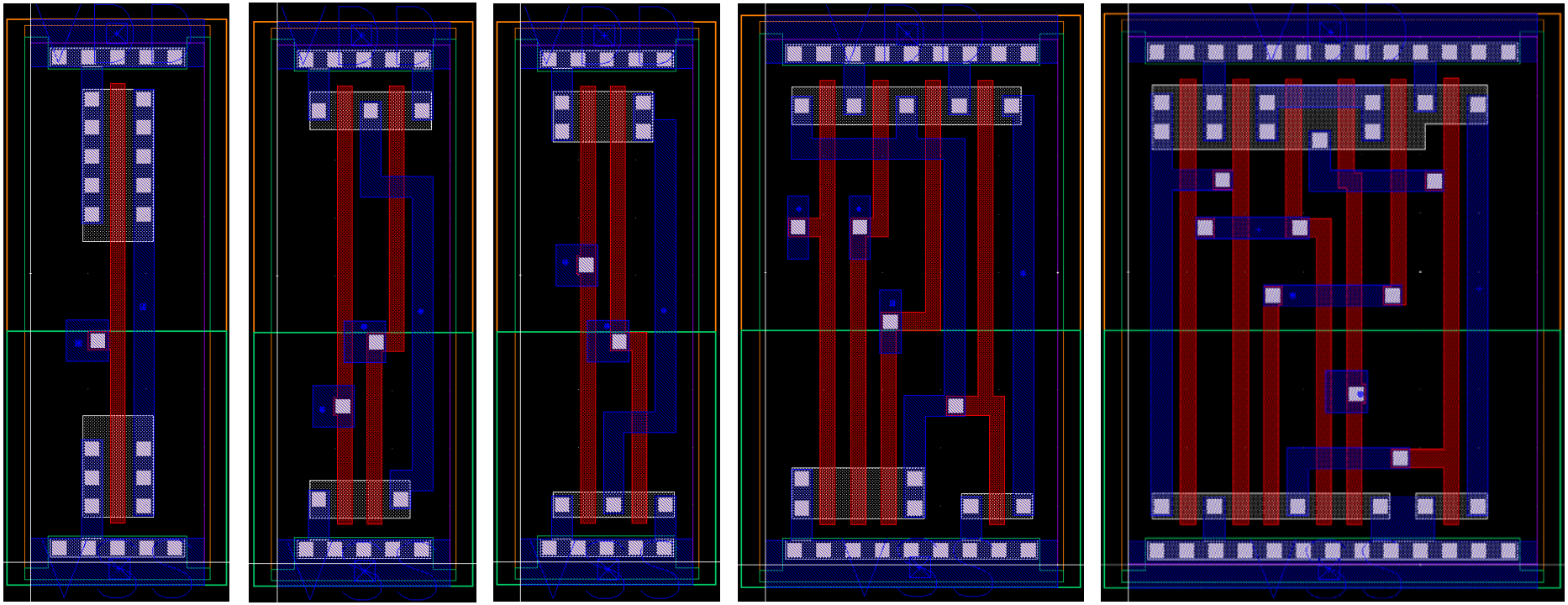
Standard Cell-Based VLSI Design

- Inputs
  - Netlist (.v)
  - Design constraints
    - Timing (.sdc)
    - Power
    - Area
    - …
  - Physical library of standard cells (.lef)
  - Timing/power library (.lib)
  - Capacitance tables, signal integrity information

- Outputs
  - gdsii

Standard Cells

- Standard cells
  - Pre-characterized cells



Standard Cell-Based VLSI Design

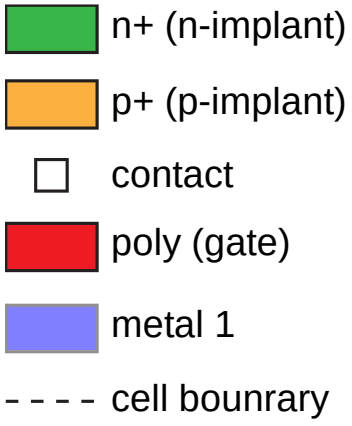
- Design steps
  - Floorplanning
  - Placement of standard cells
  - Routing
    - Signal
    - Power
    - Clock
    - Bus
  - Analysis
    - Timing
    - Power
  - Metal fill insertion
  - RC extraction

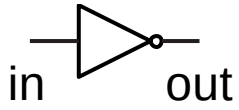
Standard Cell-Based VLSI Design

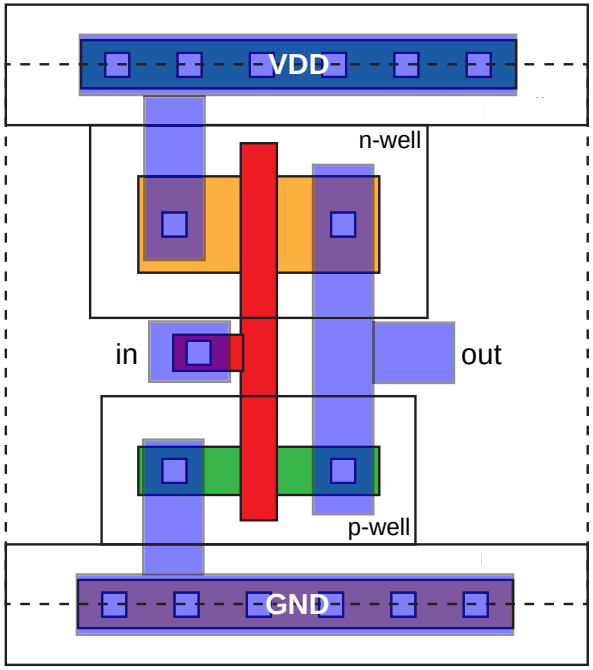
- Routing
  - Use Metal layers only (and via layers).
    - Do not use Poly and Contact layers.

Standard Cells

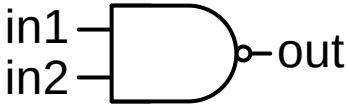
- Design

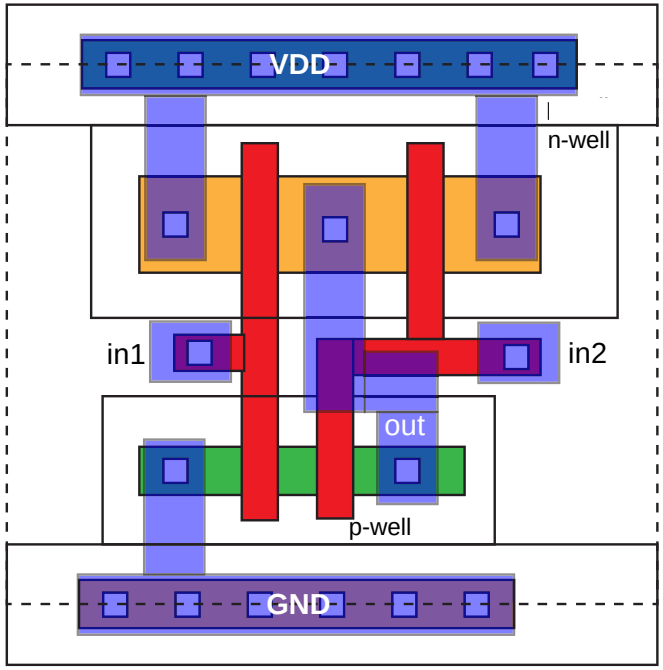






INV

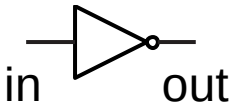


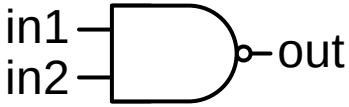


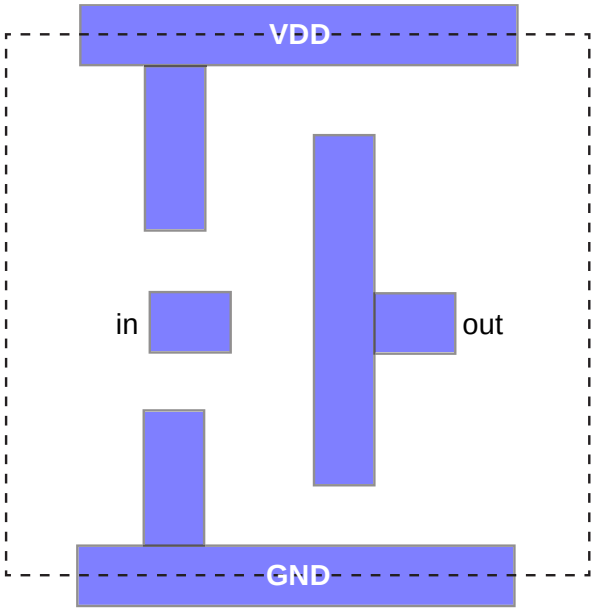
NAND2

Standard Cells

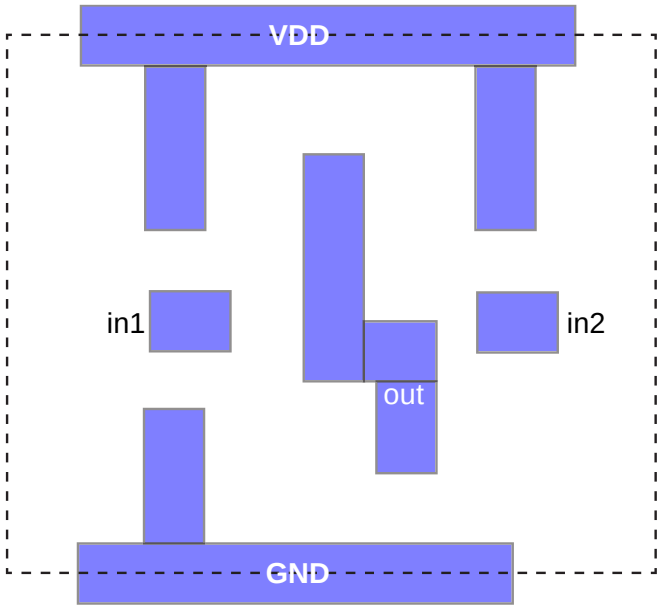
- Abstraction







INV



NAND2

Standard Cells

- Physical library (.lef)
  - Metal layers
  - Macros (standard cells)

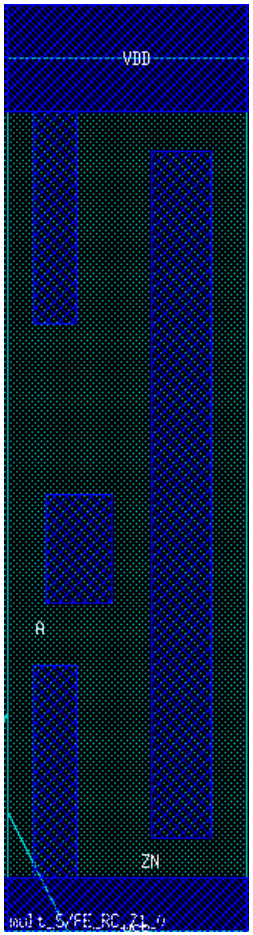
Metal Layers

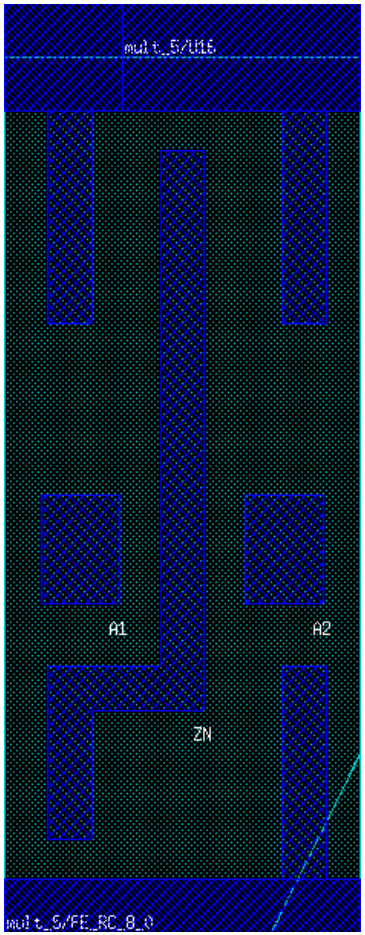
```
LAYER metal1
  TYPE ROUTING ;
  SPACING 0.065 ;
  WIDTH 0.07 ;
  PITCH 0.14 ;
  DIRECTION HORIZONTAL ;
  OFFSET 0.095 0.07 ;
  RESISTANCE RPERSQ 0.38 ;
  THICKNESS 0.13 ;
  HEIGHT 0.37 ;
  CAPACITANCE CPERSQDIST 7.7161e-05 ;
  EDGECAPACITANCE 2.7365e-05 ;
END metal1

LAYER via1
  TYPE CUT ;
  SPACING 0.08 ;
  WIDTH 0.07 ;
  RESISTANCE 5 ;
END via1
```

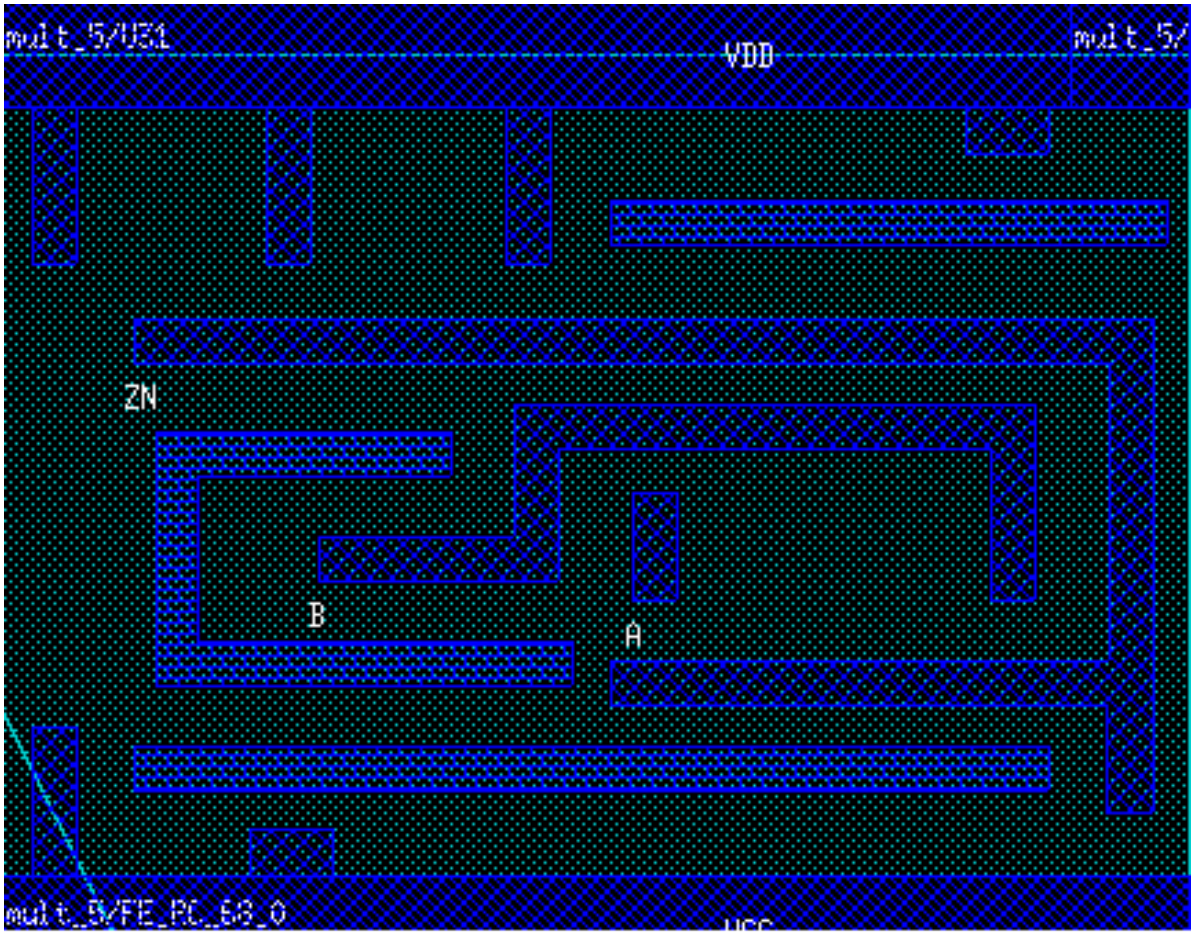
Macros (Standard Cells)

```
MACRO INV_X1
  CLASS core ;
  FOREIGN INV_X1 0.0 0.0 ;
  ORIGIN 0 0 ;
  SYMMETRY X Y ;
  SITE FreePDK45_38x28_10R_NP_162NW_340 ;
  SIZE 0.38 BY 1.4 ;
  PIN A
    DIRECTION INPUT ;
    ANTENNAPARTIALMETALAREA 0.018375 LAYER metal1 ;
    ANTENNAPARTIALMETALSIDEAREA 0.0728 LAYER metal1 ;
    ANTENNAGATEAREA 0.05225 ;
    PORT
      LAYER metal1 ;
        POLYGON 0.06 0.525 0.165 0.525 0.165 0.7 0.06 0.7  ;
    END
  END A
  PIN ZN
    DIRECTION OUTPUT ;
    ANTENNAPARTIALMETALAREA 0.1045 LAYER metal1 ;
    ANTENNAPARTIALMETALSIDEAREA 0.3107 LAYER metal1 ;
    ANTENNADIFFAREA 0.109725 ;
    PORT
      LAYER metal1 ;
        POLYGON 0.23 0.15 0.325 0.15 0.325 1.25 0.23 1.25  ;
    END
  END ZN
  PIN VDD
    DIRECTION INOUT ;
    USE power ;
    SHAPE ABUTMENT ;
    PORT
      LAYER metal1 ;
        POLYGON 0 1.315 0.04 1.315 0.04 0.975 0.11 0.975 0.11 1.315 0.38 1.315 0.38 1.485 0 1.485  ;
    END
  END VDD
  PIN VSS
    DIRECTION INOUT ;
    USE ground ;
    SHAPE ABUTMENT ;
    PORT
      LAYER metal1 ;
        POLYGON 0 -0.085 0.38 -0.085 0.38 0.085 0.11 0.085 0.11 0.425 0.04 0.425 0.04 0.085 0 0.085  ;
    END
  END VSS
END INV_X1
```

Standard Cells







INV_X1 NAND2_X1 XOR2_X2

Timing/Power Library (.lib, .db)

```
cell (INV_X1) {
    drive_strength : 1;
    area           : 0.532000;
    pg_pin(VDD) {
      voltage_name : VDD;
      pg_type      : primary_power;
    }
    pg_pin(VSS) {
      voltage_name : VSS;
      pg_type      : primary_ground;
    }

    cell_leakage_power      : 14.353185;

    leakage_power () {
      when         : "!A";
      value        : 10.102224;
    }
    leakage_power () {
      when         : "A";
      value        : 18.604146;
    }

    pin (A) {
      direction          : input;
      related_power_pin  : "VDD";
      related_ground_pin : "VSS";
      capacitance        : 1.700230;
      fall_capacitance   : 1.549360;
      rise_capacitance   : 1.700230;
    }
```

```
pin (ZN) {
  direction          : output;
  related_power_pin  : "VDD";
  related_ground_pin : "VSS";
  max_capacitance    : 60.730000;
  function           : "!A";

  timing () {
    related_pin        : "A";
    timing_sense       : negative_unate;

    cell_fall(Timing_7_7) {
      index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");
      index_2 ("0.365616,1.897810,3.795620,7.591250,15.182500,30.365000,60.730000");
      values ("0.00334769,0.00529785,0.00763425,0.0122592,0.0214710,0.0398747,0.0766650", \
              "0.00461096,0.00678237,0.00912396,0.0137631,0.0229885,0.0413991,0.0781923", \
              "0.00565781,0.00963029,0.0133910,0.0192072,0.0284937,0.0468495,0.0836153", \
              "0.00501217,0.0107451,0.0162361,0.0248924,0.0380191,0.0575991,0.0941587", \
              "0.00228759,0.00977055,0.0169885,0.0284204,0.0459573,0.0721436,0.111006", \
              "-0.00275926,0.00641510,0.0153503,0.0295626,0.0514378,0.0844139,0.133051", \
              "-0.0102639,0.000468768,0.0110680,0.0280603,0.0542902,0.0939467,0.152970");
    }

    internal_power () {
      related_pin      : "A";
      fall_power(Power_7_7) {
        index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");
        index_2 ("0.365616,1.897810,3.795620,7.591250,15.182500,30.365000,60.730000");
        values ("-0.000035,-0.000051,-0.000070,-0.000108,-0.000184,-0.000336,-0.000640", \
                "-0.000086,-0.000101,-0.000121,-0.000159,-0.000235,-0.000387,-0.000690", \
                "-0.000255,-0.000278,-0.000300,-0.000338,-0.000413,-0.000565,-0.000869", \
                "0.287831,0.148648,0.030826,-0.000677,-0.000757,-0.000907,-0.001210", \
                "0.971887,0.823874,0.649421,0.408881,0.159170,-0.001443,-0.001744", \
                "1.891282,1.764827,1.588497,1.264991,0.830546,0.422656,0.157359", \
                "3.063886,2.982289,2.822534,2.481577,1.897972,1.212948,0.642966");
      }
    }
  }
}
```

Capacitance Table

BASIC_CAP_TABLE ...
M1

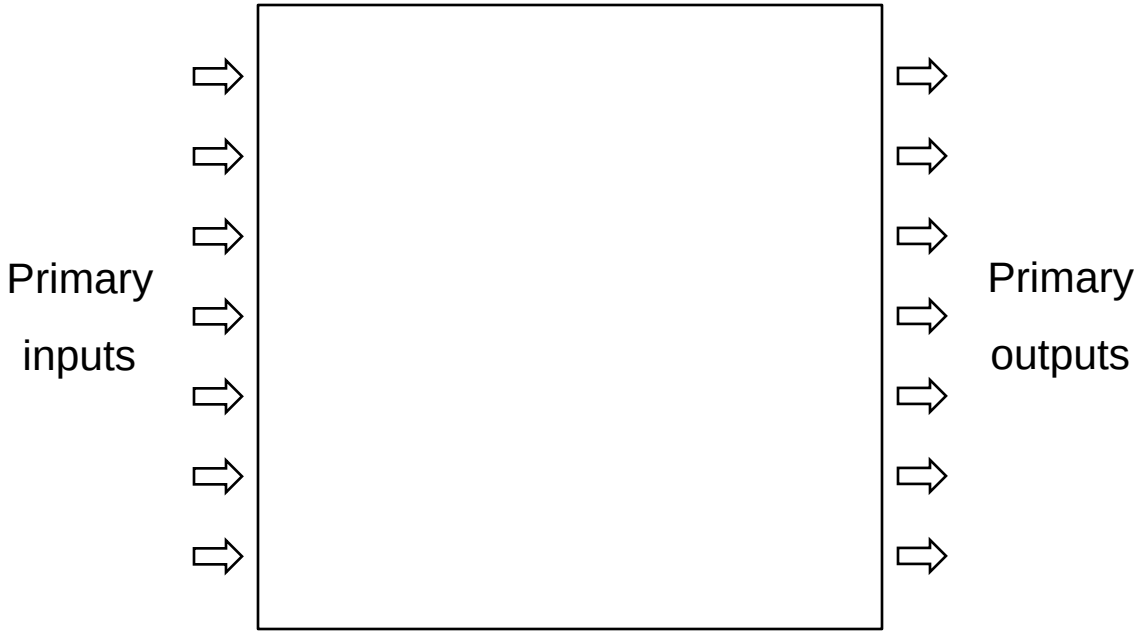
width(um)	space(um)	Ctot(Ff/um)	Cc(Ff/um)	Carea(Ff/um)	Cfrg(Ff/um)
0.070	0.052	0.1986	0.0723	0.0311	0.0115
0.070	0.065	0.1705	0.0509	0.0311	0.0143
0.070	0.200	0.1179	0.0115	0.0311	0.0319
0.070	0.335	0.1150	0.0030	0.0311	0.0388
0.070	0.470	0.1148	0.0009	0.0311	0.0409
0.070	0.605	0.1147	0.0002	0.0311	0.0416
0.070	0.740	0.1147	0.0001	0.0311	0.0417
0.070	0.875	0.1147	0.0000	0.0311	0.0418
0.210	0.052	0.2642	0.0727	0.0934	0.0127
0.210	0.065	0.2358	0.0512	0.0934	0.0155
0.210	0.200	0.1828	0.0115	0.0934	0.0331
0.210	0.335	0.1798	0.0030	0.0934	0.0401
0.210	0.470	0.1796	0.0009	0.0934	0.0422
0.210	0.605	0.1796	0.0002	0.0934	0.0428
0.210	0.740	0.1796	0.0001	0.0934	0.0430
0.210	0.875	0.1796	0.0000	0.0934	0.0431
1.000	0.052	0.6285	0.0727	0.4449	0.0191
1.000	0.065	0.6002	0.0512	0.4449	0.0219
1.000	0.200	0.5471	0.0115	0.4449	0.0396
1.000	0.335	0.5442	0.0030	0.4449	0.0465
1.000	0.470	0.5440	0.0009	0.4449	0.0487
1.000	0.605	0.5440	0.0002	0.4449	0.0493
1.000	0.740	0.5440	0.0001	0.4449	0.0495
1.000	0.875	0.5440	0.0000	0.4449	0.0495
9.000	0.052	4.3181	0.0727	4.0043	0.0842
9.000	0.065	4.2898	0.0512	4.0043	0.0870
9.000	0.200	4.2367	0.0115	4.0043	0.1047
9.000	0.335	4.2338	0.0030	4.0043	0.1116
9.000	0.470	4.2336	0.0009	4.0043	0.1138
9.000	0.605	4.2335	0.0002	4.0043	0.1144

EXTENDED_CAP_TABLE ...

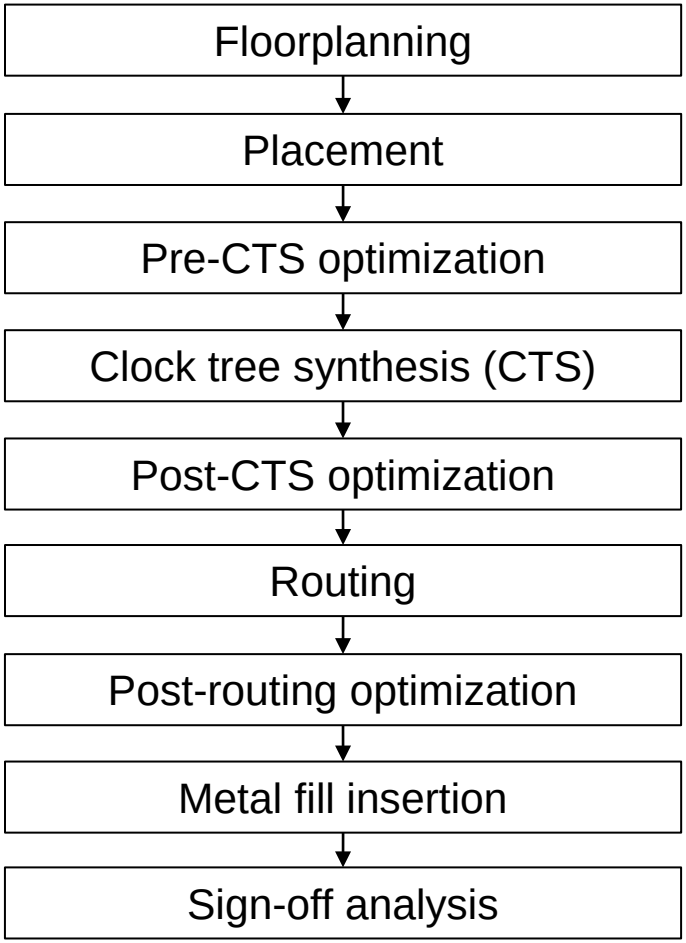
```
# Lef File: ../lef/NangateOpenCellLibrary_PDKv1_3_v2009_07.lef
# SolverExe: coyote
# Solver Type: coyote
       1.03          10          10           1           1
          1        0.37        0.13         3.9           0
          0           0           0           7           4
          2           7           2           0           0
          0           0         140        1540         700
        420         280         140         130          65
        140          70         140         240         430
        620        1000        2140           0        0.07
       0.77        0.35        0.21        0.14        0.07
      0.065      0.0325   1.2987013   2.8571429   4.7619048
  7.1428571   14.285714   15.384615   30.769231        0.07
      0.035        0.07        0.12       0.215        0.31
        0.5        1.07        2000 6.64702e-05           7
          0   1.2987013   2.8571429   4.7619048   7.1428571
  14.285714   15.384615   30.769231  1.2281e-07 2.15189e-06
7.27608e-06 1.4757835e-05 3.881235e-05 4.23737e-05 9.243475e-05
          7           0   1.2987013   2.8571429   4.7619048
```

Design Constraints

- Load cap
- Input/output delay
- Clock frequency
- …

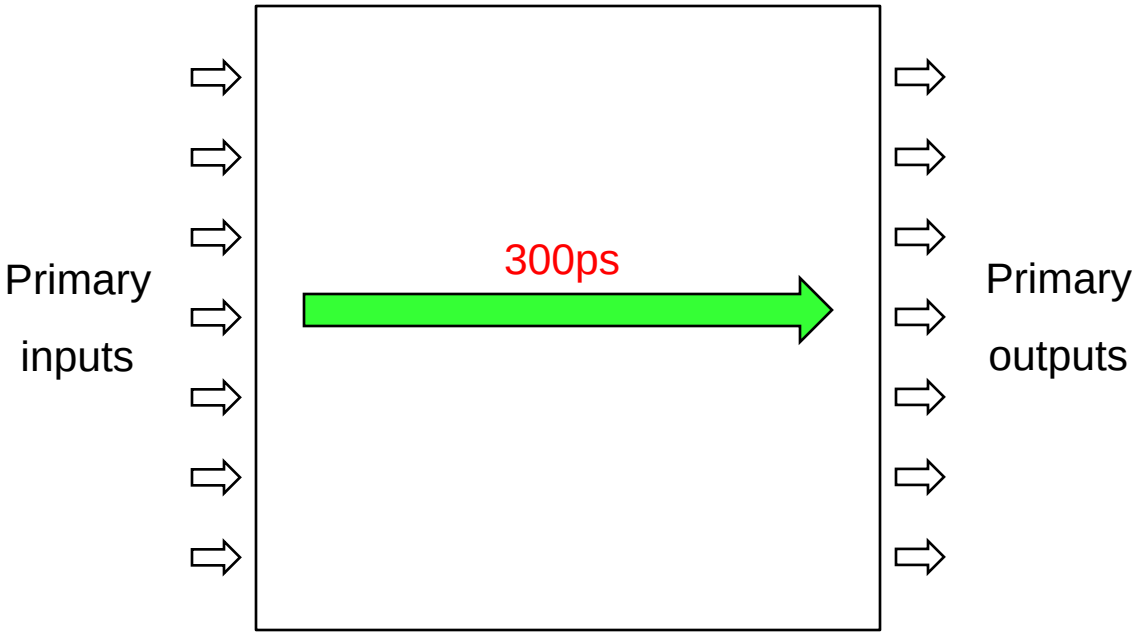


Physical Design



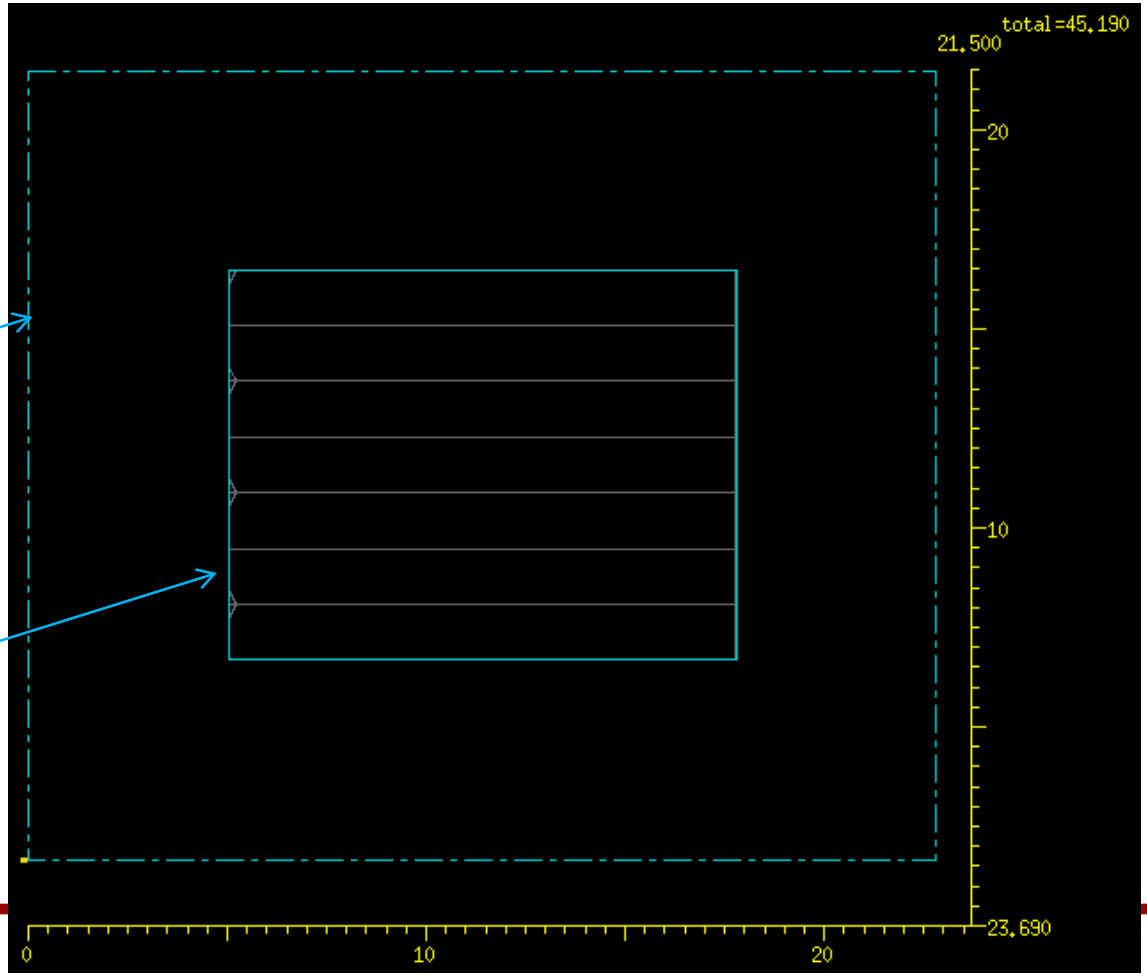
Physical Design

- A 4-bit multiplier
  - Combinational logic
  - Timing constraints



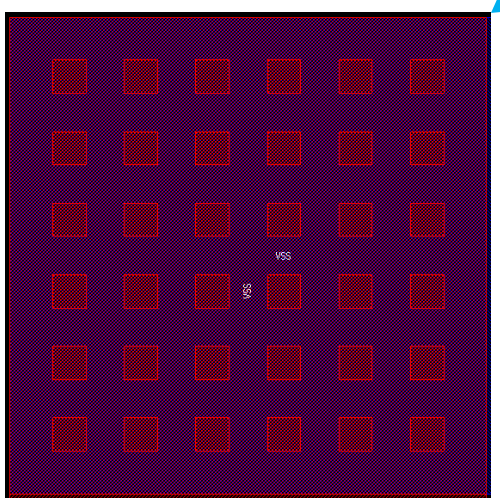
Physical Design

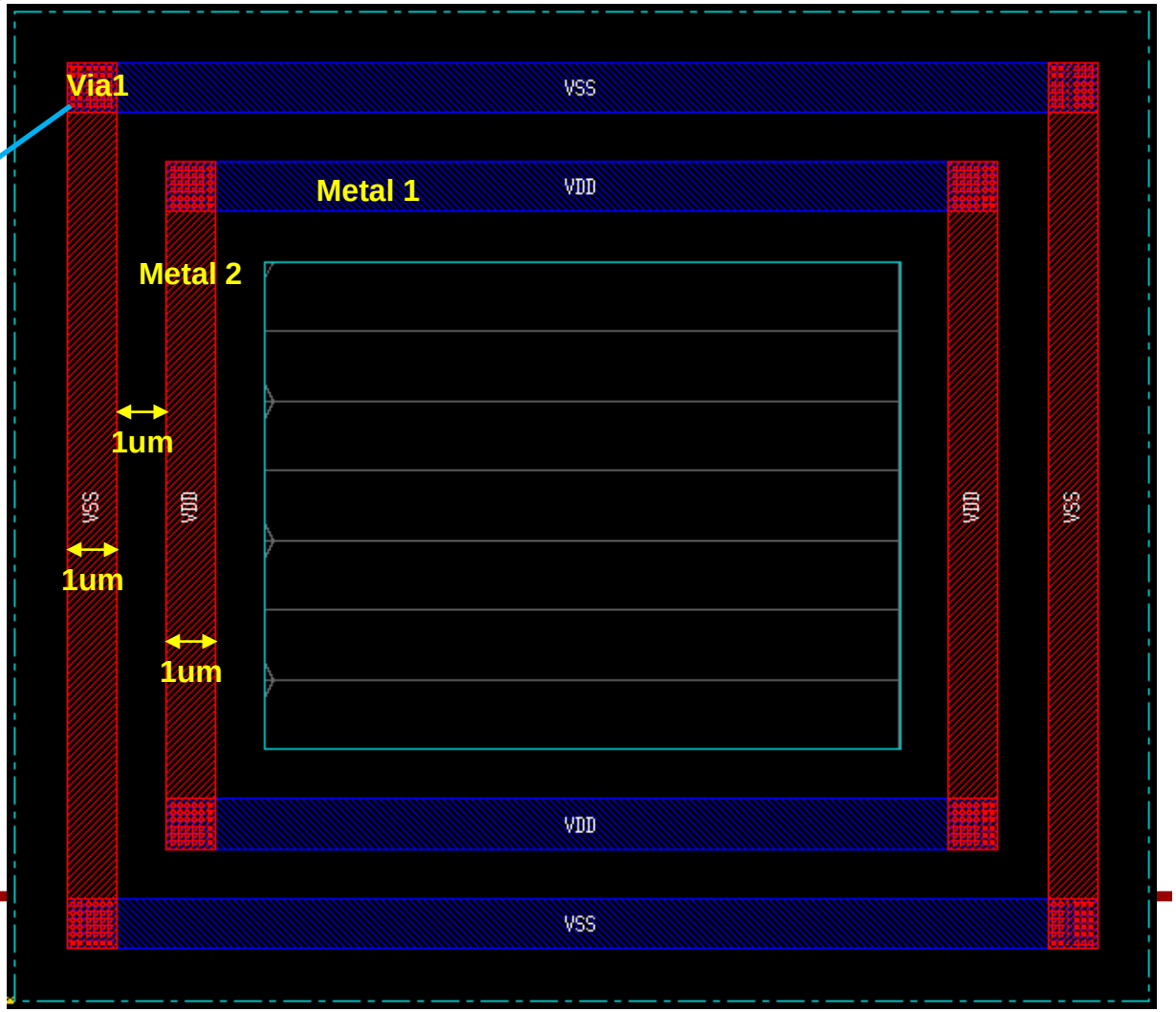
- Design space (Core utilization: 60%)



Physical Design

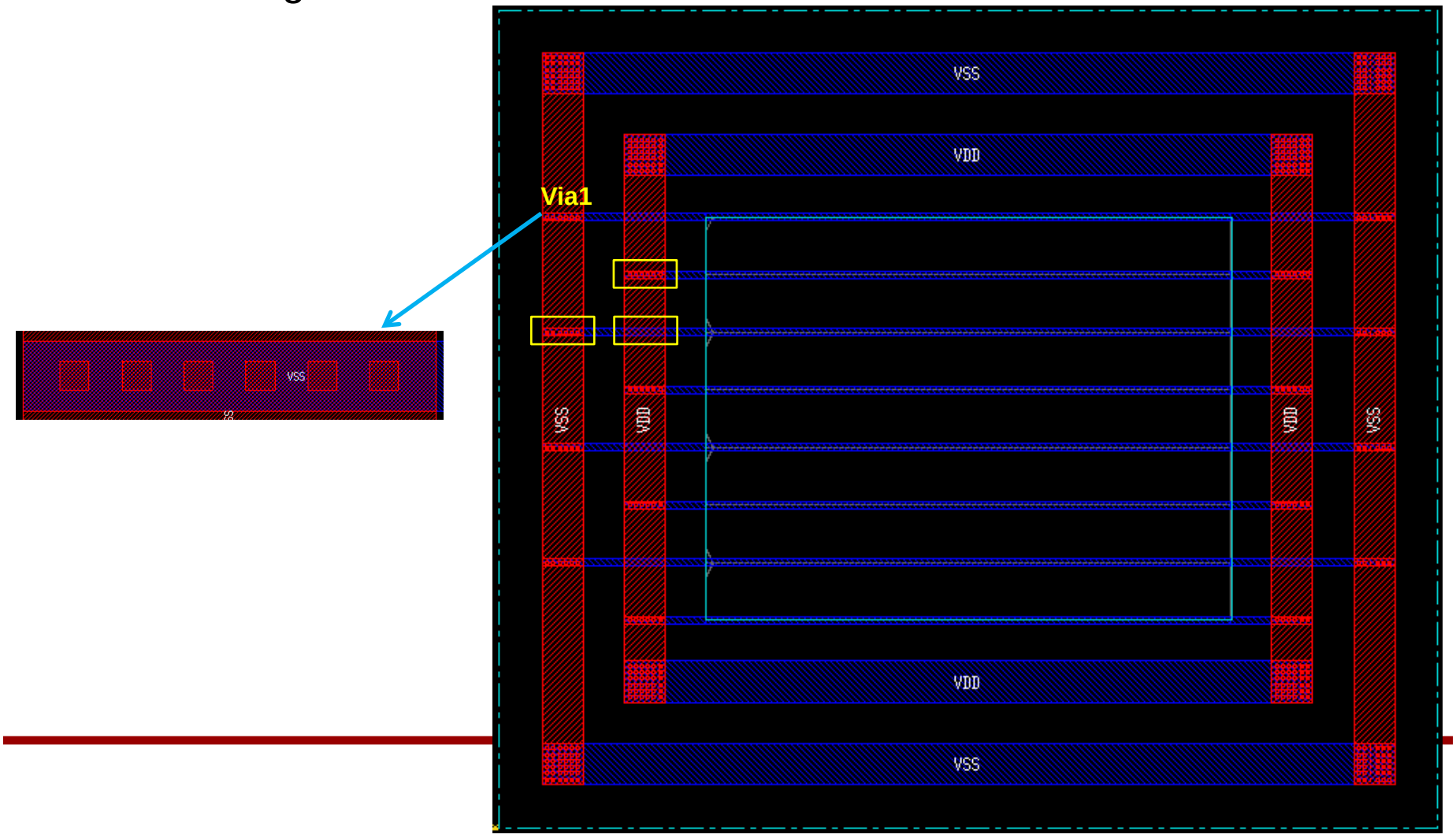
- Power/ground rings





Physical Design

- Power/ground lines

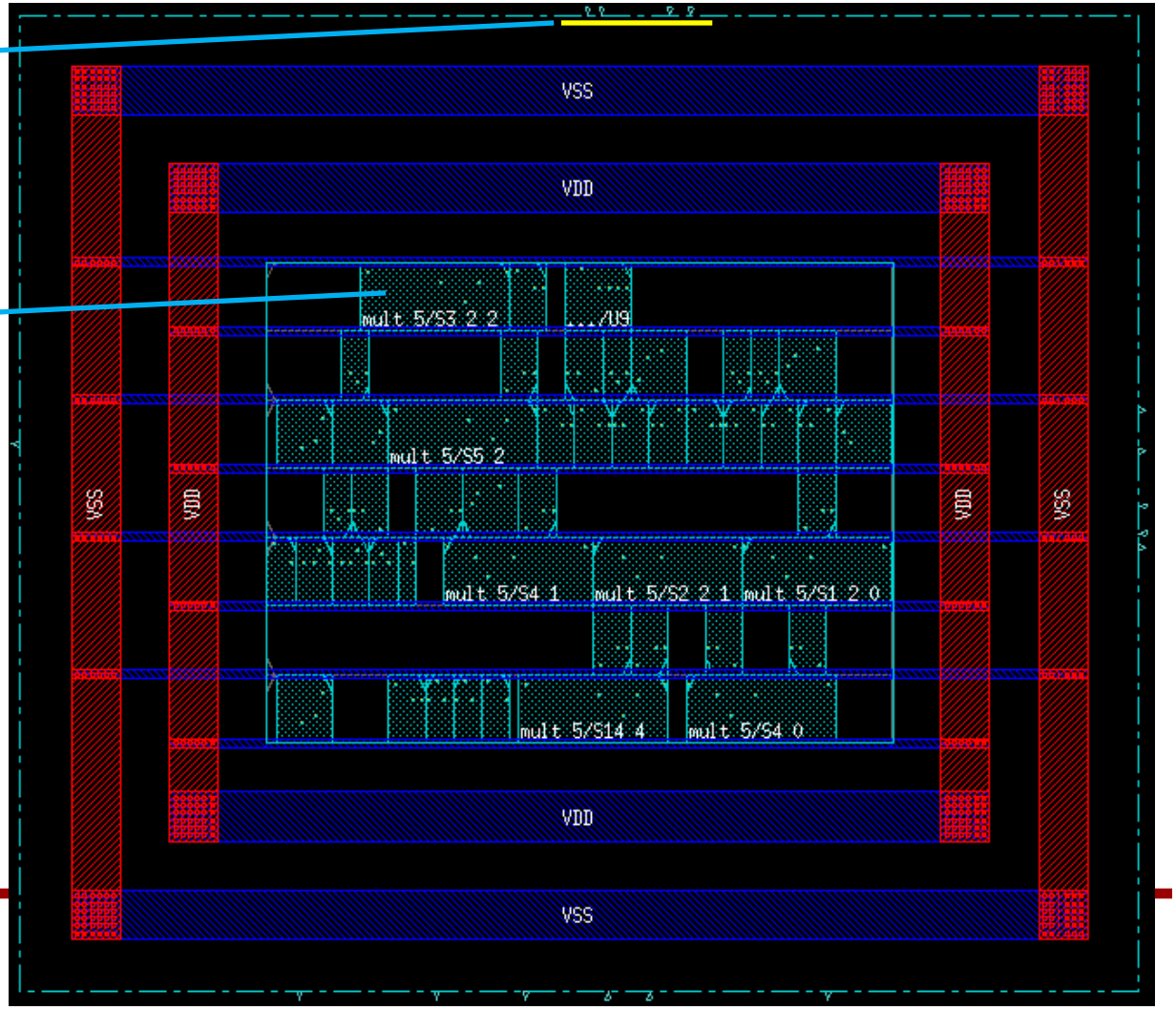


Physical Design

- Placement

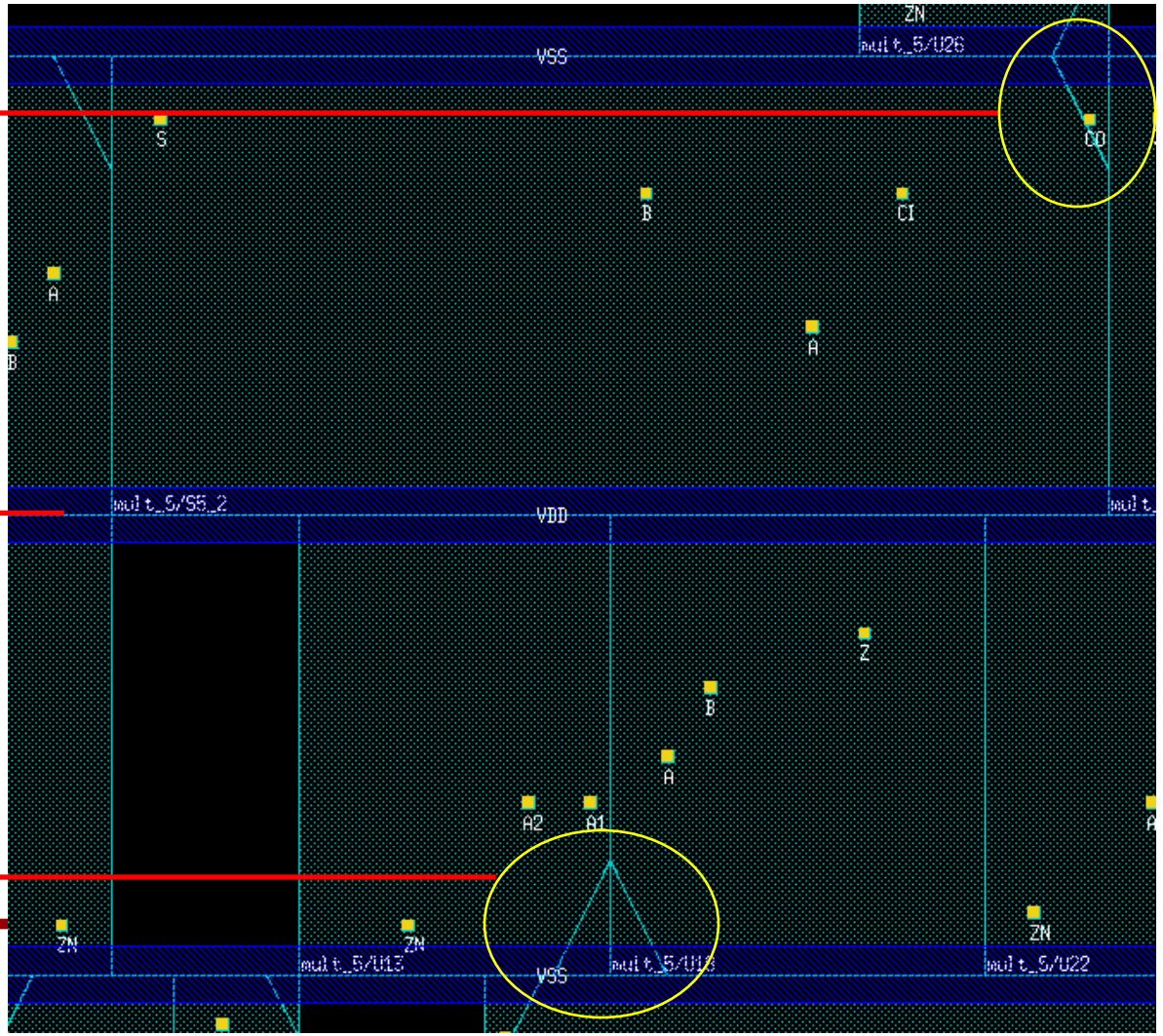
Primary input/output ports

Standard cells



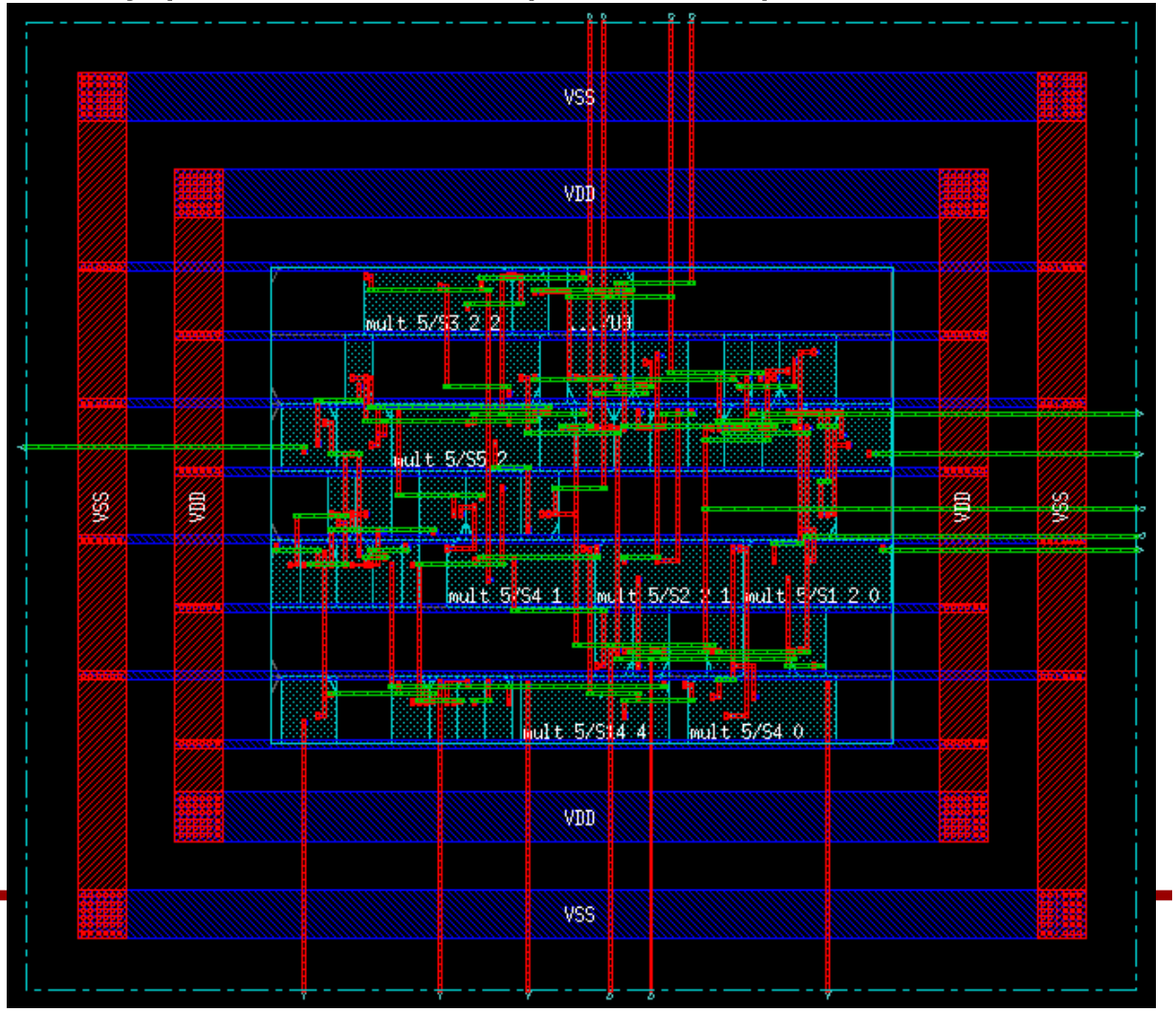
Physical Design

- Standard cells



Physical Design

- Trial route (automatically performed after placement)



Physical Design

- Timing analysis (Pre-CTS / setup time)

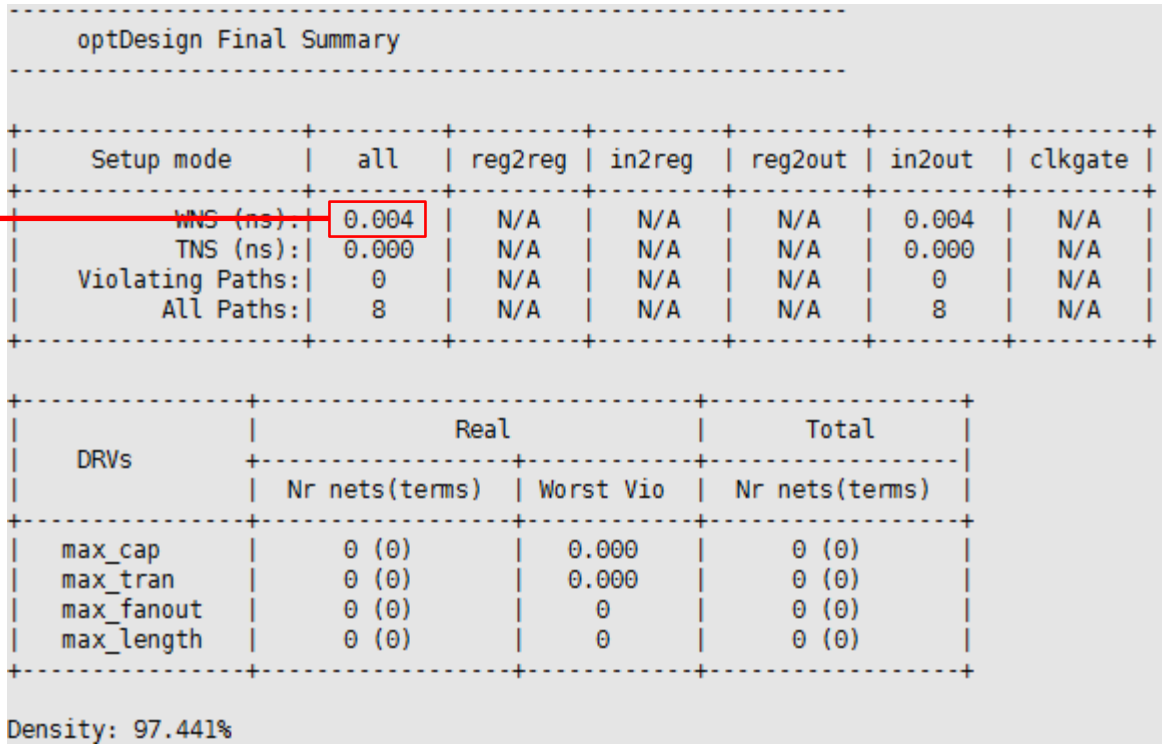
```
Path 1: VIOLATED Path Delay Check
Endpoint:   poutM[7] (^)
Beginpoint: pinB[2]  (^) triggered by  leading edge of '@'
Analysis View: NG_view_typ
- External Delay                0.000
+ Path Delay                    0.300
= Required Time                 0.300
- Arrival Time                  0.398
= Slack Time                   -0.098
     Clock Rise Edge                      0.000
     + Input Delay                        0.000
     = Beginpoint Arrival Time            0.000
     +-------------------------------------------------------------------------+
     |   Instance    |     Arc      |   Cell   | Delay | Arrival | Required |
     |               |              |          |       |  Time   |   Time   |
     |---------------+--------------+----------+-------+---------+----------|
     |               | pinB[2] ^    |          |       |   0.000 |   -0.098 |
     | mult_5/U9     | A4 ^ -> ZN ^ | AND4_X2  | 0.052 |   0.052 |   -0.047 |
     | mult_5/S3_2_2 | CI ^ -> S v  | FA_X1    | 0.095 |   0.147 |    0.049 |
     | mult_5/S4_1   | A v -> S ^   | FA_X1    | 0.119 |   0.266 |    0.168 |
     | mult_5/S14_4  | CI ^ -> CO ^ | FA_X1    | 0.049 |   0.315 |    0.216 |
     | mult_5/U15    | A1 ^ -> ZN v | NAND2_X1 | 0.014 |   0.328 |    0.230 |
     | mult_5/U41    | B1 v -> ZN ^ | OAI21_X1 | 0.031 |   0.359 |    0.261 |
     | mult_5/U42    | A ^ -> ZN ^  | XNOR2_X1 | 0.039 |   0.398 |    0.300 |
     |               | poutM[7] ^   |          | 0.000 |   0.398 |    0.300 |
     +-------------------------------------------------------------------------+
```

negative slack

Physical Design

- Optimization

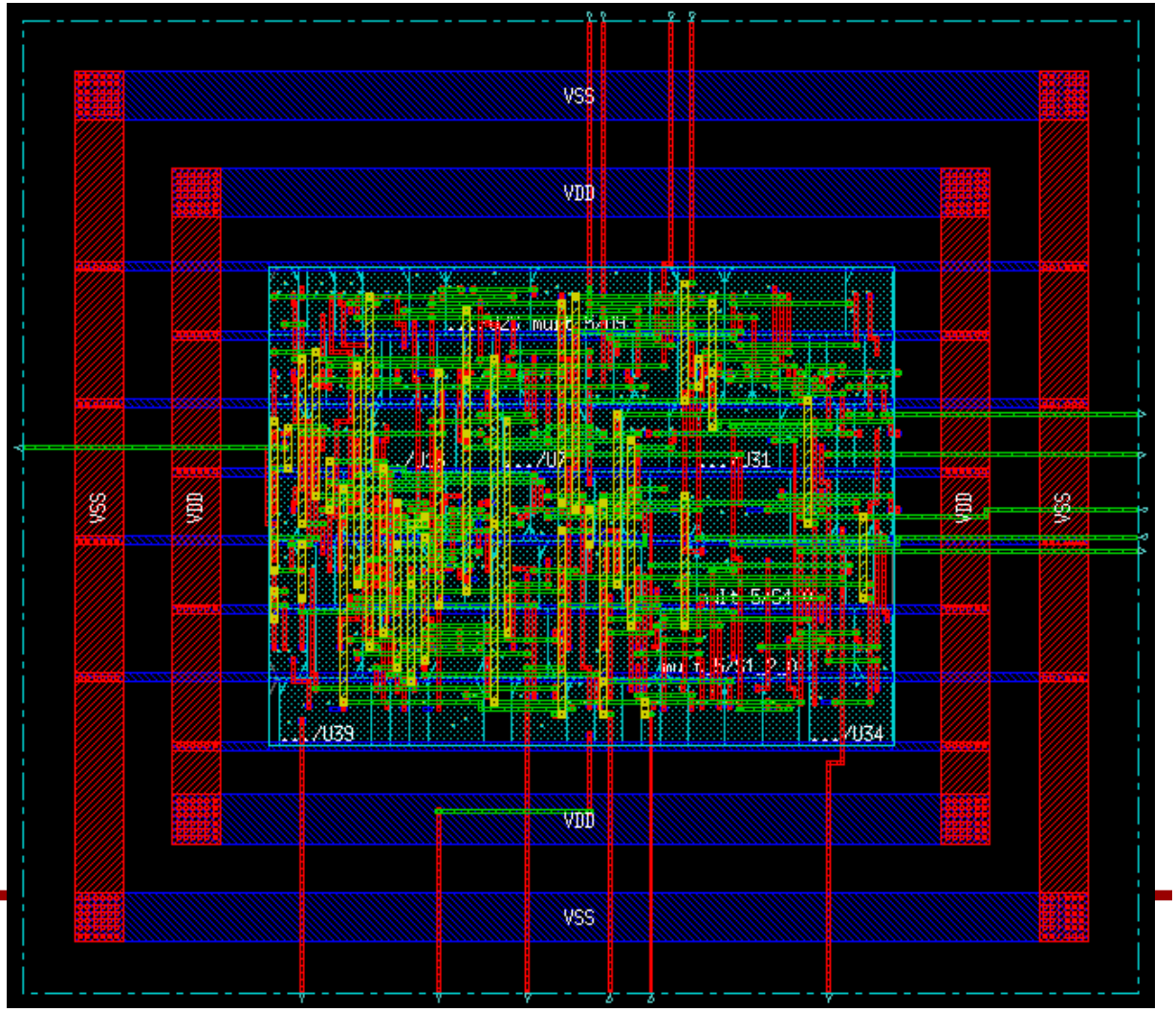
positive slack



```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.004  |   N/A   |   N/A   |   N/A   |  0.004  |   N/A   |
|           TNS (ns):|  0.000  |   N/A   |   N/A   |   N/A   |  0.000  |   N/A   |
|    Violating Paths:|    0    |   N/A   |   N/A   |   N/A   |    0    |   N/A   |
|          All Paths:|    8    |   N/A   |   N/A   |   N/A   |    8    |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 97.441%
```

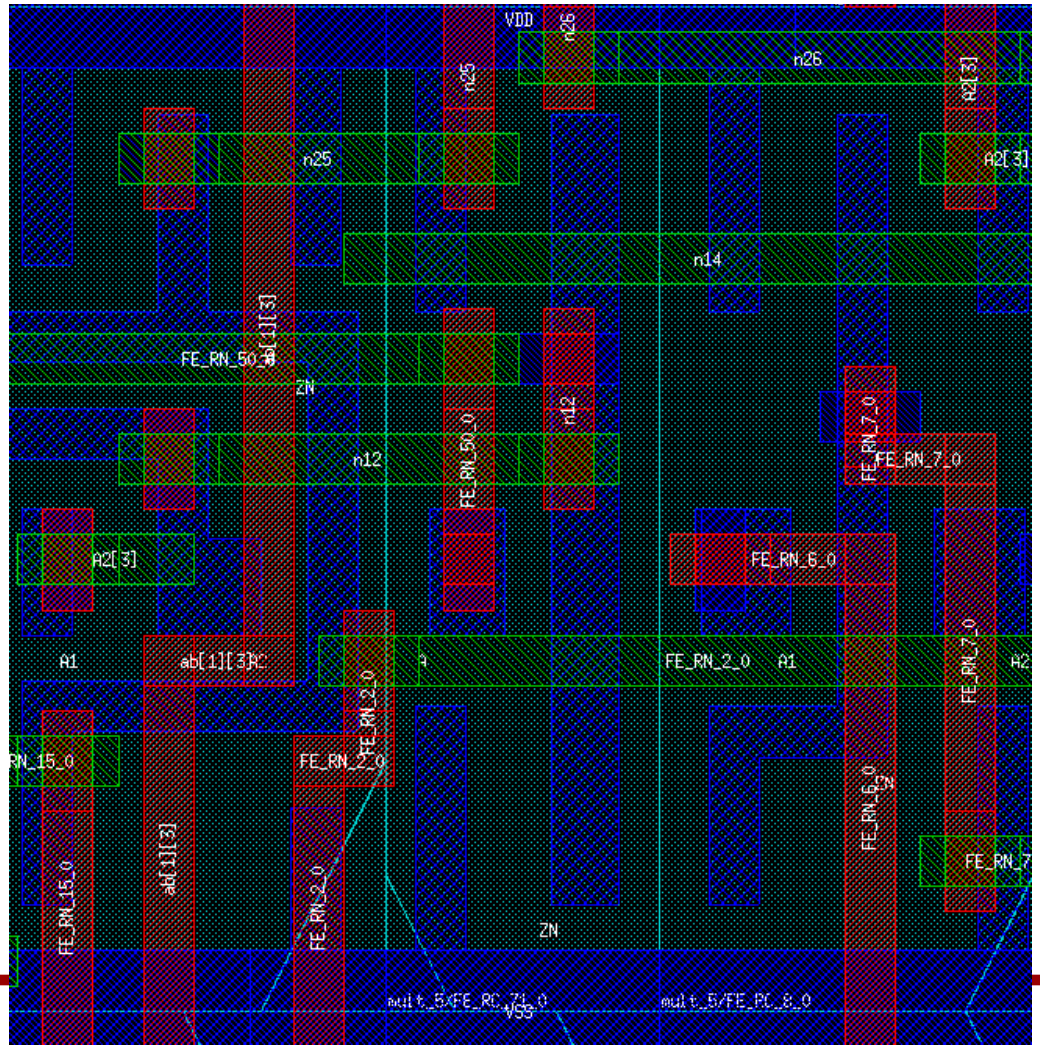
Physical Design

- Routing



Physical Design

- Routing



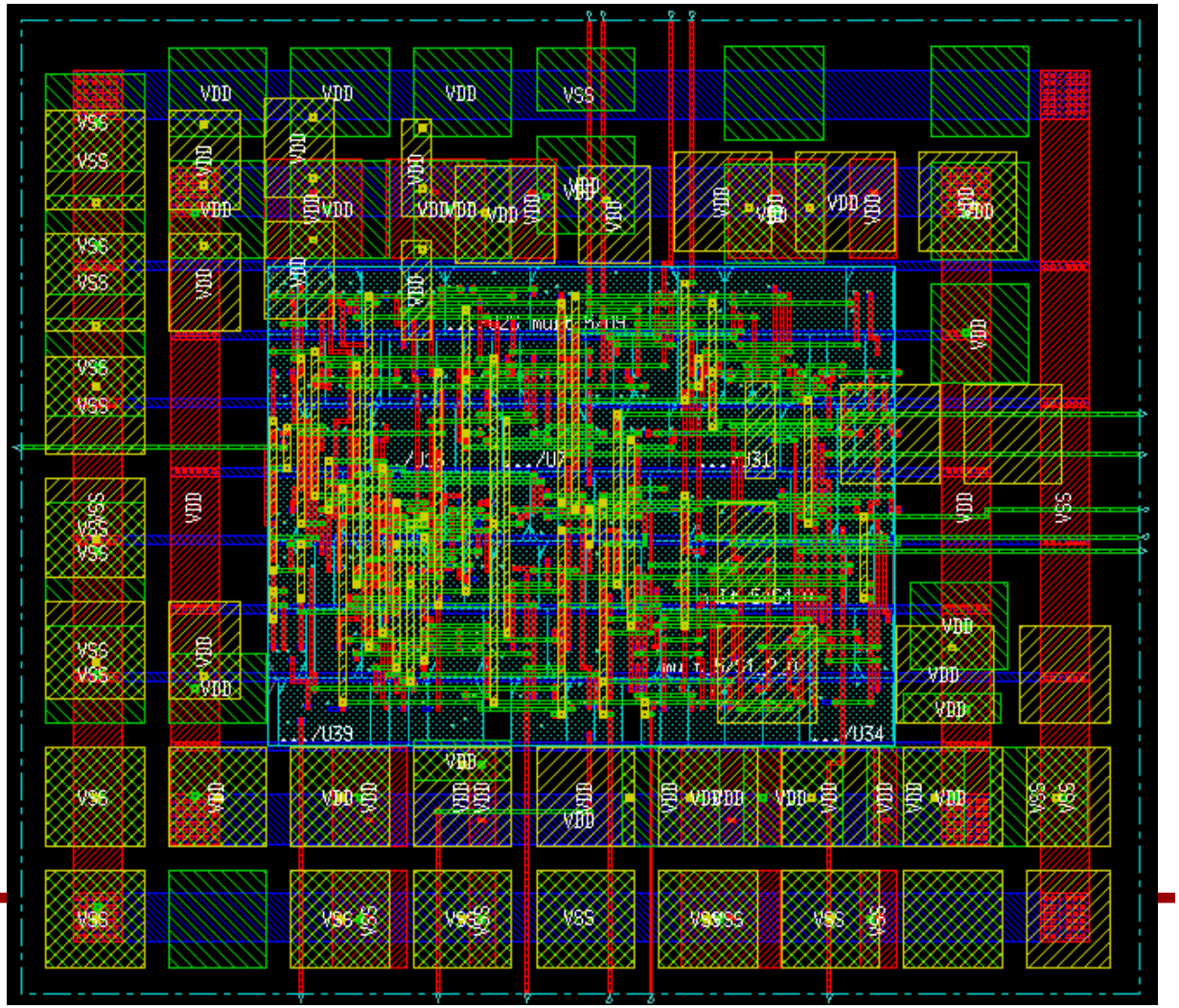
Physical Design

- Timing analysis (Post-Route / setup time)

```
Path 1: MET Path Delay Check
Endpoint:   poutM[7] (v)
Beginpoint: pinB[1]  (v) triggered by  leading edge of '@'
Analysis View: NG_view_typ
- External Delay                0.000
+ Path Delay                    0.300
= Required Time                 0.300
- Arrival Time                  0.298
= Slack Time                    0.002
     Clock Rise Edge                        0.000
     + Input Delay                          0.000
     = Beginpoint Arrival Time              0.000
     +-------------------------------------------------------------------------+
     |     Instance      |     Arc      |   Cell   | Delay | Arrival | Required |
     |                   |              |          |       |  Time   |   Time   |
     |-------------------+--------------+----------+-------+---------+----------|
     |                   | pinB[1] v    |          |       |   0.000 |    0.002 |
     | mult_5/U6         | A2 v -> ZN ^ | NAND2_X2 | 0.014 |   0.014 |    0.017 |
     | mult_5/FE_RC_68_0 | A ^ -> ZN ^  | XNOR2_X2 | 0.034 |   0.049 |    0.051 |
     | mult_5/FE_RC_69_0 | A ^ -> ZN v  | INV_X1   | 0.011 |   0.060 |    0.063 |
     | mult_5/S1_2_0     | CI v -> CO v | FA_X1    | 0.072 |   0.132 |    0.134 |
     | mult_5/S4_0       | A v -> CO v  | FA_X1    | 0.081 |   0.213 |    0.216 |
     | mult_5/FE_RC_0_0  | A1 v -> ZN ^ | NAND2_X2 | 0.018 |   0.231 |    0.233 |
     | mult_5/FE_RC_2_0  | A ^ -> ZN v  | INV_X2   | 0.011 |   0.242 |    0.244 |
     | mult_5/U15        | A1 v -> ZN ^ | NAND2_X2 | 0.012 |   0.254 |    0.257 |
     | mult_5/U41        | B1 ^ -> ZN v | OAI21_X2 | 0.014 |   0.268 |    0.270 |
     | mult_5/FE_RC_34_0 | A1 v -> ZN ^ | NAND2_X1 | 0.014 |   0.282 |    0.285 |
     | mult_5/FE_RC_33_0 | A ^ -> ZN v  | OAI21_X1 | 0.015 |   0.298 |    0.300 |
     |                   | poutM[7] v   |          | 0.000 |   0.298 |    0.300 |
     +-------------------------------------------------------------------------+
```

Physical Design

- Metal fill insertion



Physical Design

- Timing analysis (Post-fill / setup time)

```
Path 1: MET Path Delay Check
Endpoint:   poutM[7] (v)
Beginpoint: pinB[1]  (v) triggered by  leading edge of '@'
Analysis View: NG_view_typ
- External Delay                0.000
+ Path Delay                    0.300
= Required Time                 0.300
- Arrival Time                  0.298
= Slack Time                    0.002
     Clock Rise Edge                        0.000
     + Input Delay                          0.000
     = Beginpoint Arrival Time              0.000
     +-------------------------------------------------------------------------+
     |     Instance      |     Arc      |   Cell   | Delay | Arrival | Required |
     |                   |              |          |       |  Time   |   Time   |
     |-------------------+--------------+----------+-------+---------+----------|
     |                   | pinB[1] v    |          |       |   0.000 |    0.002 |
     | mult_5/U6         | A2 v -> ZN ^ | NAND2_X2 | 0.014 |   0.014 |    0.017 |
     | mult_5/FE_RC_68_0 | A ^ -> ZN ^  | XNOR2_X2 | 0.034 |   0.049 |    0.051 |
     | mult_5/FE_RC_69_0 | A ^ -> ZN v  | INV_X1   | 0.011 |   0.060 |    0.063 |
     | mult_5/S1_2_0     | CI v -> CO v | FA_X1    | 0.072 |   0.132 |    0.134 |
     | mult_5/S4_0       | A v -> CO v  | FA_X1    | 0.081 |   0.213 |    0.215 |
     | mult_5/FE_RC_0_0  | A1 v -> ZN ^ | NAND2_X2 | 0.018 |   0.231 |    0.233 |
     | mult_5/FE_RC_2_0  | A ^ -> ZN v  | INV_X2   | 0.011 |   0.242 |    0.244 |
     | mult_5/U15        | A1 v -> ZN ^ | NAND2_X2 | 0.012 |   0.254 |    0.256 |
     | mult_5/U41        | B1 ^ -> ZN v | OAI21_X2 | 0.014 |   0.268 |    0.270 |
     | mult_5/FE_RC_34_0 | A1 v -> ZN ^ | NAND2_X1 | 0.014 |   0.282 |    0.285 |
     | mult_5/FE_RC_33_0 | A ^ -> ZN v  | OAI21_X1 | 0.015 |   0.298 |    0.300 |
     |                   | poutM[7] v   |          | 0.000 |   0.298 |    0.300 |
     +-------------------------------------------------------------------------+
```

Physical Design

- Sign-off analysis

```
Startpoint: pinB[3] (input port)
Endpoint: poutM[7] (output port)
Path Group: **default**
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
pinB[3] (in)                             0.00 &     0.00 r
FE_RC_72_0/ZN (NAND2_X2)                 0.01 &     0.01 f
FE_RC_73_0/ZN (INV_X4)                   0.01 &     0.03 r
FE_RC_22_0/ZN (INV_X1)                   0.01 &     0.04 f
FE_RC_20_0/ZN (NAND2_X1)                 0.02 &     0.05 r
FE_RC_18_0/ZN (NAND2_X1)                 0.02 &     0.07 f
FE_RC_17_0/ZN (NAND2_X1)                 0.02 &     0.09 r
FE_RC_16_0/ZN (NAND2_X2)                 0.02 &     0.11 f
FE_RC_51_0/ZN (NAND2_X2)                 0.02 &     0.13 r
FE_RC_49_0/ZN (OAI21_X2)                 0.02 &     0.15 f
FE_RC_83_0/ZN (NAND2_X2)                 0.01 &     0.17 r
FE_RC_82_0/ZN (OAI21_X1)                 0.02 &     0.19 f
FE_RC_81_0/ZN (INV_X2)                   0.02 &     0.20 r
FE_RC_0_0/ZN (NAND2_X2)                  0.01 &     0.22 f
FE_RC_2_0/ZN (INV_X2)                    0.02 &     0.24 r
U15/ZN (NAND2_X2)                        0.01 &     0.25 f
U41/ZN (OAI21_X2)                        0.03 &     0.28 r
FE_RC_34_0/ZN (NAND2_X1)                 0.02 &     0.29 f
FE_RC_33_0/ZN (OAI21_X1)                 0.02 &     0.31 r
poutM[7] (out)                           0.00 &     0.31 r
data arrival time                                   0.31

max_delay                                0.30       0.30
output external delay                    0.00       0.30
data required time                                  0.30
-----------------------------------------------------------
data required time                                  0.30
data arrival time                                  -0.31
-----------------------------------------------------------
slack (VIOLATED)                                   -0.01
```

Physical Design

- Delay calculation
  - Elmore delay
  - Look-up table
  - Asymptotic waveform evaluation (AWE)

- Timing analysis
  - Setup time
  - Hold time