# EE434
# ASIC & Digital Systems

**Testing**

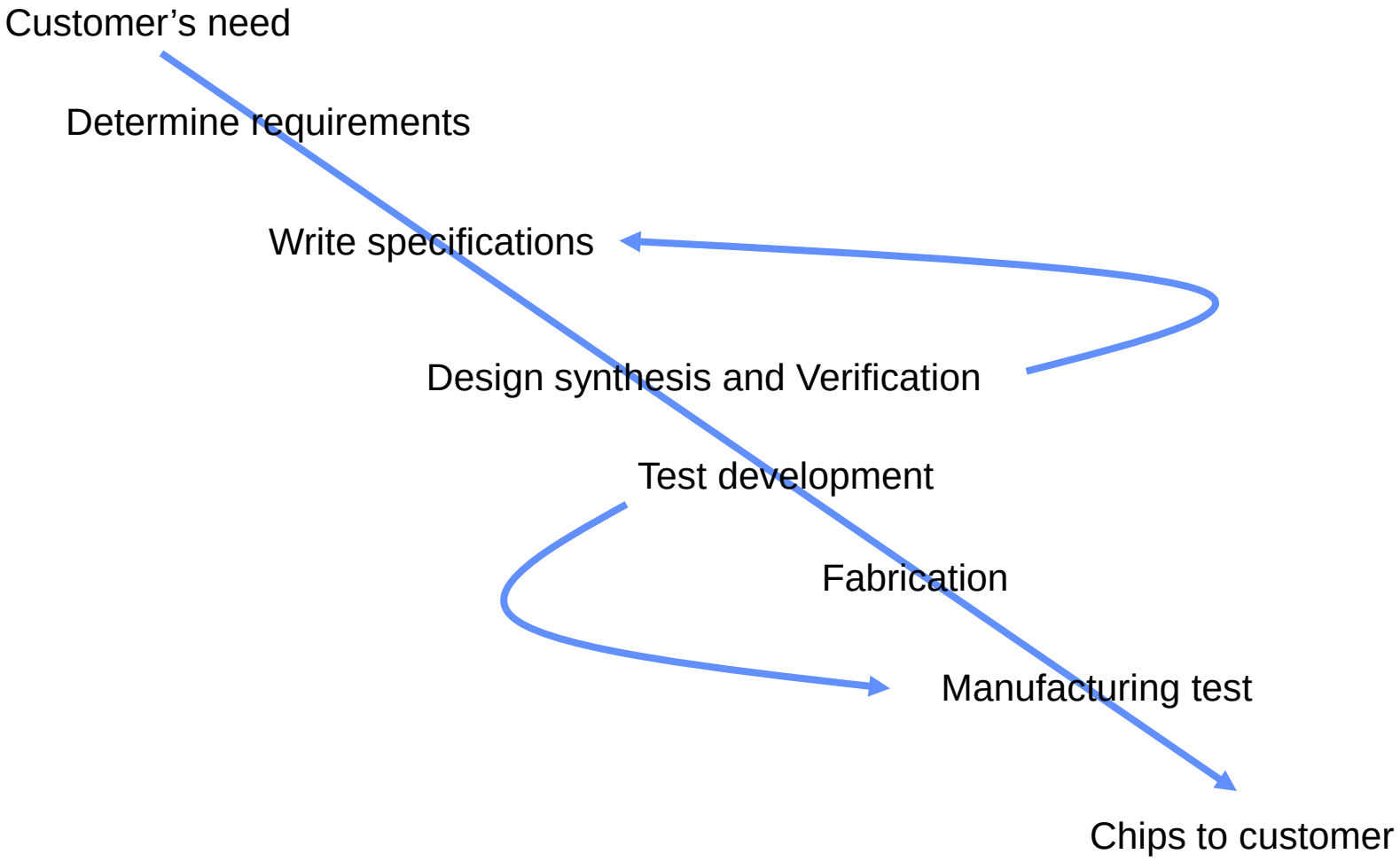
Spring 2015

Dae Hyun Kim
daehyun@eecs.wsu.edu

# Introduction

- VLSI realization process
- Verification and test
- Ideal and real tests
- Costs of testing
- Roles of testing
- A modern VLSI device - system-on-a-chip

# VLSI Realization Process



# Verification vs. Test

- Verification
  - Verifies correctness of design.
  - Performed by simulation, hardware emulation, or formal methods.
  - Performed once prior to manufacturing.
  - Responsible for quality of design.

- Test
  - Verifies correctness of manufactured hardware.
  - Two-part process:
    - 1. Test generation: software process executed once during design
    - 2. Test application: electrical tests applied to hardware
  - Test application performed on every manufactured device.
  - Responsible for quality of devices.

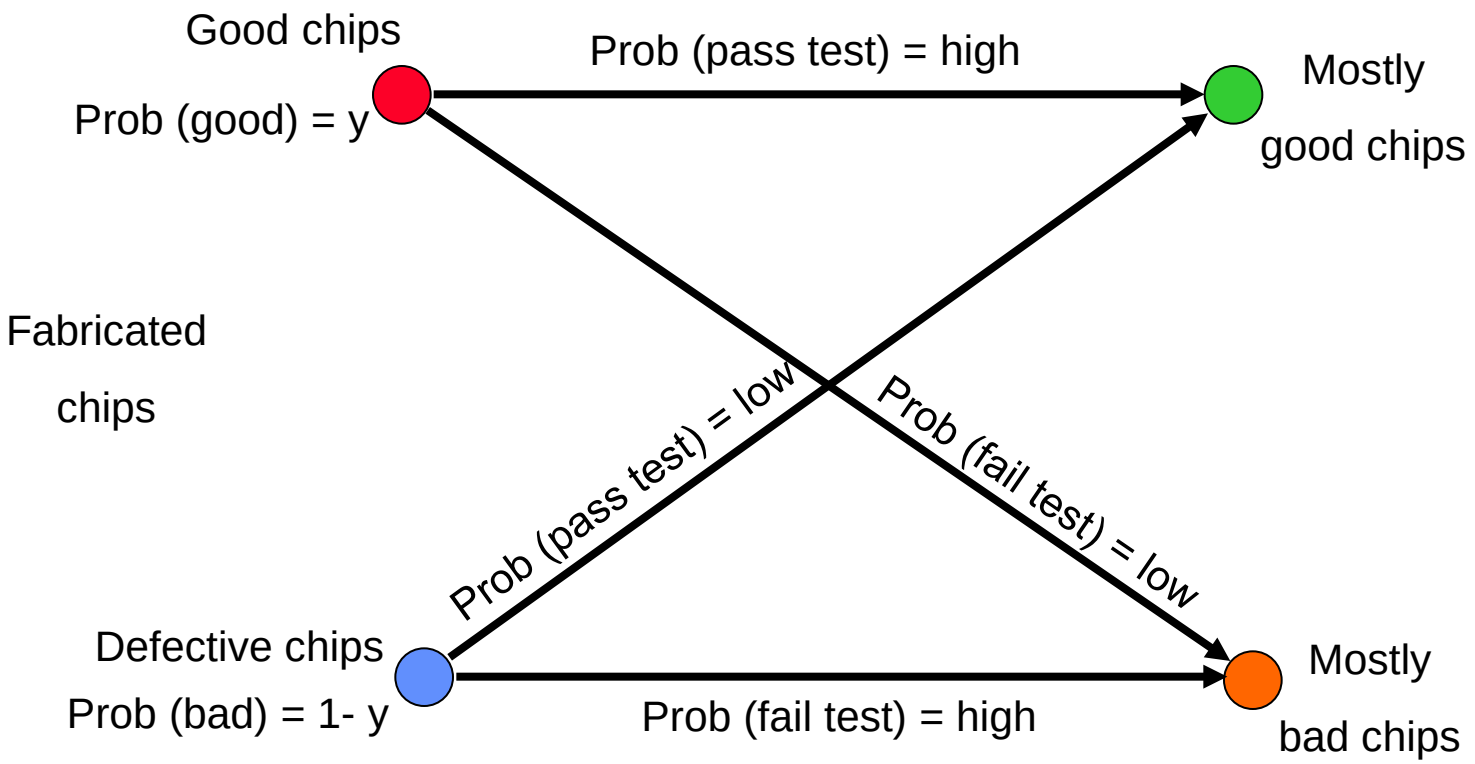
# Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

# Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*

# Testing as Filter Process

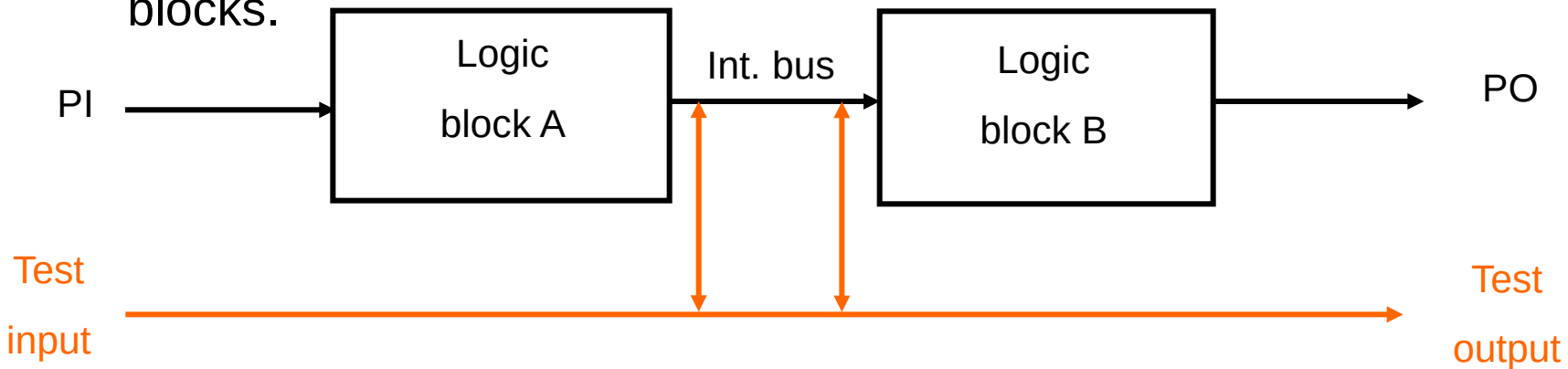


# Cost of Testing

- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

# Design for Testability (DFT)

- *DFT refers to hardware design styles or added hardware that reduces test generation complexity.*
- Motivation: Test generation complexity increases exponentially with the size of the circuit.
- Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.



# Cost of Manufacturing Testing in 2000

- 0.5-1.0GHz, analog instruments,1,024 digital pins: ATE purchase price
  - $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  - Depreciation + Maintenance + Operation
  - $0.854M + $0.085M + $0.5M = $1.439M/year
- Test cost (24 hour ATE operation)
  - $1.439M/(365 x 24 x 3,600)
  - 4.5 cents/second

# Roles of Testing

- Detection: Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- *Failure mode analysis* (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

# VLSI Testing Process and Equipment

- Motivation
- Types of Testing
- Test Specifications and Plan
- Test Programming
- Test Data Analysis
- Automatic Test Equipment
- Parametric Testing
- Summary

# Motivation

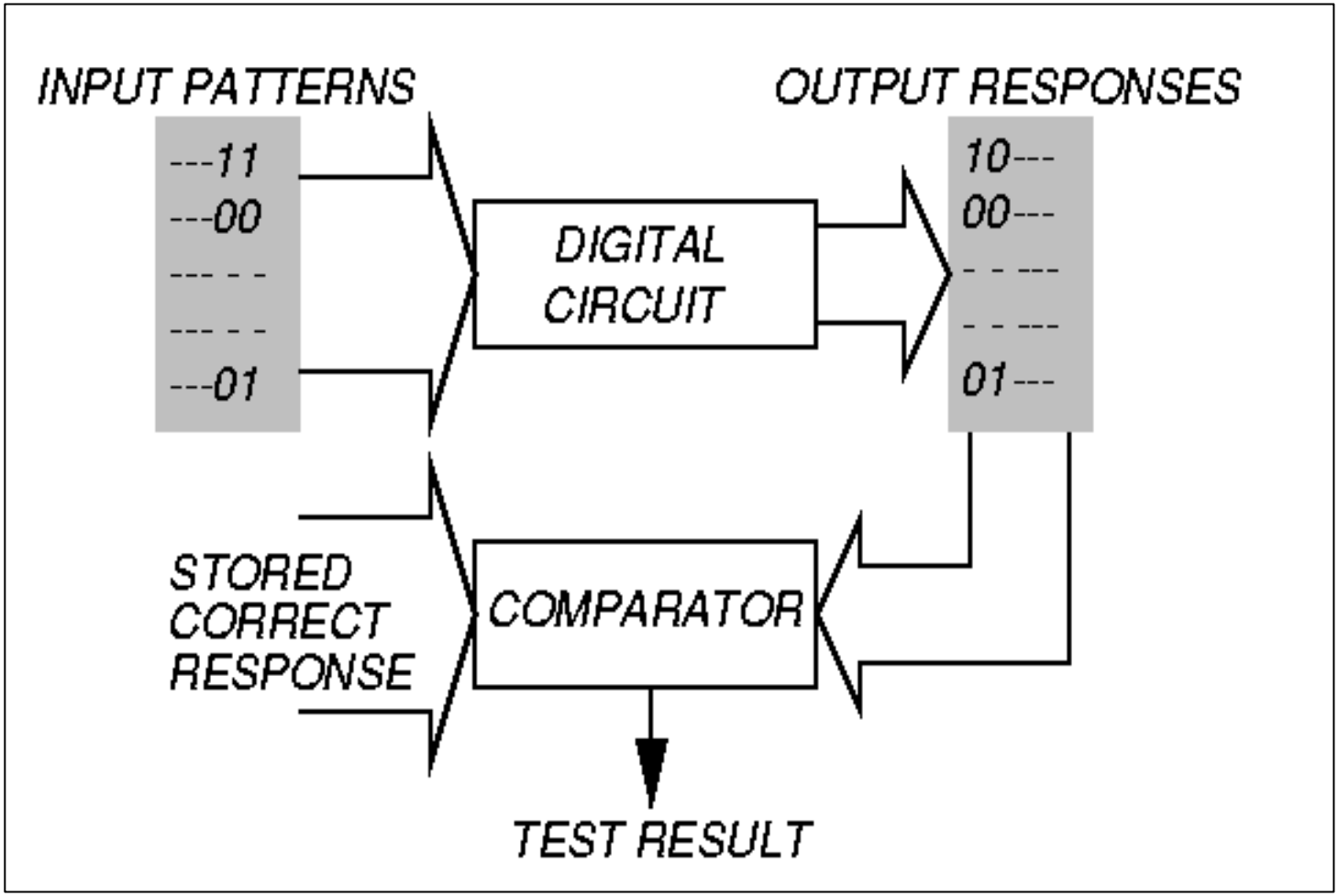
- **Need to understand some *Automatic Test Equipment* (ATE) technology**
  - **Influences what tests are possible**
  - **Serious analog measurement limitations at high digital frequency or in the analog domain**
  - **Need to understand capabilities for digital logic, memory, and analog test in *System-on-a-Chip* (SOC) technology**

- **Need to understand parametric testing**
  - **Used to take setup, hold time measurements**
  - **Use to compute $V_{IL}$ , $V_{IH}$ , $V_{OL}$ , $V_{OH}$ , $t_r$ , $t_f$ , $t_d$ , $I_{OL}$, $I_{OH}$ , $I_{IL}$, $I_{IH}$**

# Types of Testing

- ***Verification testing*, *characterization testing*, or *design debug***
  - **Verifies correctness of design and of test procedure – usually requires correction to design**
- ***Manufacturing testing***
  - **Factory testing of all manufactured chips for parametric faults and for random defects**
- ***Acceptance testing* (*incoming inspection*)**
  - **User (customer) tests purchased parts to ensure quality**

# Testing Principle



# Automatic Test Equipment Components

- **Consists of:**
  - **Powerful computer**
  - **Powerful 32-bit *Digital Signal Processor* (DSP) for analog testing**
  - **Test Program (written in high-level language) running on the computer**
  - **Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)**
  - ***Probe Card* or *Membrane Probe* (contains electronics to measure signals on chip pin or pad)**

# Verification Testing

- **Very expensive**

- **May comprise:**
  - **Scanning Electron Microscope tests**
  - **Bright-Lite detection of defects**
  - **Electron beam testing**
  - **Artificial intelligence (expert system) methods**
  - **Repeated functional tests**

# Characterization Test

- **Worst-case test**
  - **Choose test that passes/fails chips**
  - **Select statistically significant sample of chips**
  - **Repeat test for every combination of 2+ environmental variables**
  - **Diagnose and correct design errors**

- **Continue throughout production life of chips to improve design and process to increase yield**

# Manufacturing Test

- **Determines whether manufactured chip meets specs**
- **Must cover high % of modeled faults**
- **Must minimize test time (to control cost)**
- **No fault diagnosis**
- **Tests every device on chip**
- **Test at speed of application or speed guaranteed by supplier**

# Burn-In or Stress Test

- **Process:**
  - **Subject chips to high temperature & over-voltage supply, while running production tests**

- **Catches:**
  - ***Infant mortality* cases – these are damaged chips that will fail in the first 2 days of operation – causes bad devices to actually fail before chips are shipped to customers**
  - ***Freak failures* – devices having same failure mechanisms as reliable devices**

# Incoming Inspection

- **Can be:**
  - **Similar to production testing**
  - **More comprehensive than production testing**
  - **Tuned to specific systems application**

- **Often done for a random sample of devices**
  - ***Sample size* depends on device quality and system reliability requirements**
  - **Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost**

# Types of Manufacturing Tests

- ***Wafer sort* or *probe* test – done before wafer is scribed and cut into chips**
  - **Includes test site characterization – specific test devices are checked with specific patterns to measure:**
    - **Gate threshold**
    - **Polysilicon field threshold**
    - **Poly sheet resistance, etc.**

- **Packaged device tests**

# Sub-Types of Tests

- ***Parametric*** **– measures electrical properties of pin electronics – delay, voltages, currents, etc. – fast and cheap**

- ***Functional*** **– used to cover very high % of modeled faults – test every transistor and wire in digital circuits – long and expensive – main topic of tutorial**

# Two Different Meanings of Functional Test

- ***ATE and Manufacturing World*** **– any vectors applied to cover high % of faults during manufacturing test**

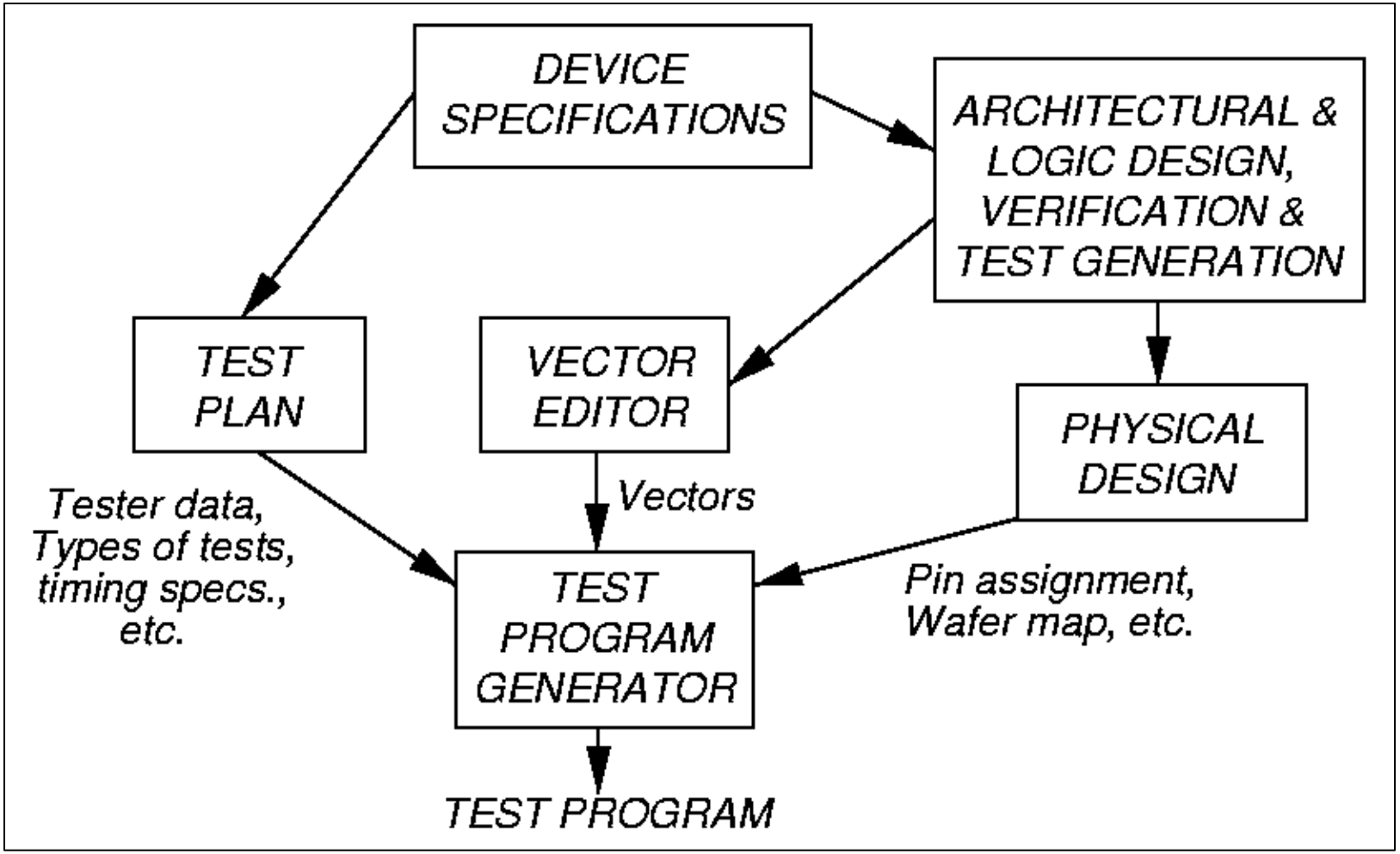
- ***Automatic Test-Pattern Generation World*** **– testing with *verification vectors*, which determine whether hardware matches its specification – typically have low fault coverage (< 70 %)**

# Test Specifications & Plan

- **Test Specifications:**
  - **Functional Characteristics**
  - **Type of *Device Under Test* (DUT)**
  - **Physical Constraints – Package, pin numbers, etc.**
  - **Environmental Characteristics – supply, temperature, humidity, etc.**
  - **Reliability – acceptance quality level (defects/million), failure rate, etc.**

- **Test plan generated from specifications**
  - **Type of test equipment to use**
  - **Types of tests**
  - **Fault coverage requirement**

# Test Programming



# Test Data Analysis

- **Uses of ATE test data:**
  - **Reject bad DUTS**
  - **Fabrication process information**
  - **Design weakness information**

- **Devices that did not fail are good only if tests covered 100% of faults**

- ***Failure mode analysis* (FMA)**
  - **Diagnose reasons for device failure, and find design and process weaknesses**
  - **Allows improvement of logic & layout design rules**