EE434
ASIC & Digital Systems

Test Methodologies

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Fault Modeling

- Why model faults?
- Some real defects in VLSI and PCB
- Common fault models
- Stuck-at faults
    - Single stuck-at faults
    - Fault equivalence
    - Fault dominance and checkpoint theorem
    - Classes of stuck-at faults and multiple faults
- Transistor faults
- Summary

Why Model Faults?

- **I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing)**
- **Real defects (often mechanical) too numerous and often not analyzable**
- **A fault model identifies targets for testing**
- **A fault model makes analysis possible**
- **Effectiveness measurable by experiments**

Functional vs. Structural Testing

- Consider testing of a ten-input AND function
- We apply an input pattern 0101010101
- Output is 0
- More than one inferences possible
- Functional test is necessary for verification
- The purpose of manufacturing test is to find any faults caused due to manufacturing defects

Some Real Defects in Chips

- Processing defects
  - Missing contact windows
  - Parasitic transistors
  - Oxide breakdown
  - . . .
- Material defects
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - . . .
- Time-dependent failures
  - Dielectric breakdown
  - Electromigration
  - . . .
- Packaging failures
  - Contact degradation
  - Seal leaks
  - . . .

Observed PCB Defects

Defect Classes	Occurrence Frequency (%)
Shorts	51
Opens	1
Missing components	6
Wrong components	13
Reversed components	6
Bent leads	8
Analog specifications	5
Digital logic	5
Performance (timing)	5

Ref.: J. Bateson, *In-Circuit Testing*, Van Nostrand Reinhold, 1985.

Common Fault Models

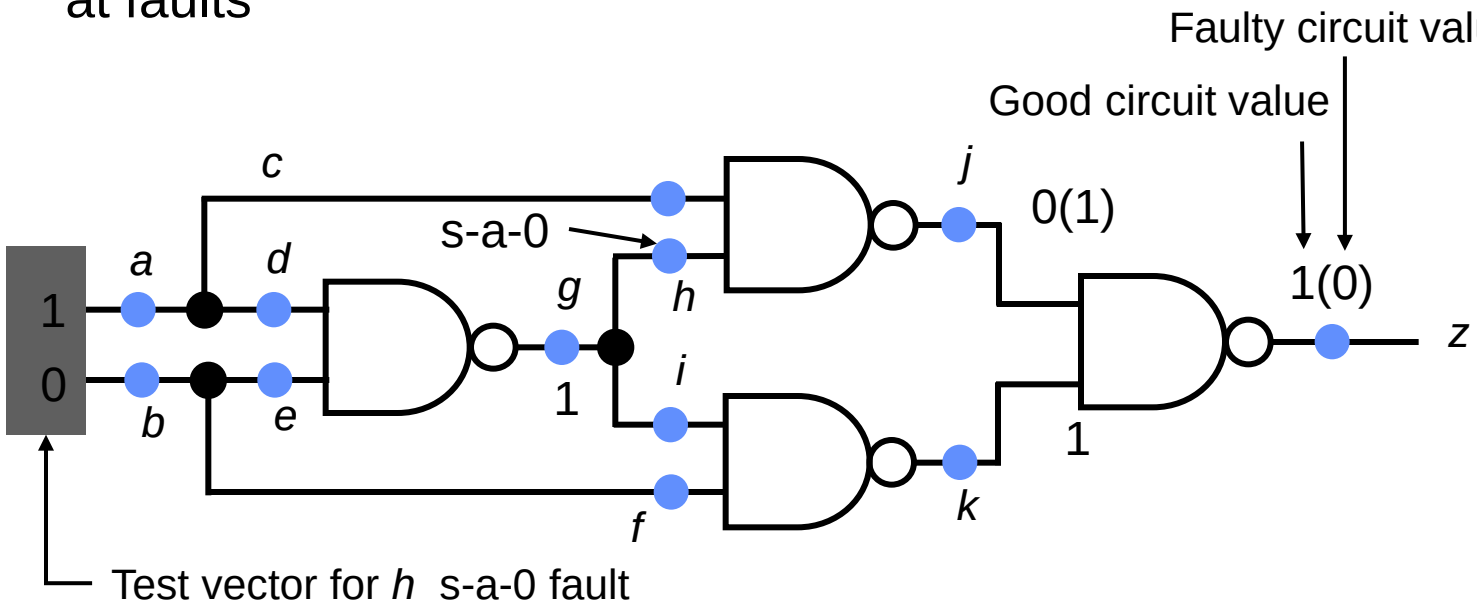
- **Single stuck-at faults**
- **Transistor open and short faults**
- **Memory faults**
- **PLA faults (stuck-at, cross-point, bridging)**
- **Functional faults (processors)**
- **Delay faults (transition, path)**
- **Analog faults**
- **For more examples, see Section 4.4 (p. 60-70) of the book.**

Stuck-at Fault

- The circuit is modeled as an interconnection of Boolean gates
- Each connecting line can have two types of faults
  - Stuck-at-1 (s-a-1) & Stuck-at-0 (s-a-0)
- A circuit with n lines can have 3^n-1 possible stuck line combinations
- An n-line circuit can have at most 2n single stuck-at faults

Single Stuck-at Fault

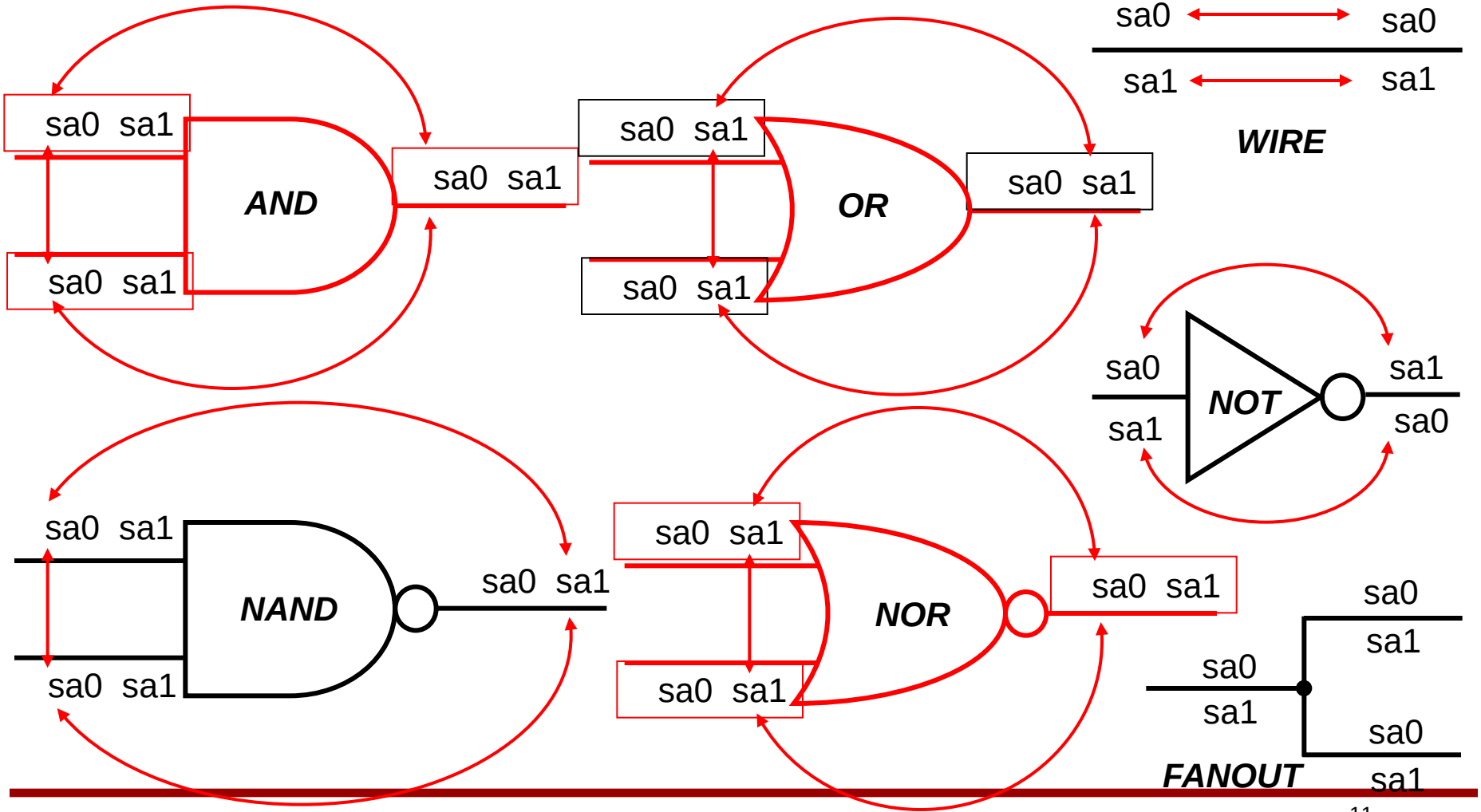
- Three properties define a single stuck-at fault
  - Only one line is faulty
  - The faulty line is permanently set to 0 or 1
  - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults



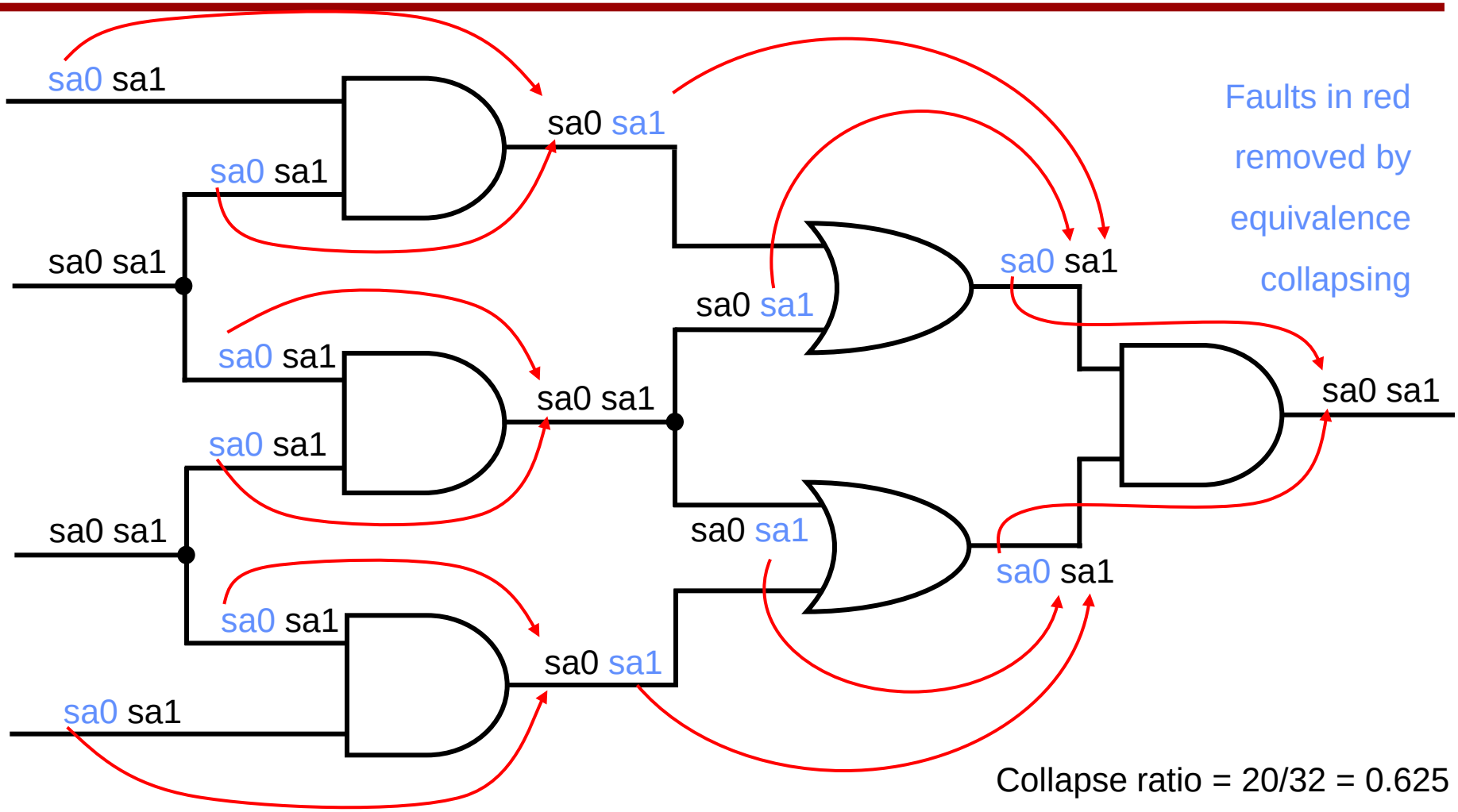
Fault Equivalence

- Number of fault sites in a Boolean gate circuit = #PI + #gates + # (fan-out branches).
- Fault equivalence: Two faults f1 and f2 are equivalent if all tests that detect f1 also detect f2.
- If faults f1 and f2 are equivalent then the corresponding faulty functions are identical.
- Fault collapsing: All single faults of a logic circuit can be divided into disjoint equivalence subsets, where all faults in a subset are mutually equivalent. A collapsed fault set contains one fault from each equivalence subset.

Equivalence Rules



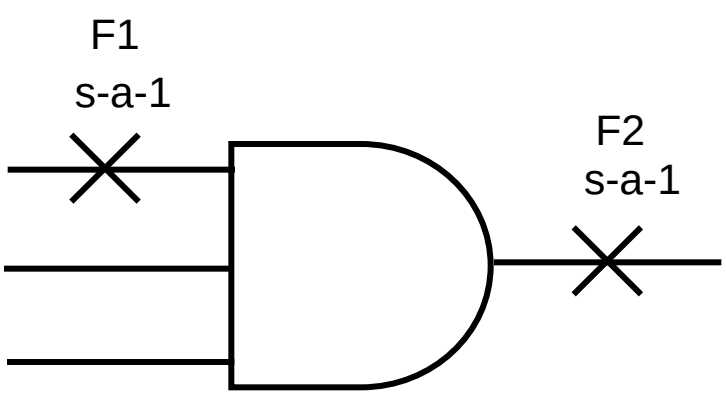
Equivalence Example

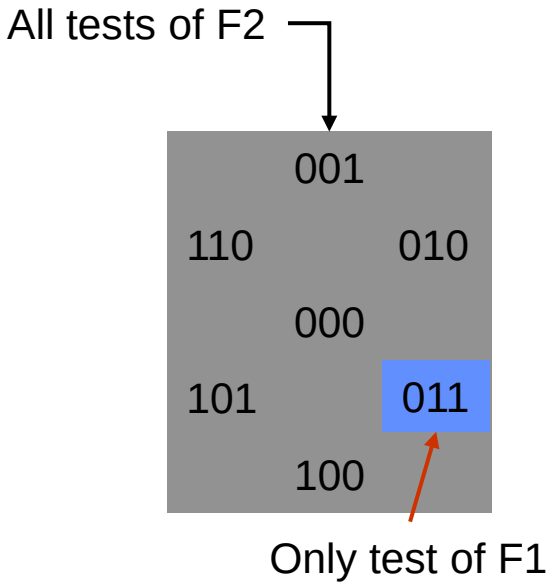


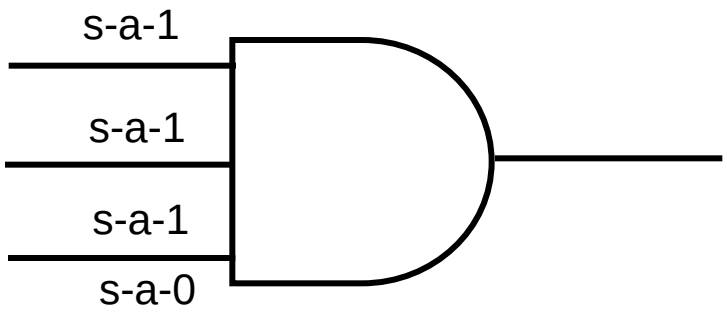
Fault Dominance

- If all tests of some fault F1 detect another fault F2, then F2 is said to dominate F1.
- Dominance fault collapsing: If fault F2 dominates F1, then F2 is removed from the fault list.
- When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates. See the next example.
- If two faults dominate each other then they are equivalent.

Dominance Example





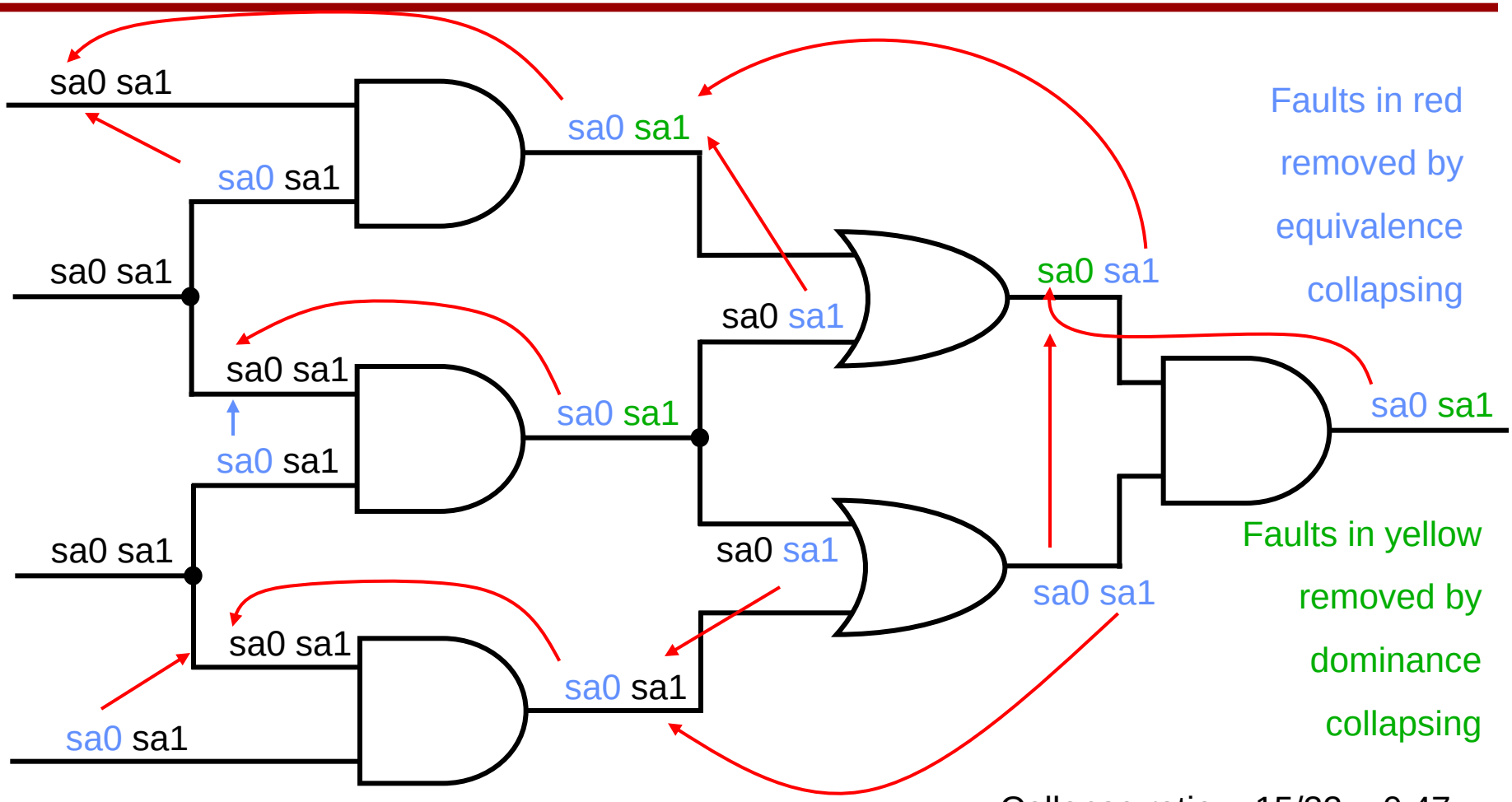


A dominance collapsed fault set

Dominance Fault Collapsing

- An n-input Boolean gate requires (n+1) single stuck-at faults to be modeled
- To collapse faults of a gate, all faults from the output can be eliminated retaining one type of fault on each input and the other type on any one of the inputs
- The output faults of the NOT gate, and the wire can be removed as long as both faults on the input are retained

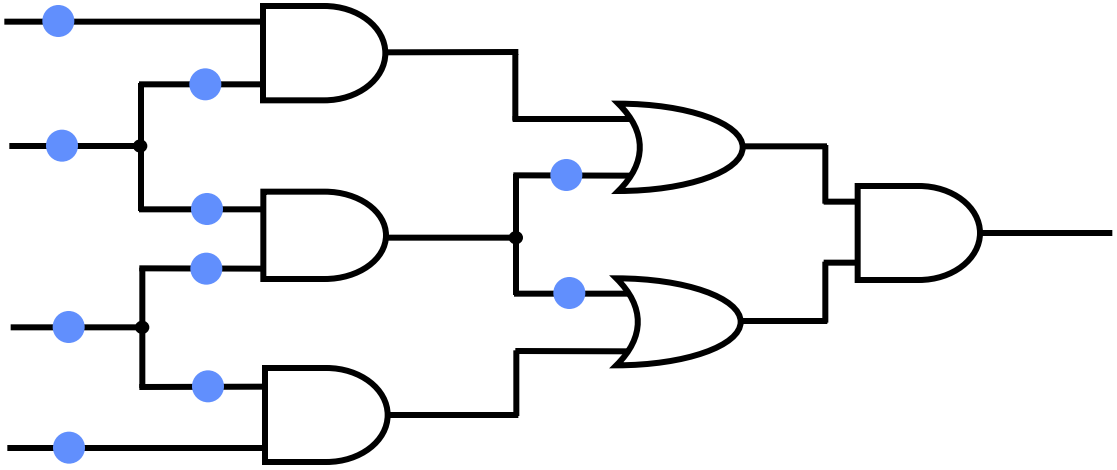
Dominance Example



Checkpoints

- Primary inputs and fan-out branches of a combinational circuit are called *checkpoints*.

- Checkpoint theorem: A test set that detects all single (multiple) stuck-at faults on all checkpoints of a combinational circuit, also detects all single (multiple) stuck-at faults in that circuit.



Total fault sites = 16

Checkpoints (●) = 10

Classes of Stuck-at Faults

- Following classes of single stuck-at faults are identified by fault simulators:
  - *Potentially-detectable fault*: Test produces an unknown (X) state at *primary output* (PO); detection is probabilistic, usually with 50% probability.
  - *Initialization fault*: Fault prevents initialization of the faulty circuit; can be detected as a potentially-detectable fault.
  - *Hyperactive fault*: Fault induces much internal signal activity without reaching PO.
  - *Redundant fault*: No test exists for the fault.
  - *Untestable fault*: Test generator is unable to find a test.

Multiple Stuck-at Faults

- A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.
- The total number of single and multiple stuck-at faults in a circuit with k single fault sites is 3^k-1.
- A single fault test can fail to detect the target fault if another fault is also present, however, such masking of one fault by another is rare.
- Statistically, single fault tests cover a very large number of multiple faults.

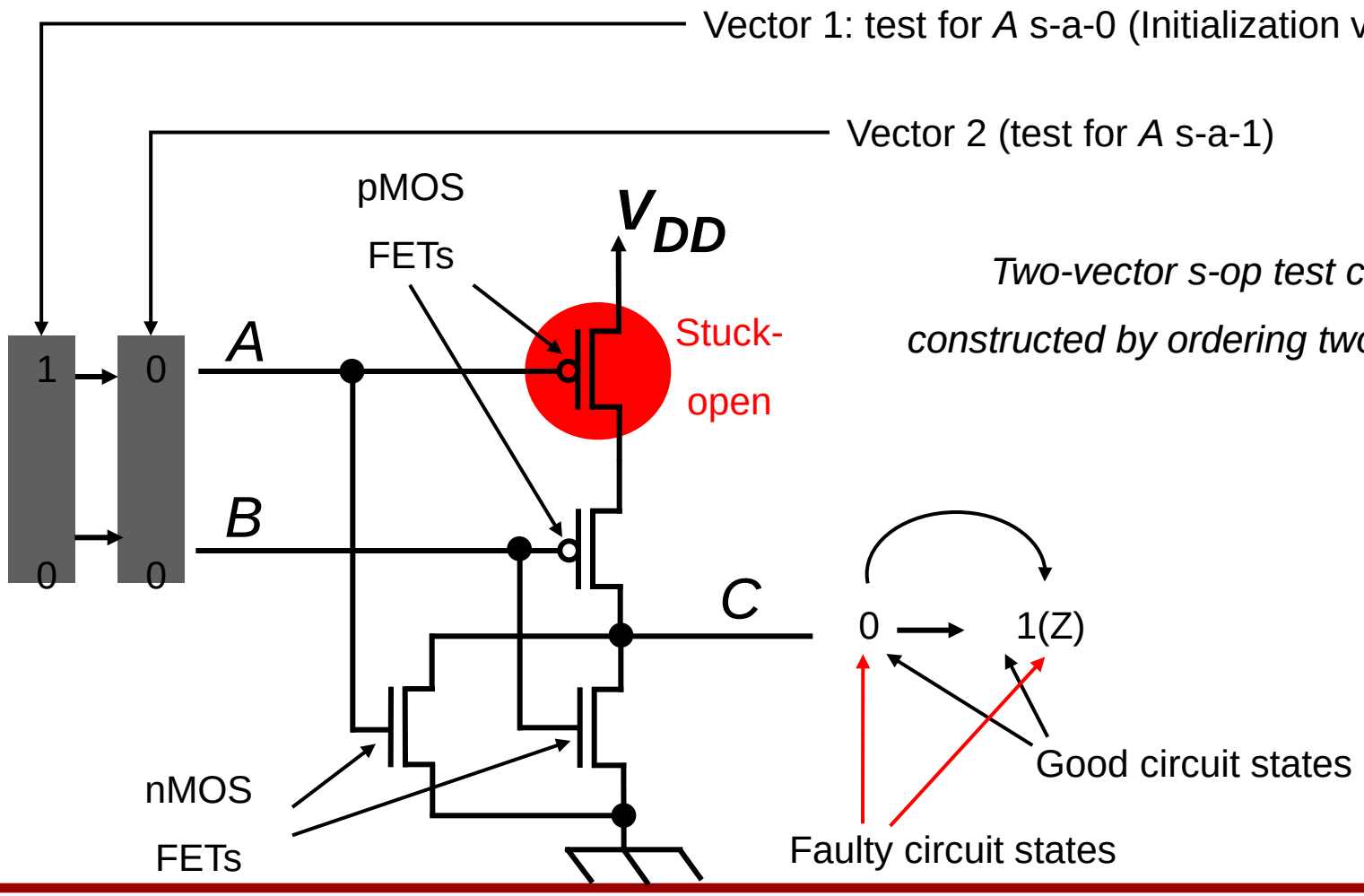
Transistor (Switch) Faults

- MOS transistor is considered an ideal switch and two types of faults are modeled:
  - Stuck-open: a single transistor is permanently stuck in the open state.
  - Stuck-short: a single transistor is permanently shorted irrespective of its gate voltage.

- Detection of a stuck-open fault requires two vectors.

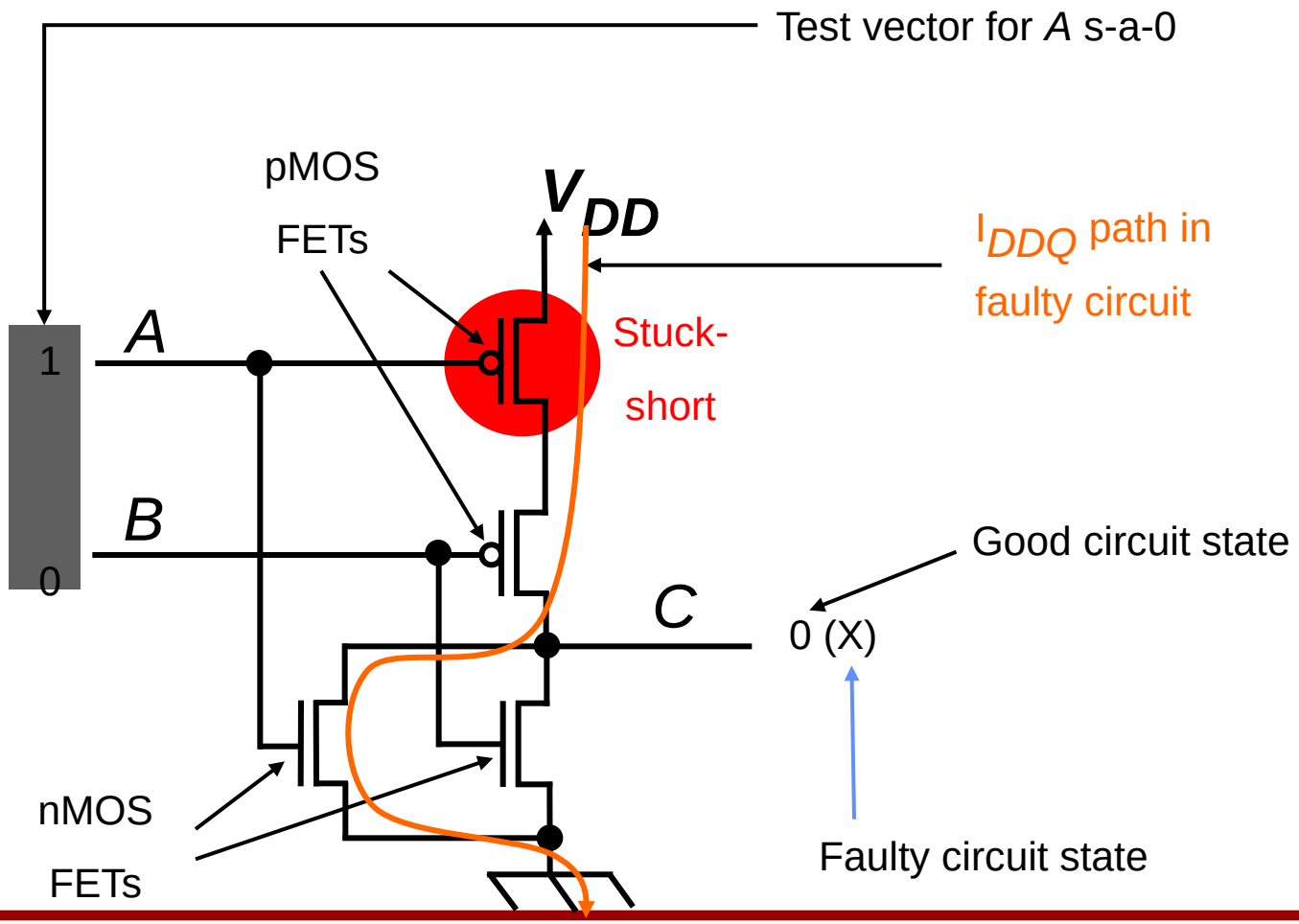
- Detection of a stuck-short fault requires the measurement of quiescent current (I_{DDQ}).

Stuck-Open Example

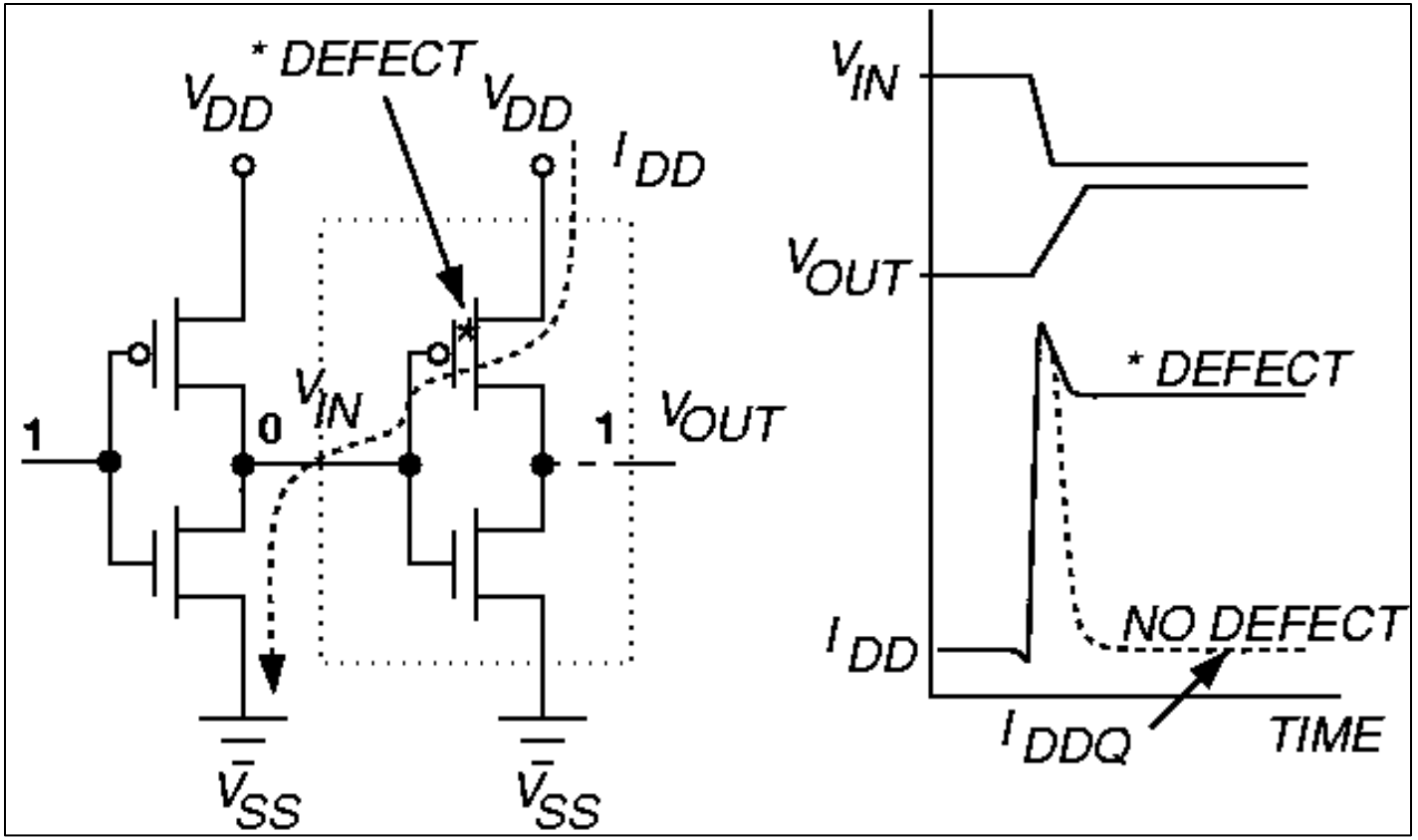


Two-vector s-op test can be constructed by ordering two s-at tests

Stuck-Short Example



Basic Principle of I_{DDQ} Testing



– Measure I_{DDQ} current through V_{SS} bus

Summary

- Fault models are analyzable approximations of defects and are essential for a test methodology.
- For digital logic single stuck-at fault model offers best advantage of tools and experience.
- Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests.
- Stuck-short and delay faults and technology-dependent faults require special tests.
- Memory and analog circuits need other specialized fault models and tests.