
EE434

ASIC & Digital Systems

Projected Schedule

Spring 2015
Dae Hyun Kim
daehyun@eecs.wsu.edu

| | | |
|--|--|--|
| (3/23) Project , Interconnect | (3/25) Interconnect | (3/27) Interconnect Lab1 (Layout) |
| (3/30) Interconnect HW6 (Interconnect) | (4/1) Timing Analysis | (4/3) Midterm 2 preview, Memory |
| (4/6) Timing Analysis HW7 (Interconnect) | (4/8) Midterm 2 | (4/10) Midterm 2 review Lab2 (P&R) |
| (4/13) Timing Analysis | (4/15) Timing Analysis | (4/17) Memory |
| (4/20) Arithmetic Circuits | (4/22) Arithmetic Circuits HW8 (Timing Analysis) | (4/24) Arithmetic Circuits Lab3 (FPGA) |
| (4/27) Arithmetic Circuits / Testing | (4/29) Testing HW9 (Arithmetic Circuits) | (5/1) Testing / FPGA / Final exam preview Project |
| (5/4) HW10 (Testing / Arithmetic Circuits) | (5/5) Final exam (1pm – 3pm) | |