# EE434
# ASIC & Digital Systems

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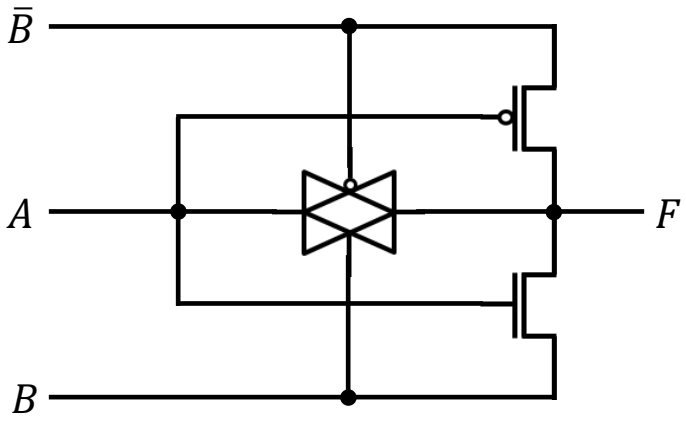
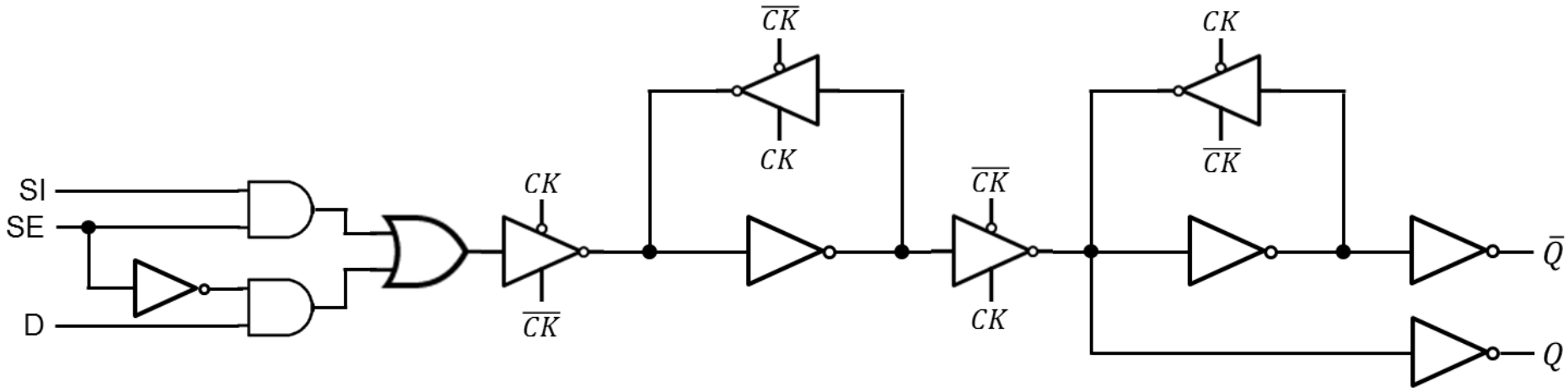
# Static CMOS Gates

- Represent F as a function of the inputs.



# Static CMOS Gates

- Describe the function of the following circuit in as much detail as possible.



# Transistor Sizing

- Optimal sizing
  - NAND2

# Problems

- Elmore Delay
- Dynamic CMOS
- DC Characteristics
- Pseudo-NMOS
- Switching Characteristics
- Transmission Gates
- Pass Transistor
- Static CMOS Gates
- Domino Logic

# Stat

| Problem | Avg. | Std. dev. |
|---|---|---|
| P1 (Schematic Analysis) | 5.00 | 4.48 |
| P2 (Schematic Analysis) | 6.40 | 3.30 |
| P3 (Schematic Analysis) | 6.35 | 4.22 |
| P4 (Transistor Sizing) | 8.60 | 2.76 |
| P5 (Optimal Transistor Sizing) | 1.15 | 2.37 |
| P6 (Elmore Delay) | 5.10 | 3.04 |
| P7 (Dynamic CMOS) | 4.20 | 3.56 |
| P8 (DC Characteristics) | 5.15 | 3.42 |
| Total | 41.95 | 15.46 |