Homework Assignment 1 (Due Feb. 4th at the beginning of the class)

(1) [Static CMOS Circuit, **5 points**] Draw a transistor-level schematic for the following function. Use six NMOS and six PMOS transistors.



 $F = \overline{A \cdot B + A \cdot C + B \cdot D}$

(2) [Static CMOS Circuit, **5 points**] Draw a transistor-level schematic for the above function. Use the smallest number of transistors.



(3) [Static CMOS Circuit, 5 points] An NMOS logic array for a function is shown below. Construct the PMOS circuit to complete the function.



(4) [Static CMOS Circuit, **5 points**] Draw a transistor-level schematic for the following function.



(5) [Logic Conversion, **5 points**] The two-input AND and OR gates use six transistors, but the two-input NAND and NOR gates use four transistors, so NAND and NOR gates are preferred to AND and OR gates in the design of CMOS circuits. Convert the following logic (F = A + B + C) into a new logic

using only INV, two-input NAND, and two-input NOR gates. Use the smallest number of transistors.



(6) [Static CMOS Circuit, **5 points**] Draw a transistor-level schematic for a two-input MUX ($F = \overline{S} \cdot A + S \cdot B$).







(7) [CMOS gates, 5 points] What is the intended function of the circuit shown in the figure below? What is the output swing?



Out = Vin. Swing = $[V_{tp}, V_{DD} - V_{tn}]$.

- (8) [HSPICE simulation, 10 points]
- 1. (Wn, Wp) = (90nm, 140nm): tf=70ps, tr=69ps
- 2. (Wn, Wp) = (180nm, 280nm): tf=34ps, tr=34ps
- 3. (Wn, Wp) = (90nm, 140nm), Cout=20fF: tf=137ps, tr=138ps
- 4. (Wn, Wp) = (90nm, 140nm), Cout=20fF, 50ps: tf=137ps, tr=136ps