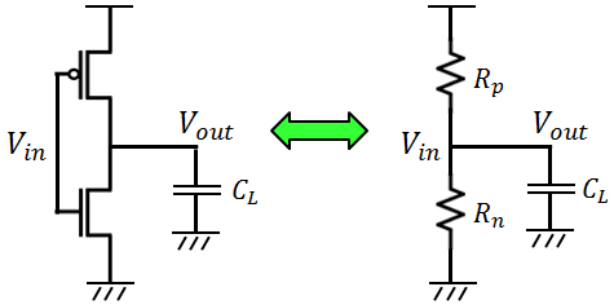
Homework Assignment 2

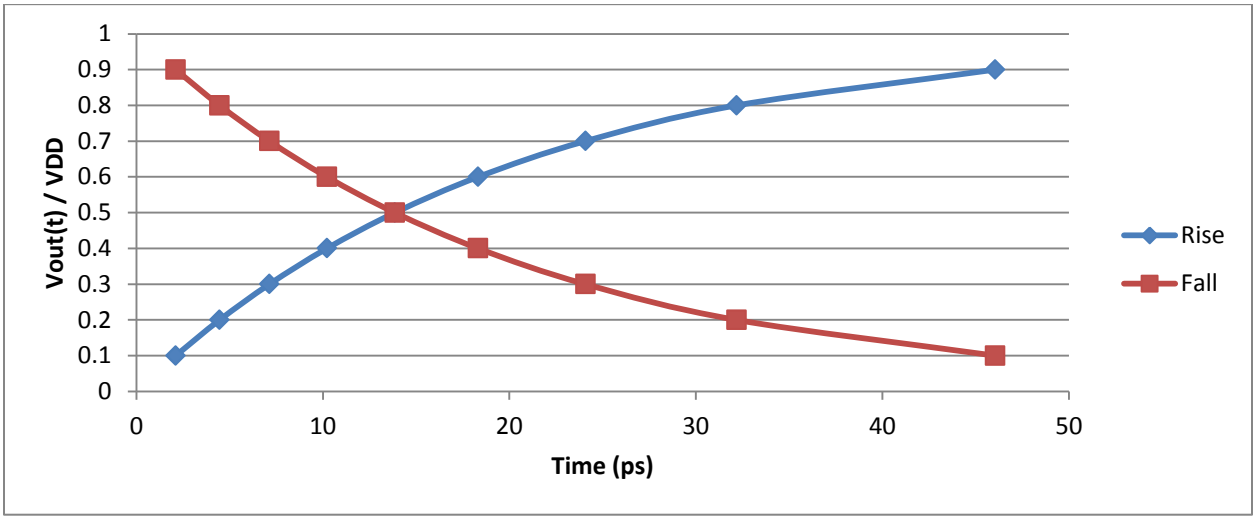
(Due Feb. 11th at the beginning of the class)

1. [Modeling, **10 points**] We can model an inverter by a simple RC circuit as follows. ($R_{OFF,p} = \infty, R_{OFF,n} = \infty, R_{ON,p} = 1k\Omega, R_{ON,n} = 1k\Omega, C_L = 20fF$) When $V_{in} = 0$ and V_{DD}, $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_{ON,p} \cdot C_L}}\right)$ and $V_{DD} \cdot e^{-\frac{t}{R_{ON,n} \cdot C_L}}$, respectively. Find t satisfying $V_{out}(t) = 0.1V_{DD}, 0.2V_{DD}, \dots, 0.9V_{DD}$ when $V_{in} = 0$. Find t satisfying $V_{out}(t) = 0.9V_{DD}, 0.8V_{DD}, \dots, 0.1V_{DD}$ when $V_{in} = V_{DD}$. Sketch $V_{out}(t)$ for $V_{in} = 0$ and V_{DD} by interpolating and extrapolating the points.



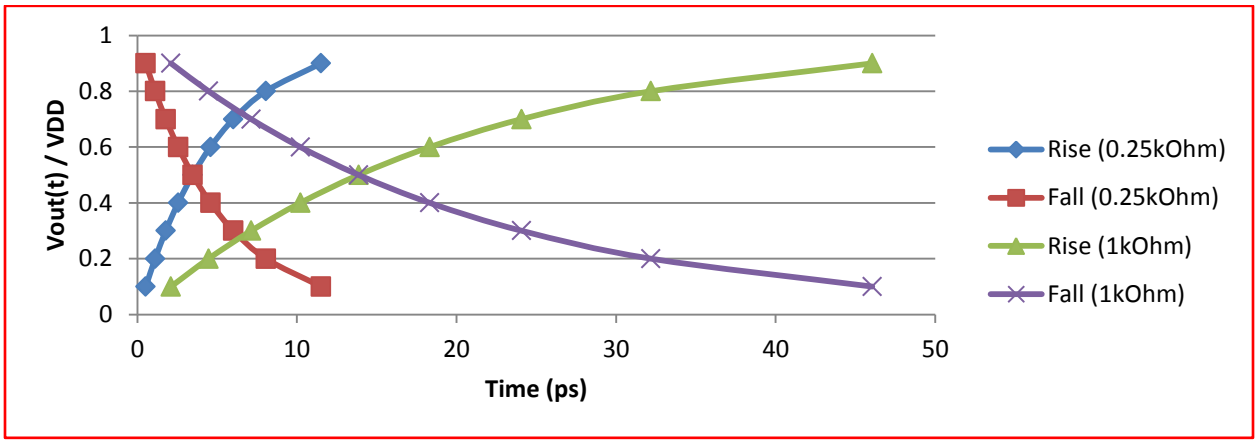
1) $V_{in} = 0$: for $V_{out}(t) = \alpha \cdot V_{DD}$ $(0 < \alpha < 1)$, $t = RC \cdot \ln(\frac{1}{1-\alpha})$.

2) $V_{in} = V_{DD}$: for $V_{out}(t) = \alpha \cdot V_{DD}$ $(0 < \alpha < 1)$, $t = RC \cdot \ln(\frac{1}{\alpha})$.

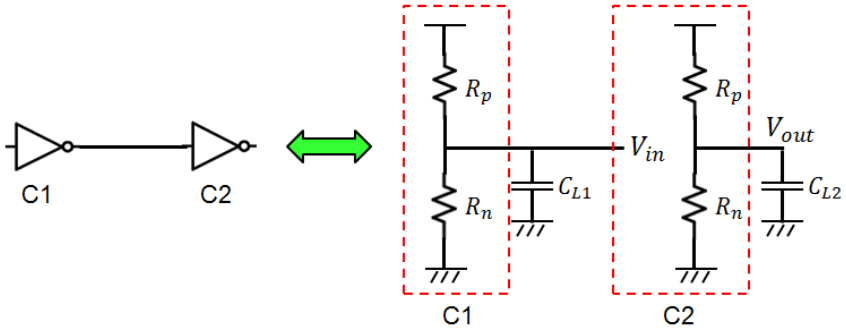


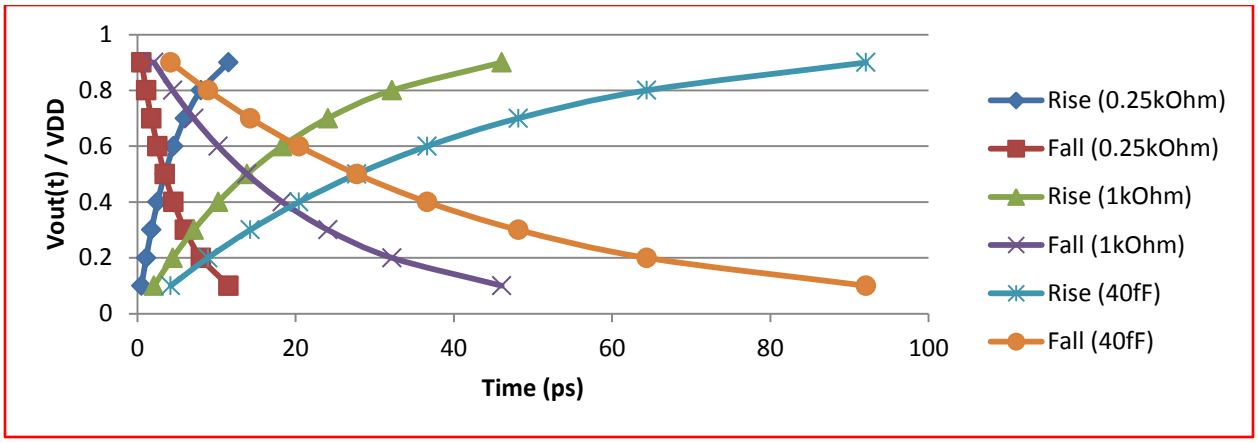
2. [Modeling, **10 points**] We upsize the NMOS and PMOS transistors in Problem 1 by 4x. Upsizing them increases the widths of the transistors, so their resistances go down. Now,

$R_{ON,p} = 0.25k\Omega, R_{ON,n} = 0.25k\Omega$. Repeat Problem 1 with these new resistances. Do you see the impact of upsizing?



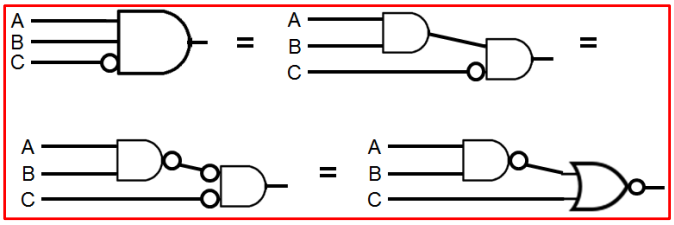
3. [Modeling, **10 points**] If you upsize a gate, the gate becomes faster (i.e., stronger). However, there are two side effects. First, it occupies more silicon area. Second, its input capacitance goes up, which has negative impact on the gate driving this gate. For example, in the following figure, upsizing C2 increases C_{L1}, so C1 needs more time to charge C_{L1}. This problem simulates the side effect of transistor sizing. Repeat Problem 1 using the following parameters. ($R_{OFF,p} = \infty, R_{OFF,n} = \infty, R_{ON,p} = 1k\Omega, R_{ON,n} = 1k\Omega, C_L = 40fF$)

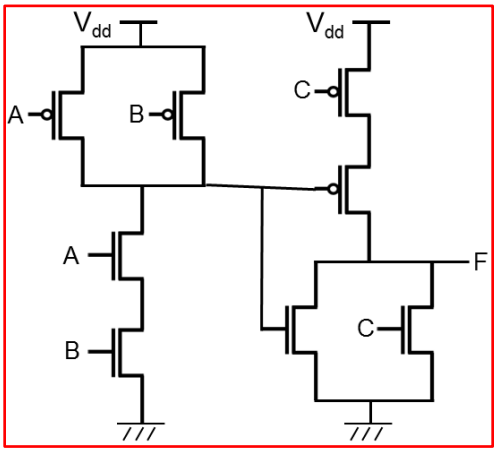




4. [Static CMOS Circuit, **5 points**] Draw a transistor-level schematic for the following function. (Primary inputs are A, B, and C). Simplify the logic before you draw the schematic so that you can use NAND2 and NOR2 gates.

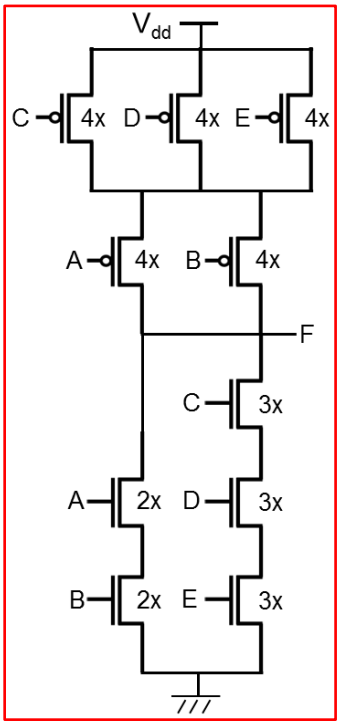
$$\boldsymbol{F = A \cdot B \cdot \overline{C}}$$





5. [Transistor Sizing, **5 points**] We are supposed to design the following function. $\mu_n = 2\mu_p$, C_L is the output load, and R_n is the resistance of a 1x NMOS. Design the gate and size the transistors so that both the NMOS and PMOS time constants become $R_n C_L$.

$$\boldsymbol{F = \overline{A \cdot B + C \cdot D \cdot E}}$$



6. [DC Analysis, **10 points**]
   1) $(W_n, W_p) = (90nm, 70nm)$: $V_{IL} = 335mV$, $V_{IH} = 540mV$, $V_{OL} = 45mV$, $V_{OH} = 950mV$, $\boldsymbol{NM_L = 290mV, NM_H = 410mV.}$
   2) $(W_n, W_p) = (45nm, 140nm)$: $V_{IL} = 410mV$, $V_{IH} = 620mV$, $V_{OL} = 45mV$, $V_{OH} = 950mV$, $\boldsymbol{NM_L = 365mV, NM_H = 330mV.}$
   3) $(W_n, W_p) = (90nm, 140nm)$: $V_{IL} = 370mV$, $V_{IH} = 575mV$, $V_{OL} = 50mV$, $V_{OH} = 950mV$, $\boldsymbol{NM_L = 320mV, NM_H = 375mV.}$

7. [Switching Characteristics, **10 points**]
   1) $(W_n, W_p) = (90nm, 140nm)$: $\boldsymbol{t_f = 101ps, t_r = 103ps.}$
   2) $(W_n, W_p) = (135nm, 210nm)$: $\boldsymbol{t_f = 67.2ps, t_r = 66.9ps.}$
   3) $(W_n, W_p) = (180nm, 280nm)$: $\boldsymbol{t_f = 50.7ps, t_r = 51.1ps.}$
   4) $(W_n, W_p) = (450nm, 700nm)$: $\boldsymbol{t_f = 21.8ps, t_r = 21.8ps.}$