Homework Assignment 3

(Due Feb. 23rd at the beginning of the class)

1. [Power Analysis, **10 points**]

C_L=10fF	Power (fall)	Power (rise)
1X	**5.15uW**	**5.20uW**
2X	**5.31uW**	**5.37uW**
4X	**5.47uW**	**5.58uW**
8X	**6.04uW**	**6.13uW**
16X	**6.62uW**	**6.53uW**

C_L=20fF	Power (fall)	Power (rise)
1X	**10.2uW**	**10.3uW**
2X	**10.3uW**	**10.4uW**
4X	**10.6uW**	**10.9uW**
8X	**11.0uW**	**11.0uW**
16X	**11.9uW**	**11.9uW**

2. [DC Analysis, **10 points**]
   - [**Submit**] V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H for the following three cases for the 1x two-input NAND gate with a 10fF load cap:
     - Case 1) V_A: 0→V_{DD} and V_B: V_{DD}.
       - **V_{IL}=410mV, V_{IH}=583mV, V_{OL}=65mV,V_{OH}=958mV, NM_L=345mV, NM_H=375mV.**
     - Case 2) V_A: V_{DD} and V_B: 0→V_{DD}.
       - **V_{IL}=390mV, V_{IH}=595mV, V_{OL}=56mV, V_{OH}=945mV, NM_L=334mV, NM_H=350mV.**
     - Case 3) V_A: 0→V_{DD} and V_B: 0→V_{DD}.
       - **V_{IL}=465mV, V_{IH}=644mV, V_{OL}=52mV, V_{OH}=966mV, NM_L=413mV, NM_H=322mV.**
   - [**Submit**] Create a netlist for a 1X two-input NOR gate with a 10fF load cap. Obtain V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H for the following three cases:

     - Case 1) V_A: 0→V_{DD} and V_B: 0→V_{DD}.
       - **V_{IL}=375mV, V_{IH}=526mV, V_{OL}=29mV, V_{OH}=955mV, NM_L=346mV, NM_H=429mV.**
     - Case 2) V_A: 0→V_{DD} and V_B: 0.
       - **V_{IL}=440mV, V_{IH}=595mV, V_{OL}=39mV, V_{OH}=946mV, NM_L=401mV, NM_H=351mV.**

- Case 3) V_A: 0 and V_B: 0→V_{DD}.
  - **V_{IL}=430mV, V_{IH}=642mV, V_{OL}=50mV, V_{OH}=955mV, NM_L=380mV, NM_H=313mV.**

3. [Elmore Delay, **10 points**]
   - [**Submit**] 10%-90% rise time of the RC tree in elmore_s.sp (at Vout) obtained by hspice simulation. 10%-90% rise time of the RC tree approximated by the Elmore delay model.
     - Spice = **497ps**
     - Elmore delay-based rise time = 2.2*(258.5ps) = **568.7ps**
   - [**Submit**] 10%-90% rise time of the RC tree in elmore_m.sp (at Vout1 and Vout2) obtained by hspice simulation. 10%-90% rise time of the RC tree approximated by the Elmore delay model.
     - Vout1
       - Spice = **896ps**
       - Elmore = 2.2*(429ps) = **943.8ps**
     - Vout2
       - Spice = **932ps**
       - Elmore = 2.2*(488.5ps) = **1074.7ps**
   - [**Submit**] In all the above simulations, we use 10ps for the rising transition time at the input. Now, open elmore_ex.sp and change the input rising transition time from 10ps to 100ps. Run hspice again and obtain 10%-90% rise time at Vout. Compare this with the rise time I obtained above (724ps). Is the delay dependent on the input transition time? Obtain 10%-90% rise time for the following input transition times (200ps, 300ps, 400ps, 500ps).

Slew	Rise time
10ps	**724ps**
100ps	**733ps**
200ps	**743ps**
300ps	**769ps**
400ps	**807ps**
500ps	**850ps**

4. [Transient Analysis of Transmission Gates, **10 points**]

	Fall time	Rise time
1X	**264ps**	**290ps**
2X	**173ps**	**191ps**
4X	**141ps**	**153ps**

5. [Analysis of Pass Transistors, **10 points**]
   - [**Submit**] Simulate pt_1.sp and obtain 10%-60% rise time. If you use the "measurement tool" in WaveView and set H(%) to 60.00, it will measure 10%-55% rise time, but this is acceptable. Submit the 10%-60% rise time.
     - **1.01ns**
   - [**Submit**] Obtain 10%-60% rise time for the following pass transistor sizes: 2X, 4X, 8X.

	Rise time
1X	**1.01ns**
2X	**588ps**
4X	**361ps**
8X	**245ps**

   - [**Submit**] Add one more pass transistor between the existing pass transistor and the output capacitor. Set the sizes of the two pass transistors (the existing one and the new one) to 1X. Obtain 10%-60% rise time. Upsize them to 2X, 4X, and 8X, and obtain 10%-60% rise time.

	Rise time
1X	**2.18ns**
2X	**1.28ns**
4X	**802ps**
8X	**527ps**

   - [**Submit**] Add two more pass transistors between the new pass transistor you added above and the output capacitor (so there are total four pass transistors between the output of the inverter and the output capacitor). Obtain 10%-60% rise time for 1X, 2X, 4X, and 8X pass transistor sizes.

	Rise time
1X	**3.33ns**
2X	**1.94ns**
4X	**1.21ns**
8X	**809ps**