Homework Assignment 5

(Due Mar. 13th at the beginning of the class)

0. Preparation
    - Download the following file into your working directory.
        - o wget http://www.eecs.wsu.edu/~ee434/Homework/hw05.tar.gz
    - Unzip it.
        - o tar xvzf hw05.tar.gz
    - Source synopsys.sh
        - o source synopsys.sh

1. [Synthesis and Analysis, **10 points**]
    - In this problem, we will synthesize and analyze a four-bit adder.
    - Open add4.v and see the source code.
    - Open add4.tcl and see the script.
    - Run design compiler.
        - o *design_vision –no_gui*
    - Run the following script.
        - o design_vision> *source add4.tcl*
    - It will compile the source code and synthesize a four-bit adder.
    - Let's analyze the circuit.
    - Run the following command to analyze area.
        - o design_vision> *report_area*

```
Number of ports:              14
Number of nets:               30
Number of cells:              21
Number of references:          5

Combinational area:       24.738000
Noncombinational area:     0.000000
Net Interconnect area:    undefined  (Wire load has zero net area)

Total cell area:          24.738000
Total area:               undefined
```

    - There are 14 ports (A:four bits, B: four bits, Cin, S: five bits, 4+4+1+5=14).
    - There are 30 nets. Open add4_mapped.v (netlist) and count the number of nets. There are 16 internal nets (wire n3, n4, …) and 14 input/output nets (primary input and output nets). 16+14=30.
    - There are 21 cells (= instances = standard cells). Open add4_mapped.v and count the number of instances.

- # references is # types of the standard cells used. Open add4_mapped.v and count the number of the types of the standard cells used. INV_X1, AOI22_X1, OR2_X1, XOR2_X1, OAI21_X1.
- The total area of the combinational cells is 24.738um^2.
- The total area of the non-combinational cells (FFs, latches, fill cells, etc.) is 0.
- Run the following command to analyze timing.
    - design_vision> *report_timing*

```
Startpoint: B[0] (input port)
Endpoint: S[4] (output port)
Path Group: (none)
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
myAdd4             5K_hvratio_1_1        NangateOpenCellLibrary

Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 f
B[0] (in)                                0.00       0.00 f
U19/ZN (OAI21_X1)                        0.04       0.04 r
U18/ZN (OAI21_X1)                        0.04       0.09 f
U15/ZN (OR2_X1)                          0.06       0.15 f
U14/ZN (AOI22_X1)                        0.05       0.21 r
U13/ZN (INV_X1)                          0.03       0.24 f
U10/ZN (OR2_X1)                          0.06       0.30 f
U9/ZN (AOI22_X1)                         0.05       0.35 r
U8/ZN (INV_X1)                           0.03       0.38 f
U5/ZN (OR2_X1)                           0.06       0.44 f
U4/ZN (AOI22_X1)                         0.05       0.50 r
U3/ZN (INV_X1)                           0.02       0.52 f
S[4] (out)                               0.00       0.52 f
data arrival time                                   0.52
-----------------------------------------------------------
(Path is unconstrained)
```

- It shows a worst path (there could be multiple worst paths).
- The start point of the worst path shown above is B[0].
- The end point of the worst path shown above is S[4] (this is actually the carry-out output port).
- The delay of the worst path is 0.52ns (520ps).
- The path is “unconstrained”, i.e., it doesn’t have any timing constraint.
- Run the following command to analyze power.
    - design_vision> *report_power*

```
Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =   9.3815 uW   (67%)
  Net Switching Power  =   4.7099 uW   (33%)
                         ---------
Total Dynamic Power    =  14.0914 uW  (100%)

Cell Leakage Power     = 580.0209 nW
```

- "Cell Internal Power" is the power consumed inside cells.
- "Net Switching Power" is the power consumed to drive nets.
- [**Submit**]
    - Create a netlist for a four-bit ripple-carry adder. Use only the following standard cell to implement it.

```
module myAdd4 ( A, B, Cin, S );
  input [3:0] A;
  input [3:0] B;
  output [4:0] S;
  input Cin;

  wire n1, n2, n3;

  FA_X1 U1 ( .A(A[0]), .B(B[0]), .CI(Cin), .CO(n1), .S(S[0]) );
  FA_X1 U2 ( .A(A[1]), .B(B[1]), .CI(n1),  .CO(n2), .S(S[1]) );
  FA_X1 U3 ( .A(A[2]), .B(B[2]), .CI(n2),  .CO(n3), .S(S[2]) );
  FA_X1 U4 ( .A(A[3]), .B(B[3]), .CI(n3),  .CO(S[4]), .S(S[3]) );
endmodule
```

```
set link_library {NangateOpenCellLibrary_typical_ecsm.db}
set target_library {NangateOpenCellLibrary_typical_ecsm.db}
read_file -format verilog {add4_fa.v}
```

    - Standard cell: FA_X1
        - Primary inputs: A, B, CI
        - Primary outputs: S, CO
    - Load the netlist into Design Compiler (modify add4.tcl. Do not run "compile –exact_map" and "write –format …").
    - Show area, timing, and power.

```
Number of ports:                14
Number of nets:                 17
Number of cells:                 4
Number of references:            1

Combinational area:         17.024000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:            17.024000
Total area:                 undefined
```

```
Startpoint: A[0] (input port)
Endpoint: S[3] (output port)
Path Group: (none)
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
myAdd4             5K_hvratio_1_1        NangateOpenCellLibrary

Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 f
A[0] (in)                                0.00       0.00 f
U1/CO (FA_X1)                            0.10       0.10 f
U2/CO (FA_X1)                            0.09       0.19 f
U3/CO (FA_X1)                            0.09       0.28 f
U4/S (FA_X1)                             0.13       0.41 r
S[3] (out)                               0.00       0.41 r
data arrival time                                   0.41
-----------------------------------------------------------
(Path is unconstrained)
```

```
  Cell Internal Power  =   6.6156 uW   (85%)
  Net Switching Power  =   1.1426 uW   (15%)
                         ---------
Total Dynamic Power    =   7.7581 uW  (100%)

Cell Leakage Power     = 303.0029 nW
```

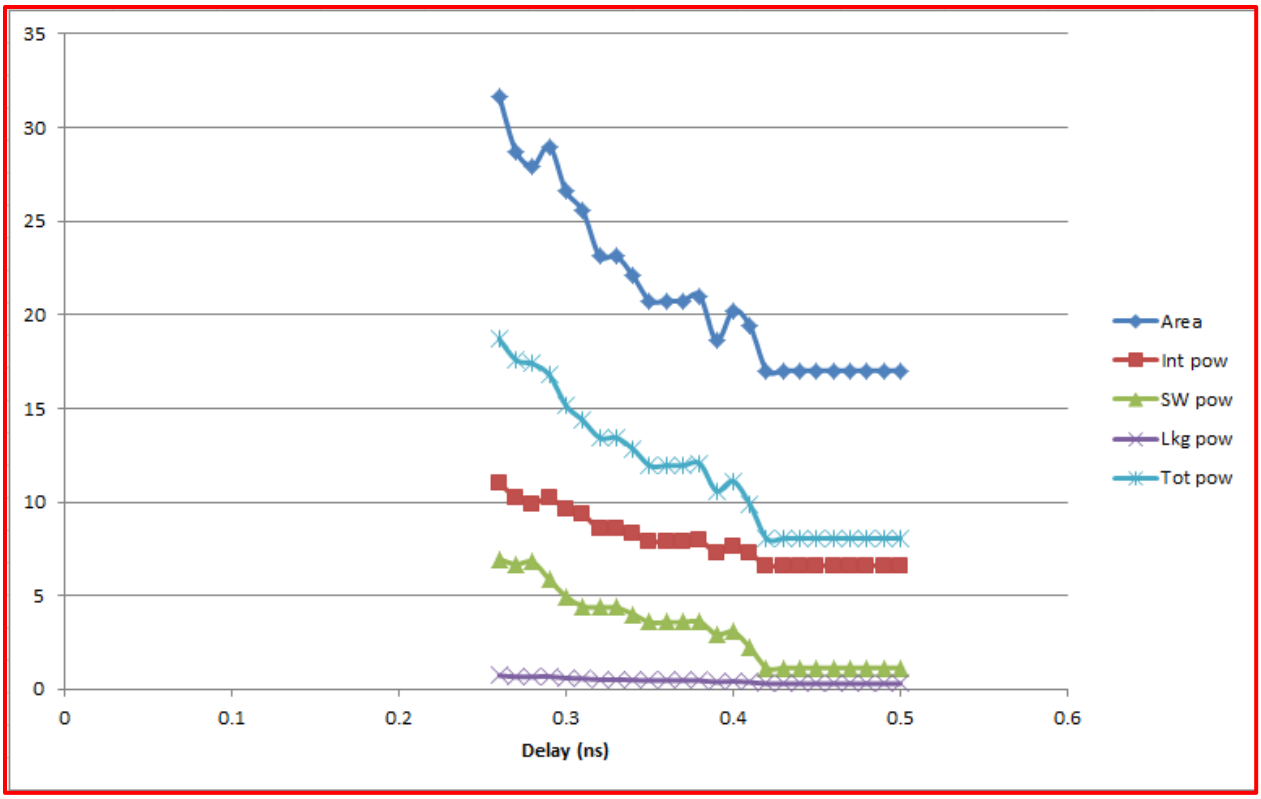
	Synthesis	Manual
Area	24.738 (um^2)	17.024 (um^2)
Timing	520 (ps)	410 (ps)
Power (Total) Internal Switching Leakage	14.0914 (uW) 9.3815 (uW) 4.7099 (uW) 0.580 (uW)	7.7581 (uW) 6.6156 (uW) 1.1426 (uW) 0.303 (uW)

2. [Optimization, **20 points**]
   - In this problem, we will optimize the HDL code and compare area, timing, and power.
   - Run Design Compiler and source “add4_read.tcl” to read in the HDL code.
   - Run the following command to synthesize and optimize the code.

- design_vision> *set_max_delay -from {A* B* Cin} -to {S*} 0.5*
- This sets a max. delay (0.5ns) from any input pin to any output pin.

- Compile.
  - design_vision> *compile*
- Get total area, a worst path delay (**data arrival time**), cell internal power, net switching power, cell leakage power, and total power (= internal power + switching power + leakage power).
- Change the max. delay constraint from 0.5ns to 0.49ns and re-compile it.
  - design_vision> *set_max_delay -from {A* B* Cin} -to {S*} 0.49*
  - design_vision> *compile*
- Get the area, delay, and power numbers again.
  - [**Submit**] Get {area, delay, internal power, switching power, leakage power, total power} for each max. delay constraint (d_{MAX}) and fill in the following table.

Max. delay (ns)	area (um2)	Delay (ps)	Int power	SW power	Lkg power	Total power (uW)
0.5	17.024	410	6.6156	1.1426	0.303	8.0612
0.49	17.024	410	6.6156	1.1426	0.303	8.0612
0.48	17.024	410	6.6156	1.1426	0.303	8.0612
0.47	17.024	410	6.6156	1.1426	0.303	8.0612
0.46	17.024	410	6.6156	1.1426	0.303	8.0612
0.45	17.024	410	6.6156	1.1426	0.303	8.0612
0.44	17.024	410	6.6156	1.1426	0.303	8.0612
0.43	17.024	410	6.6156	1.1426	0.303	8.0612
0.42	17.024	410	6.6156	1.1426	0.303	8.0612
0.41	19.418	400	7.2623	2.2362	0.384	9.8825
0.4	20.216	400	7.6165	3.0704	0.428	11.1149
0.39	18.62	350	7.276	2.9255	0.391	10.5925
0.38	21.014	370	7.9779	3.6106	0.472	12.0605
0.37	20.748	330	7.8944	3.5877	0.465	11.9471
0.36	20.748	330	7.8944	3.5877	0.465	11.9471
0.35	20.748	330	7.8944	3.5877	0.465	11.9471
0.34	22.078	320	8.3305	4.013	0.497	12.8405
0.33	23.142	310	8.5366	4.3697	0.524	13.4303
0.32	23.142	310	8.5366	4.3697	0.524	13.4303
0.31	25.536	310	9.3622	4.4324	0.571	14.3656
0.3	26.6	300	9.5944	4.9499	0.605	15.1493
0.29	28.994	250	10.2363	5.8564	0.687	16.7797
0.28	27.93	280	9.9084	6.7981	0.672	17.3785
0.27	28.728	280	10.2323	6.6849	0.669	17.5862
0.26	31.654	260	11.0175	6.9429	0.743	18.7034



3. [Design, Synthesis, and Optimization, **30 points**]
   - Write a Verilog code for a 32-bit adder.
     - Primary inputs: [31:0] A, [31:0] B, Cin
     - Primary outputs: [32:0] S
   - Synthesize and time it.
   - Use "set_max_delay –from {A* B* Cin} –to {S*} XX" to set up timing constraints.
   - Minimize the longest-path delay (but you should not violate the timing constraint).
   - [**Submit**] Area, worst-path delay, cell internal power (PI), net switching power (PS), cell leakage power (PL), and total power (PI+PS+PL).

```
Number of ports:                98
Number of nets:                 99
Number of cells:                 1
Number of references:            1

Combinational area:        303.771998
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           303.771998
Total area:                 undefined
```

```
Startpoint: A[5] (input port)
Endpoint: S[19] (output port)
Path Group: default
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
myAdd4             5K_hvratio_1_1        NangateOpenCellLibrary

Point                                                   Incr       Path
-----------------------------------------------------------------------
input external delay                                    0.00       0.00 r
A[5] (in)                                               0.00       0.00 r
add_1_root_add_6_2/A[5] (myAdd4_DW01_add_1)             0.00       0.00 r
add_1_root_add_6_2/U11/ZN (OR2_X2)                      0.04       0.04 r
add_1_root_add_6_2/U217/ZN (AND4_X1)                    0.07       0.11 r
add_1_root_add_6_2/U288/ZN (NAND2_X1)                   0.03       0.13 f
add_1_root_add_6_2/U287/ZN (NOR2_X1)                    0.04       0.17 r
add_1_root_add_6_2/U284/ZN (NOR2_X1)                    0.02       0.19 f
add_1_root_add_6_2/U303/ZN (OAI21_X1)                   0.03       0.23 r
add_1_root_add_6_2/U305/ZN (AOI21_X1)                   0.03       0.26 f
add_1_root_add_6_2/U310/ZN (OAI21_X1)                   0.05       0.30 r
add_1_root_add_6_2/U241/ZN (AND2_X1)                    0.05       0.36 r
add_1_root_add_6_2/U260/ZN (NOR2_X1)                    0.02       0.38 f
add_1_root_add_6_2/U249/ZN (OAI21_X1)                   0.04       0.42 r
add_1_root_add_6_2/U276/ZN (INV_X1)                     0.03       0.45 f
add_1_root_add_6_2/U289/ZN (OAI21_X1)                   0.05       0.50 r
add_1_root_add_6_2/U4/ZN (INV_X1)                       0.02       0.53 f
add_1_root_add_6_2/U290/ZN (OAI21_X1)                   0.04       0.57 r
add_1_root_add_6_2/U313/ZN (AOI21_X1)                   0.03       0.60 f
add_1_root_add_6_2/U312/ZN (XNOR2_X1)                   0.05       0.65 f
add_1_root_add_6_2/SUM[19] (myAdd4_DW01_add_1)          0.00       0.65 f
S[19] (out)                                             0.00       0.65 f
data arrival time                                                  0.65

max_delay                                               0.65       0.65
output external delay                                   0.00       0.65
data required time                                                 0.65
-----------------------------------------------------------------------
data required time                                                 0.65
data arrival time                                                 -0.65
-----------------------------------------------------------------------
slack (MET)                                                        0.00
```

```
  Cell Internal Power  =  99.0128 uW   (55%)
  Net Switching Power  =  81.7295 uW   (45%)
                         ---------
Total Dynamic Power    = 180.7424 uW  (100%)

Cell Leakage Power     =   7.7265 uW
```