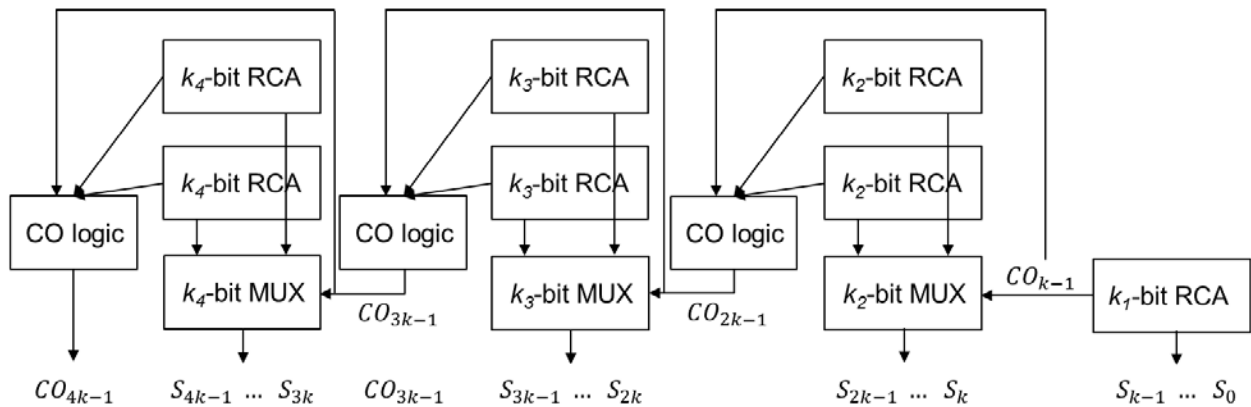


## Homework Assignment 9

(Due May 3<sup>rd</sup>, 12pm)

1. [Carry Select Adder, **40 points**] In the lecture note, we used k-bit adders to design an N-bit carry select adder. However, we can use variable-length adders instead of fixed-length adders. The following shows the specification of logic blocks we are going to use:

- N: 64
- Delay of a full adder:  $\Delta_{FA} = 100ps$
- Delay of a k-bit ripple carry adder (RCA):  $k \cdot \Delta_{FA}$
- Delay of a k-bit MUX (when  $k \geq 10$ ) and a CO logic:  $\varepsilon = 150ps$
- Architecture: We split N into four groups as follows:



Since N is 64, the above architecture should satisfy the following equation:

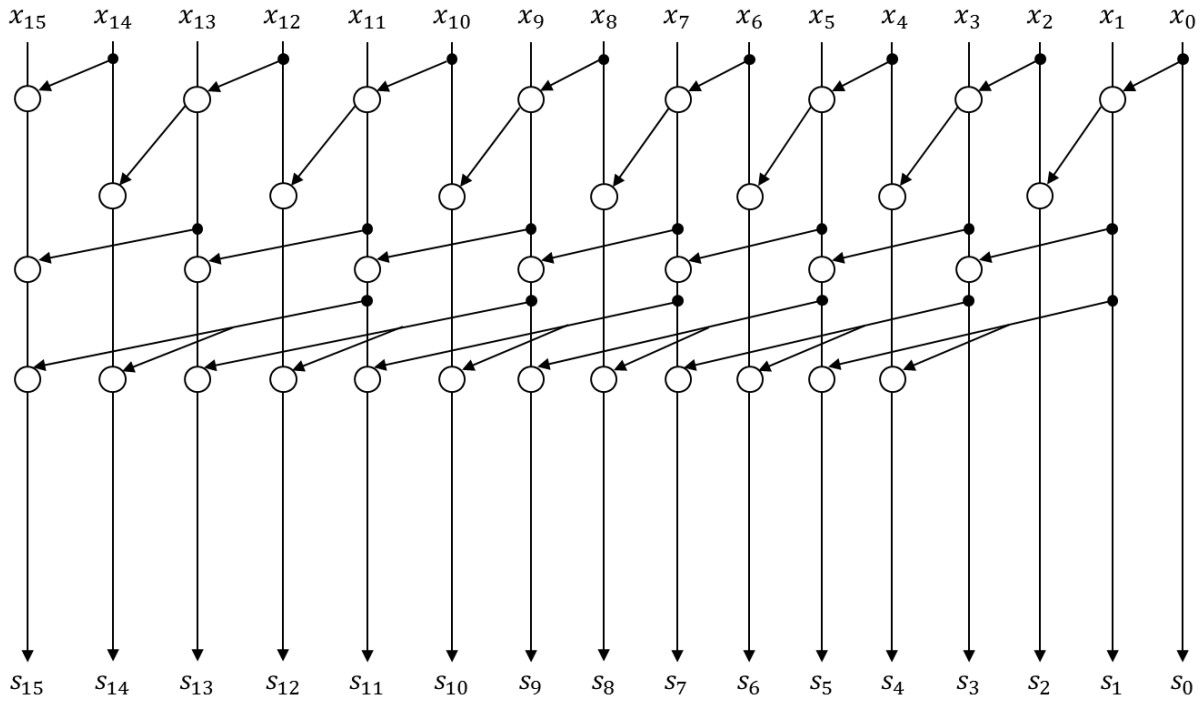
$$k_1 + k_2 + k_3 + k_4 = 64$$

We also assume that  $k_i \geq 10$  ( $i = 1 \sim 4$ ).

- 1) Represent delay of the 64-bit adder shown above as a function of  $k_1, k_2, k_3, k_4$ , and the MAX(a,b) function where “MAX(a, b) = a if (a>b) or b (if b>a)”.
- 2) Compute the total delay when  $k_1 = k_2 = k_3 = k_4$ .
- 3) Compute  $k_1, k_2, k_3$ , and  $k_4$  minimizing the delay and show the minimum delay. (Hint: (1) Use your intuition and some math. (2) If you want, you can program it to find  $k_1, k_2, k_3, k_4$ . In this case, you should show your program in your report).

2. [Prefix Adder, **40 points**] Complete the following prefix adders by inserting merging blocks and drawing arrows (try to minimize the number of merging blocks inserted).

1)



2)

