EE434 ASIC & Digital Systems

From Layout to SPICE Simulation (Virtuoso, Calibre, HSpice)

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Preparation for Lab1

- Download the following file into your working directory.
 wget http://eecs.wsu.edu/~ee434/Labs/lab1.tar.gz
- Unzip it.
 - tar xvfz lab1.tar.gz

Files

- Shortcuts
 - common_bindkeys.il
 - leBindKeys.il
 - schBindKeys.il
- sh
 - Files to source
- Tech file
 - tech_ng45nm.tf
- Display resource file
 - display.drf
- rules
 - layer.inc
 - calibreDRC.rul
 - calibreLVS.rul
 - calibrexRC.rul
- myInv_X1_LVS.sp: A netlist for LVS
- myInv_X1_simul.sp: A netlist to simulate an inverter with parasitic RC.
- myInv_X1_noRC_simul.sp: A netlist to simulate an inverter without parasitic RC.

What We Are Going To Do

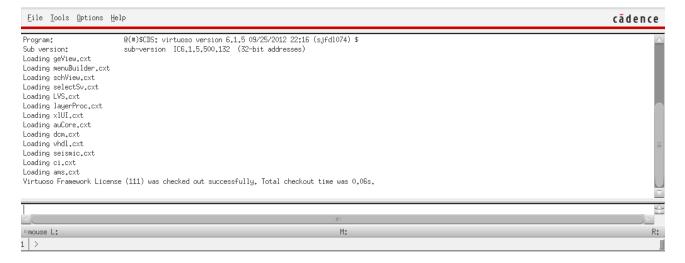
- 1. Layout
- 2. DRC
- 3. LVS
- 4. xRC
- 5. SPICE simulation

How to Launch Virtuoso

- Source the following file:
 > source sh/cadence-ic.sh
- Run Virtuoso

> virtuoso

• You will see a Cadence logo and a main window (Command Interpreter Window, CIW) as follows:



Create a Library

- In CIW
 - Click "Tools" \rightarrow "Technology File Manager...".
- In the Technology Tool Box window
 - Click "New...".
- In the New Technology Library window
 - Enter a library name you want.
 - Click "Browse..." to load tech_ng45nm.tf.
 - Click OK.
- You will see the following message.

Technology file '.'	' loaded successfully.

X New Technology Library Technology Library Name ng45nm_1		_ 🗆 ×
 Load ASCII Technology File Copy From Existing Technology Library Reference Existing Technology Libraries Directory (non-library directories) 	15_Spring/lab1/tech_ng45nm.tf US_3ths analogLib basic cdsDefTechLib ng45nm_1	Browse
sh		
Design Manager: No DM	OK Cancel	Apply Help

Create a Library

- Close the Technology Tool Box window.
- In CIW, click Tools \rightarrow Library Manager ...
- In the leftmost column, you will see both your library and some default libraries.

	Library
	ng45nm_1
	US_8ths ahdlLib analogLib basic cdsDefTechLib functional
I	ng45nm_1
	rfExamples rfLib

How to Create a Cell

- In the Library Manager window, click File \rightarrow New \rightarrow Cell View.
- Enter a cell name and click OK.

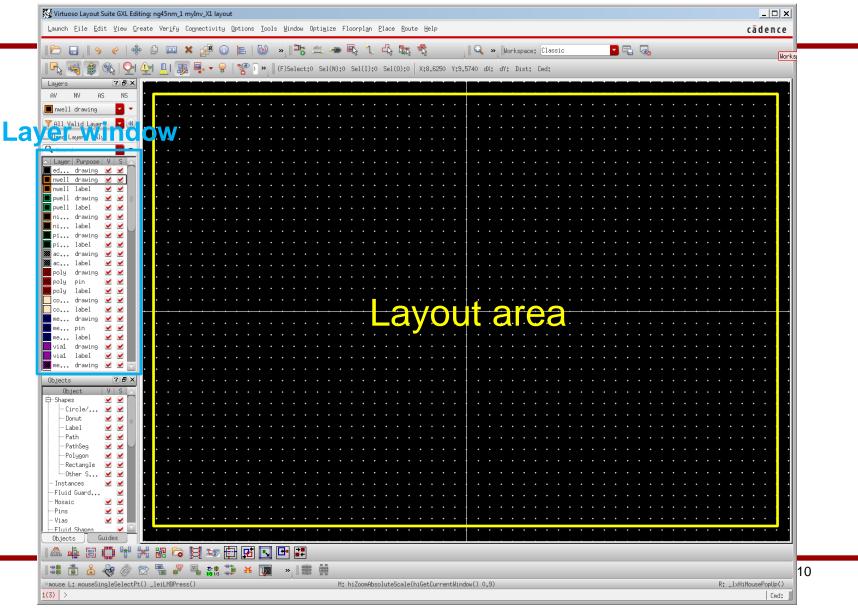
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File	
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	OK Cancel Help

How to Create a Cell

• If the following window pops up, uncheck the "Use schematic view:" and click OK.

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Library:		
Cell:		
View:		Browse
	OK	Cancel Help

Layout Window



Editor Setup

Press "e" or click "Options" → "Display…". Use the following setting.

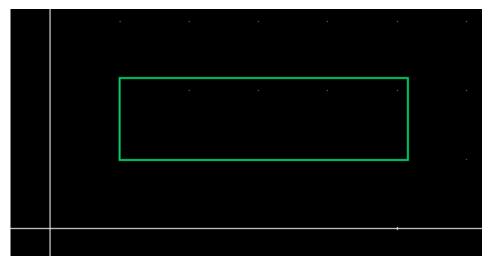
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□ Traversed instance BBox Maximum Drag Level 32 Maximum Number of Drag Figures 500 Scroll Percent 25 Instance Drawing Mode BBox ▼ Path Display Borders and Centerlines ▼ Set LPP VisibilitDo not check validity ▼ Show Name Of ○ instance ● master ○ both Array Display Display Levels ● Full Start 0 ● Border ● Source Stop 20	Snap Modes Create rthogonal C Edit rthogonal C Scope none C Automatic Dimming D Dim Intensity: 50 Jim Selected Object Content D True Color Selection only D
● Cellview ○ Library ○ Tech Library ○ File ~/. Save To Load From OK	cdsenv Browse Delete From Cancel Defaults Apply Help

Editor Setup

Press "Shift+e" or click "Options" → "Editor...". Use the following setting. (Turn off "Gravity On").

🗙 Layout Editor Options				
Layout Editor Options Editor Controls Repeat Commands Display Reference Point Auto Set Reference Point Recursion Check Maintain Connections Abut Server QCell Auto Abutment Save Rulers Select Created Object Rotate Around Combined Center Flip Around Combined Center Flip Around Combined Center Turn Off Infix In Smart Snapping Half Width Check off Conic Sides 20 Snapping Instance to Row Wires Manufacturing Grid	Gravity Controls Gravity On Types I all onone I centerline I edge I midpoint Vertex I end I nexus pin I origin Aperture O Depth 3 Bounce X 0 Bounce Y 0 Tap Auto Tap I wire Shape Tap Layer Tap Attributes Day Attributes Day attributes Even with different End Styles Even with different End Styles Include All (Wire) Via Layers	Wire Editing Wire Wire LEFRouting Via Parameters Calculation Mode Minimum Rules Auto Merge Wires Allow Loops Adjust Edited Vias Params Show Alignment Markers Blockage: Use Minimum Width Create Via Via Same as Wire Via Parameters Calculation Mode		
File ~/.cdsenv Save To	Tap Purpose List drawing	Browse Cancel Defaults Apply Help		

- Use the right mouse button to zoom in.
- Choose a layer you want to draw in the layer window.
 - Choose "drawing" for the "Purpose".
- Press "r" or Click "Create" → "Shape" → "Rectangle". Now you are ready to draw a rectangle of the layer you selected.
- Draw a rectangle by clicking the left mouse button twice.



- Press "ESC" to stop drawing rectangles.
- Click the rectangle you just drew.
- Press "q" to see the property of the rectangle.
- You can fine-control the coordinates in this window.
- Click "OK" to accept the change.

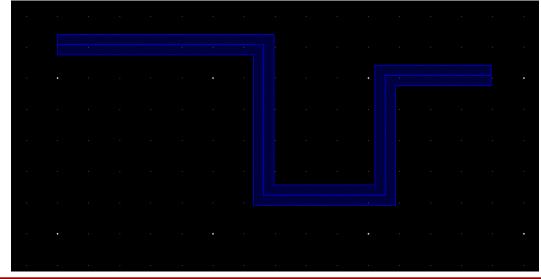
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- Press "f" to zoom out.
- Click whitespace to unselect the rectangle.

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- Drawing wires using rectangles is pretty painful.
- Click "metal 1 drawing" in the layer window.
- Press "p" or click "Create" \rightarrow "Shape" \rightarrow "Path".
- Now you are ready to draw a path of metal 1. Its width is predefined in the technology file.
- Try to draw some paths. To finish, double click the left button.

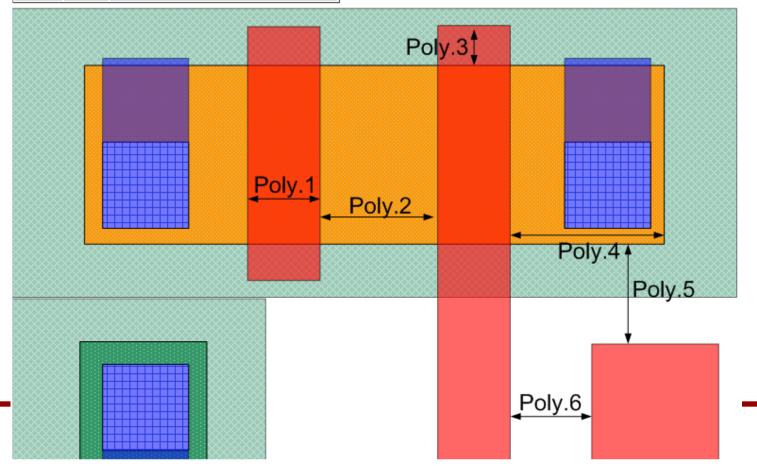


- Move: choose an object, press "m", and move it. Or, click whitespace to unselect, press "m", and click and move an object.
- Copy: Click whitespace to unselect, press "c", click the object you want to copy, and paste it.
- Stretch: click whitespace to unselect. Press "s" and stretch a boundary of an object.
- Ruler: press "k".
- Clear ruler: shift+k.
- Merge: select two objects of the same type crossing each other and press "shift+m". It will create a polygon object.
- Save: F2

- See the following page:
 - http://www.eda.ncsu.edu/wiki/FreePDK45:Contents
- Click each layer under "Design Rules".

FreePDK45:PolyRules

	Rule	Value	Description
	POLY.1	50 nm	Minimum width of poly
l	POLY.2	140 nm	Minimum spacing of poly AND active
	POLY.3	55 nm	Minimum poly extension beyond active
	POLY.4	70 nm	Minimum enclosure of active around gate
	POLY.5	50 nm	Minimum spacing of field poly to active
	POLY.6	75 nm	Minimum Minimum spacing of field poly



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FreePDK45:WellRules

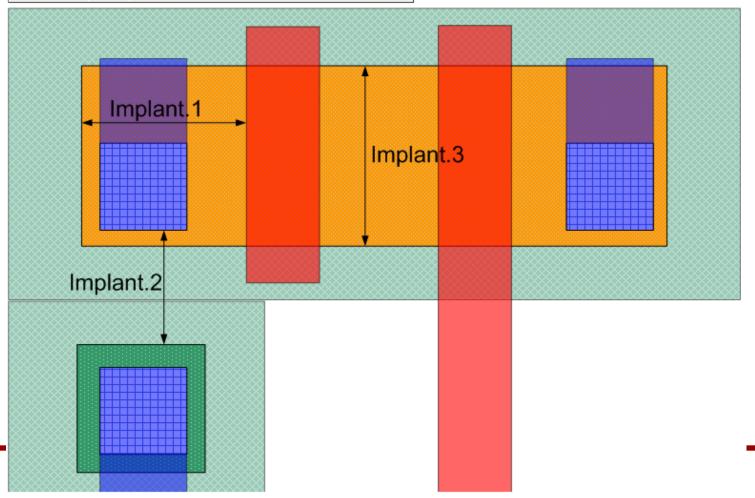
Well.1/

Well.2/ Well.3

Rule	Value	Description	
NELL.1	none	saveDerived: nwell/pwell must not overlap	
NELL.2	225 nm	Minimum spacing of nwell/pwell at different potential	
NELL.3	135 nm	Minimum spacing of nwell/pwell at the same potential	
NELL.4	200 nm	Minimum width of nwell/pwell	
Well	.4		

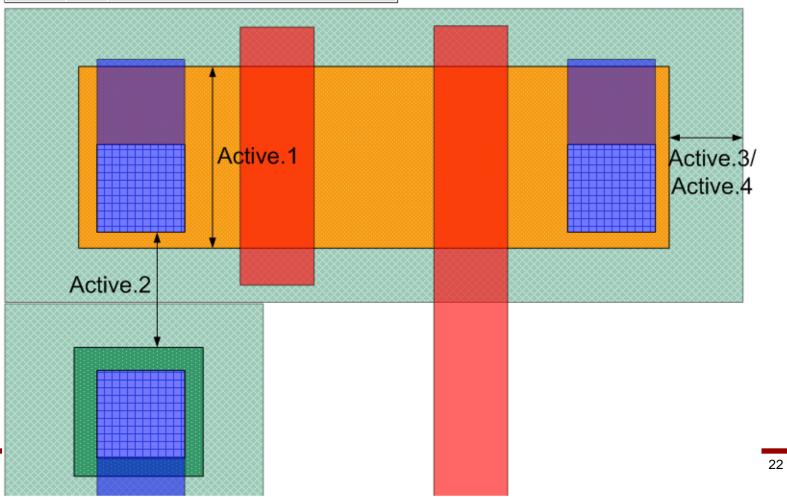
FreePDK45:ImplantRules

	Rule	Value	Description
	IMPLANT.1	70 nm	Minimum spacing of nimplant/ pimplant to channel
•	IMPLANT.2	25 nm	Minimum spacing of nimplant/ pimplant to contact
	IMPLANT.3/4	45 nm	Minimum width/ spacing of nimplant/ pimplant
	IMPLANT.5	none	Nimplant and pimplant must not overlap



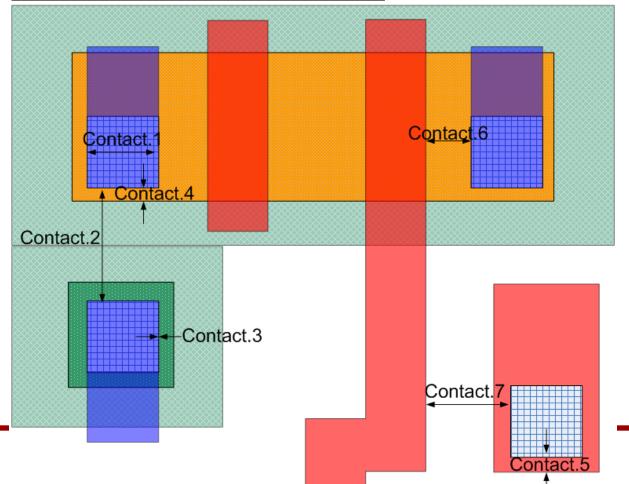
FreePDK45:ActiveRules

Rule	Value	Description	
ACTIVE.1	90 nm	Minimum width of active	
ACTIVE.2	80 nm	Minimum spacing of active	
ACTIVE.3	55 nm	Minimum enclosure/spacing of nwell/pwell to active	
ACTIVE.4	none	saveDerived: active must be inside nwell or pwell	



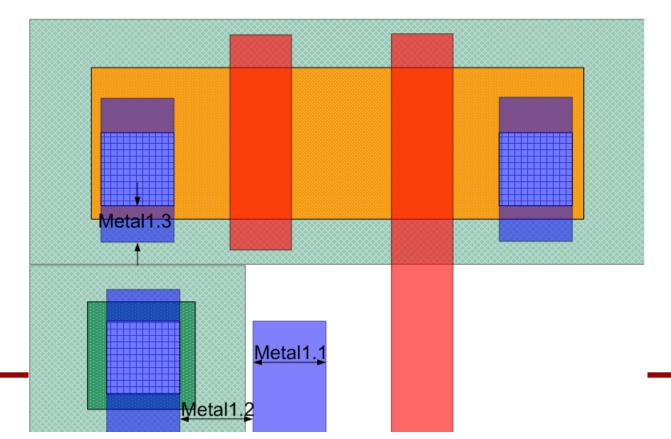
FreePDK45:ContactRules

Rule	Value	Description	
CONTACT.1	65 nm	Minimum width of contact	
CONTACT.2	75 nm	Minimum spacing of contact	
CONTACT.3	none	saveDerived: contact must be inside active or poly or metal	
CONTACT.4	5 nm	Minimum enclosure of active around contact	
CONTACT.5	5 nm	Minimum enclosure of poly around contact	
CONTACT.6	35 nm	Minimum spacing of contact and gate	
CONTACT.7	90 nm	Minimum spacing of contact and poly	



FreePDK45:Metal1Rules

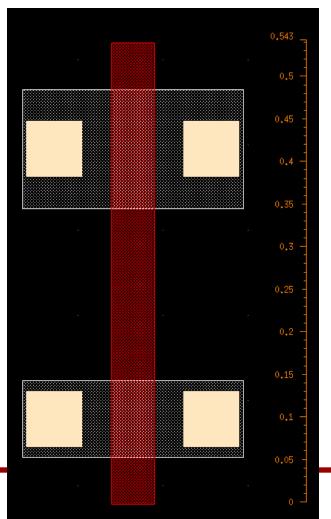
Rule	Value	Description		
METAL1.1	65 nm	Minimum width of metal1		
METAL1.2	65 nm	Minimum spacing of metal1		
METAL1.3 35 nm Minimum enclosure around contact on two opposite sides				
METAL1.4	35 nm	Minimum enclosure around via1 on two opposite sides		
METAL1.5	90 nm	Minimum spacing of metal wider than 90 nm and longer than 900 nm		
METAL1.6	270 nm	Minimum spacing of metal wider than 270 nm and longer than 300 nm		
METAL1.7	L1.7 500 nm Minimum spacing of metal wider than 500 nm and longer than 1.			
METAL1.8 900 nm Minimum spacing of metal wider than 900 nm and longer tha		Minimum spacing of metal wider than 900 nm and longer than 2.7 um		
METAL1.9	1500 nm	Minimum spacing of metal wider than 1500 nm and longer than 4.0 um		



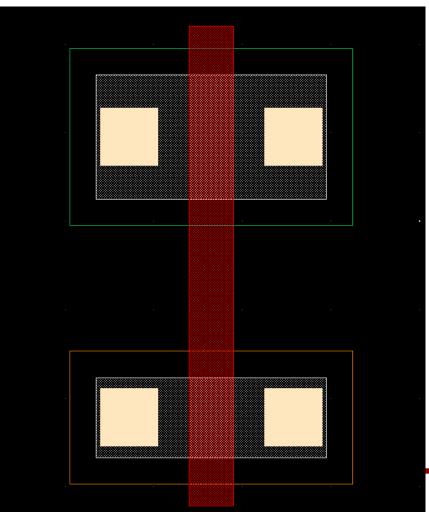
FreePDK45:Via1Rules

Rule	Value	Description		
VIA1.1	65 nm	Minimum width of via1		
VIA1.2	75 nm	Minimum spacing of via1		
VIA1.3	none	saveDerived: via1 must be inside metal1		
VIA1.4	none	saveDerived: via1 must be inside metal2		

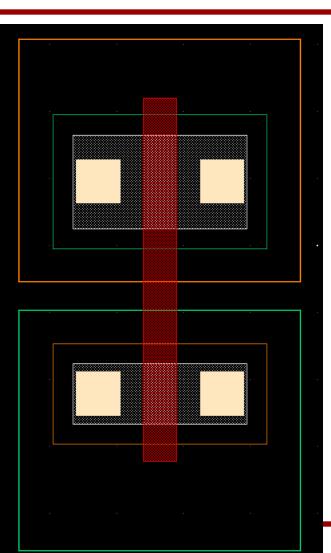
1. poly, active, and contact (Ln=50nm, Wn=90nm, Lp=50nm, Wp=140nm).



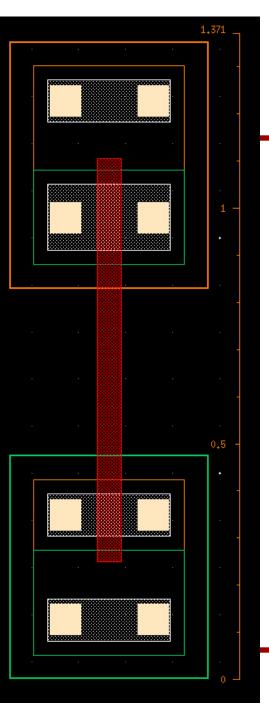
2. pimplant and nimplant.



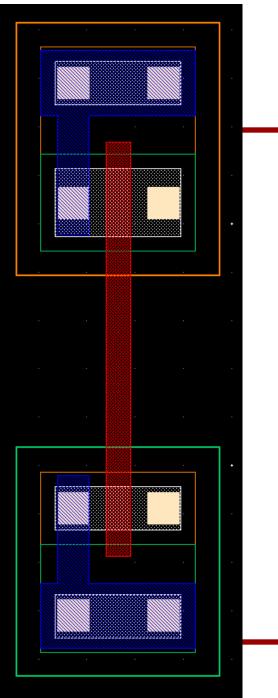
3. pwell and nwell



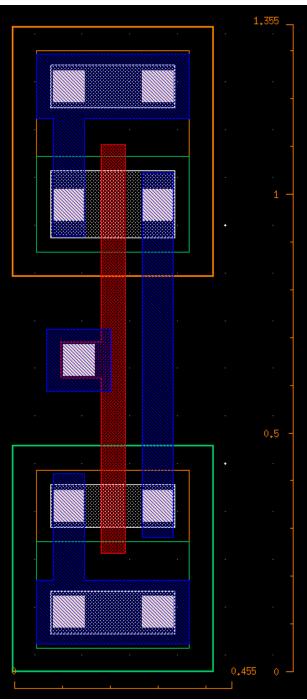
4. body contacts.



5. VDD and VSS.



6. Input and output.

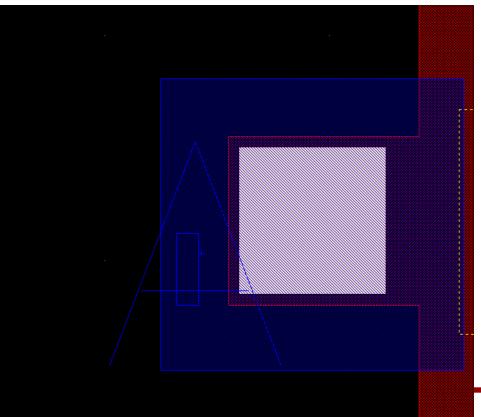


- 7. Create pins (A, ZN, VDD, VSS).
 - "Create" \rightarrow "Pin..."

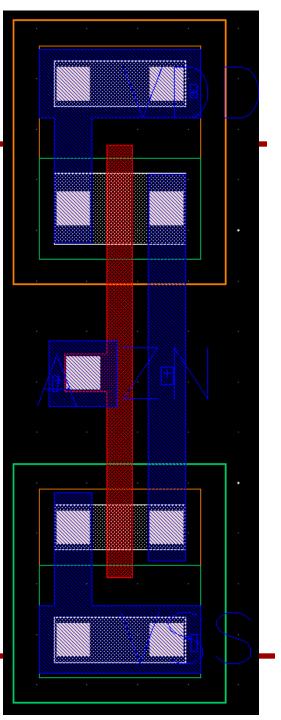
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Snap Mode	orthogonal 🔽			
Access Direction	🗹 Top 🗹 Bottom 🗹 Left 🗹 Right			
	🗹 Any 📃 None			
	Hide Cancel Help			

- 7. Create pins (A, ZN, VDD, VSS).
 - Then, create a small rectangle inside the target pin.
 - Make sure that the + mark of the pin is placed inside the wire

object.



- 7. Create pins (A, ZN, VDD, VSS).
 - A: input
 - ZN: output
 - VDD, VSS: inputOutput



- 8. Save the design.
- 9. Export the design into gdsii.
 - In CIW, click "File" \rightarrow "Export" \rightarrow "Stream...".
 - Click "Translate".

🗙 Virtuoso (R) XStream	Out	<u> </u>
Stream File Technology	myInv_X1.gds	•••
Library Library Top Level Cell(s)	ng45nm_1 myInv_X1	•••
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10. Export



1. Let's run DRC.

- 2. Source calibre.sh.> source sh/calibre.sh
- 3. Run Calibre.
 - > calibre -gui

Calibre Interactive v2013.2_18.13						<u>- 🗆 x</u>
nmDRC	DFM	nmLVS	PERC	PEX	3DSTACK	RVE

- 4. Click "nmDRC".
- 5. Close the "Load Runset File" window.
- 6. The red texts mean that some files in the input tabs are missing.

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7. Click "Rules", and "..." in the "DRC Rules File" and choose "rules/calibreDRC.rul".

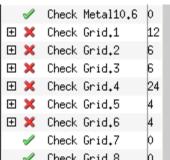
8. Click "Inputs" and "..." in the "File" and choose the gdsii file you exported.

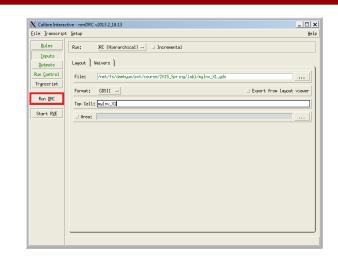
9. Enter the name of your inverter cell.

Calibre Interactive - nmDRC v2013.2_18.13		Calibre Interactive - nmDRC v2013.2_18.13	_ 🗆 🗙
Eile Iranscript Setup	Help	Eile Iranscript Setup	Help
Rules File	/calibreDRC.rul	Elle Innescript Setup Bules Run: RE (Hierarchical) Incremental Inputs Lagout Waivers Run Control File: /labi/mginu_Xi.gd Transcript Format: GUSII Run DRC Top Cell: mginu_XI	

10. Click "Run DRC" to run Calibre DRC.

- 11. It will show two windows.
 - DRC Summary Report
 - Calibre RVE
- 12. Close the Summary Report window.
- 13. See the RVE window. I have the following errors.



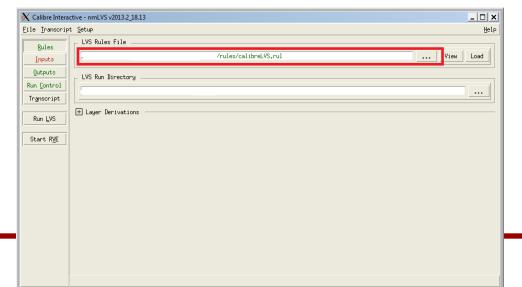


14. Ignore the "Check Grid.#" errors.

15. If you have any errors, fix them in the layout window (Virtuoso), re-export, and run DRC again.

1. Let's run LVS.

- 2. Click "nmLVS" in the main Calibre window.
- 3. Close the "Load Runset File" window.
- 4. Select the "calibreLVS.rul" in the LVS rule file section.



5. Click "Inputs". We need to enter the name of the file containing the layout and the netlist file.

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Rules	Run: Hierarchical \bigcirc Flat \bigcirc Calibre CB	
Inputs	Step: • Layout vs Netlis 🗢 Netlist vs Netl: 🗢 Netlist Extract:	
Qutputs Run <u>C</u> ontrol	Lagout Netlist H-Cells Signatures Waivers)
Tr <u>a</u> nscript	File: /myInv_X1.gds	
Run <u>L</u> VS	Format: GDSII -	□ Export from layout viewer
Start R <u>V</u> E	Top Cell: pyInv_X1	
	Layout Netlis <mark>lay.net</mark>	View
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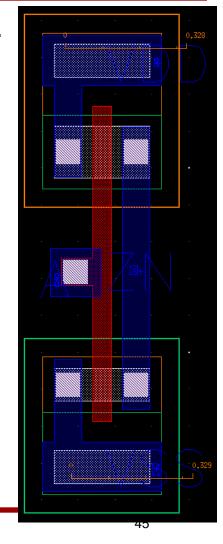
6. If everything is good, you will see the following window:

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😃 Comparison Results							∇
Reports	Cell myInv_X1 Summary	(Clean)					
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🚧 Finder	"						
■Schematics Setup							
©Options	LAYOUT CELL NAME: SOURCE CELL NAME:	myInv_X1 myInv_X1					
	INITIAL NUMBERS OF OBJECTS						
	Layout	Source	Component Type				
	Ports: 4	4					
	Nets: 4	4					
	Instances: 1		MN (4 pins) MP (4 pins)				
	1		MP (4 pins)				
	Total Inst: 2	2					
	NUMBERS OF OBJECTS AFT	FR TRANSFORMAT	TON				
	Layout	Source	Component Type				
	Ports: 4	4					
	Nets: 4	4					
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7. I'll remove the body contacts and see what happens.

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-+ Navigator	😕 Comparison Results 🗙					
→ Navigator Image: Comparison Results → Extraction Results → Extraction Report Image: Report Image: Report Image: Rules Image: Rules Image: Rules Image: Rules <t< th=""><th>Layout Cell / Type Xinginu_Xi =: Xincorrect Nets Xincorrect Nets Xincorrect Instances Xincorrect Xincorrect Xinco</th><th>ESULTS (TOP LEVEL)</th><th>Count 4 4 2 2 2</th><th>Nets SL, 4S (+2)</th><th>Instances 1L, 1S</th><th> Ports 4L, 4S</th></t<>	Layout Cell / Type Xinginu_Xi =: Xincorrect Nets Xincorrect Nets Xincorrect Instances Xincorrect Xincorrect Xinco	ESULTS (TOP LEVEL)	Count 4 4 2 2 2	Nets SL, 4S (+2)	Instances 1L, 1S	Ports 4L, 4S



8. First of all, match "Ports", which are primary inputs and outputs.



10. Then, match "Nets".

Nets: 6 4 *

- In the source (the SPICE netlist), there are four nets, which makes sense (A, ZN, VDD, VSS).

- In the layout, however, there are six nets, so something is wrong in the layout.

11. Click "Discrepancy #".

Incorrect Instances Incorrect Instances Discrepancy #3 Inscrepancy #4	2
Cell myInv_X1 (Incorrect Instances #3) LAYOUT NAME X Discrepancy #3 in myInv_X1	SOURCE NAME
M1(0.240,0.973) MP(PMOS_HP) 9: A s: ZN d: VDD b: 6 ** VDD **	mp1 MP(PMOS_HP) 9: A s: ZN d: VDD ** no similar net ** b: VDD

- It says that the body (substrate) of M1 (the PMOS transistor) in the layout is connected to net "6", but that in the source is connected to "VDD".

- From this, we know that the body of M1 is NOT connected VDD.

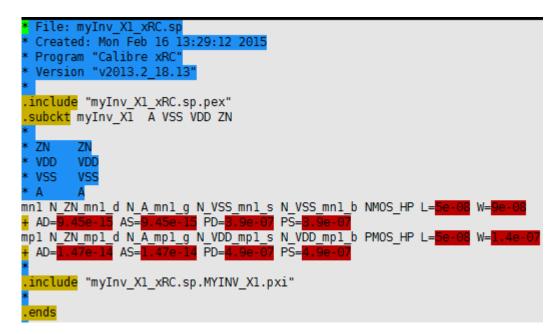
- 1. Let's run xRC.
- 2. Click "PEX" in the Calibre main window.

Rules	PEX Rules File			
Inputs		/rules/calibrexRC.rul	Vi	iew
Qutputs	PEX Run Directory			
	.ayout Netlist) H-C	ells Blocks Probes		
<u>I</u> nputs Outputs	File:	/myInv_X1.gds		
Run <u>C</u> ontrol	Format: GDSII -		□ Export from layout	viewer
Tr <u>a</u> nscript	Top Cell: myInv_X1			
Rules	Layout Netlist	H-Cells] Blocks] Probes]		
<u>I</u> nputs <u>O</u> utputs	Files: myInv_X	L_LVS.sp	*].
Run <u>C</u> ontrol	Format: SPICE	-	□ Export from schema	tic
Tr <u>a</u> nscript	Top Cell: myInv_X1			

<u>R</u> ules	Extraction Mode xRC Accuracy 200
<u>I</u> nputs	
Qutputs	Extraction Type Transistor Level R + C + CC No Inductance
Run <u>C</u> ontrol	Netlist Nets Reports SVDB
Tr <u>a</u> nscript	
	Format: HSPICE Use Names From: SCHEMATIC
Run <u>P</u> EX	
	File: myInv_X1_xRC.sp
Start R <u>V</u> E	
	View netlist after PEX finishes

3. Click "Run PEX".

4. xRC netlist (myInv_X1_xRC.sp)



Example – Inverter SPICE Simulation

- 1. Let's run HSPICE for the inverter.
 - > hspice myInv_X1_simul.sp
 - > hspice myInv_X1_noRC_simul.sp
- 2. The following shows my result:

	Fall	Rise
Without RC	112.67ps	123.11ps
With parasitic RC	119.29ps	132.62ps
Difference	+6.62ps	+9.51ps