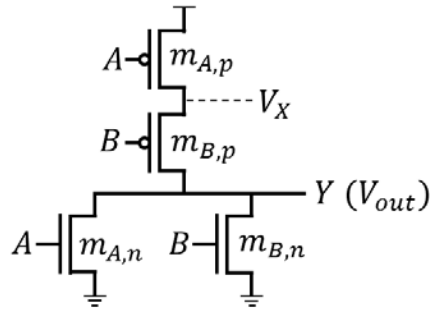


Homework Assignment 1

(Due Oct. 2nd at the beginning of the class)

(1) [NOR2, 40 points] The following shows a TR-level two-input NOR gate design.

Assume that L and W of each transistor are L_{min} and W_{min} , respectively.



- a) At time 0^- (right before time 0), both A and B are 0 (so the output Y is 1 and V_X is also 1). At time 0, A switches to 1 (and B stays at 0). Draw a plot for V_{out} vs. time t . Describe how the operation mode (cutoff, linear, saturation) of each transistor varies for $m_{A,n}$, $m_{B,n}$, $m_{A,p}$, and $m_{B,p}$.
- b) At time 0^- (right before time 0), both A and B are 0 (so the output Y is 1 and V_X is also 1). At time 0, B switches to 1 (and A stays at 0). Draw a plot for V_{out} vs. time t . Describe how the operation mode (cutoff, linear, saturation) of each transistor varies for $m_{A,n}$, $m_{B,n}$, $m_{A,p}$, and $m_{B,p}$.
- c) At time 0^- (right before time 0), both A and B are 0 (so the output Y is 1 and V_X is also 1). At time 0, both A and B switch to 1. Draw a plot for V_{out} vs. time t . Describe how the operation mode (cutoff, linear, saturation) of each transistor varies for $m_{A,n}$, $m_{B,n}$, $m_{A,p}$, and $m_{B,p}$.
- d) At time 0^- (right before time 0), both A and B are 1 (so the output Y is 0). Assume V_X is also 0. At time 0, A and B switch to 0. Draw a plot for V_{out} vs. time t . Describe how the operation mode (cutoff, linear, saturation) of each transistor varies for $m_{A,n}$, $m_{B,n}$, $m_{A,p}$, and $m_{B,p}$.

(2) [SPICE simulation, 20 points] Create a three-input NAND gate input file for SPICE simulation. The following shows the specifications you should use for this simulation.

- **Input transition time:** A, B, and C are 0 at time 0, stay at 0 until time 1ns, then start going up and reach 1 at time 1.01ns (so the transition time is 10ps).
- **Load capacitance:** 10fF
- **PFETs' width:** 70nm
- **NFETs' width:** minimum is 50nm, step size is 10nm (i.e., the width of an NFET should be $(50+10*k)$ nm where k is an integer greater than or equal to zero).
- **Measure delay:** Add the following command to your HSPICE input file so that it can automatically measure the fall delay (Nout is the name of the output node. You will need to substitute the name of your output node into Nout.)
 - **.measure tran fdly TRIG V(Nout) VAL=0.9 FALL=1 TARG V(Nout) VAL=0.1 FALL=1**
- **Problem 1)** The three NFETs should have the same width. Find the minimum width that makes the fall delay less than 100ps. (Submit only the minimum width.)
- **Problem 2)** Set the load capacitance to 50fF. The three NFETs still have the same width. Find the minimum width that makes the fall delay less than 100ps. (Submit only the minimum width.)