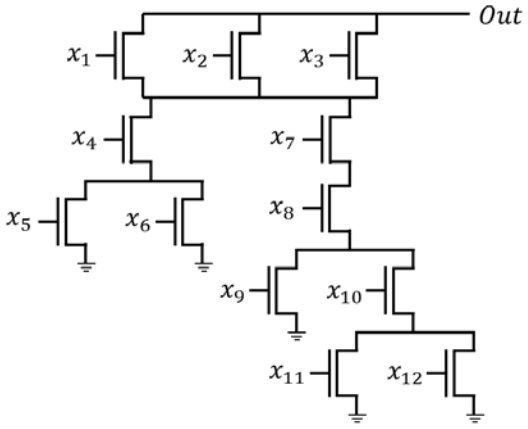
Homework Assignment 2
(Due Oct. 16th at the beginning of the class)

(1) **[Static CMOS, 10 points]** Draw a transistor-level schematic for the following Boolean function.

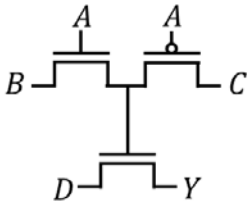
$$\boldsymbol{Y = \overline{A + B + C \cdot (D \cdot E + F \cdot (G + H))}}$$

(2) **[DC analysis, 10 points]** Draw a DC curve (Vin vs. Vout) for a buffer ($Y = A$). A buffer consists of two inverters connected in series.

(3) **[Transistor sizing, 10 points]** The following shows a schematic of an NFET network of a gate. Size the transistors. The target timing constraint is $\tau = \frac{R_n}{10}$ where R_n is the resistance of a 1X NFET.



(4) **[Schematic analysis, 10 points]** Derive output Y as a Boolean function of inputs A, B, C, and D. Use Z for high impedance.



(5) **[Power analysis, 10 points]** The following schematic shows a two-input NOR gate. It is known that input A switches between 0 and 1 very often and input B

stays at 1 most of the time. C_X and R_X show a small parasitic capacitance and a leaky path to the ground, respectively. Which one (between (a) and (b)) do you prefer to save power consumption? Why?