# *EE586*
# *VLSI Design*

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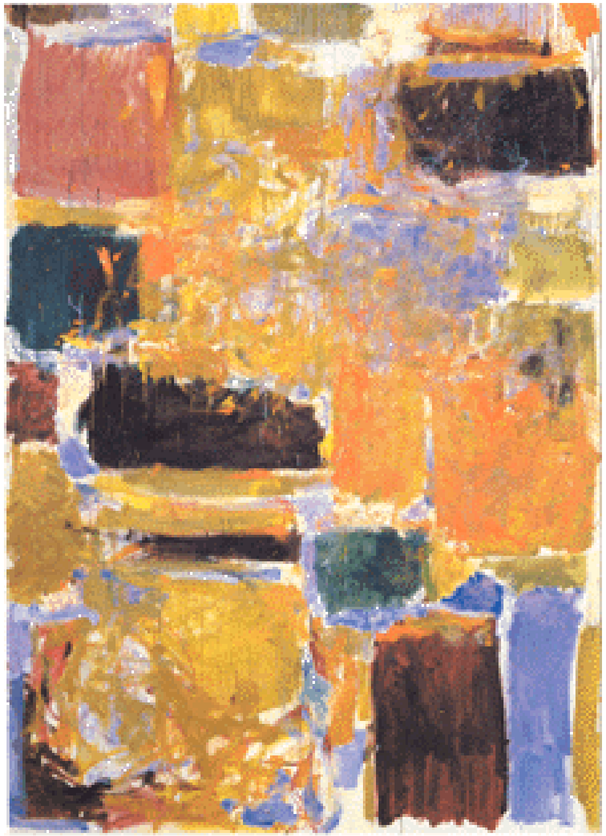
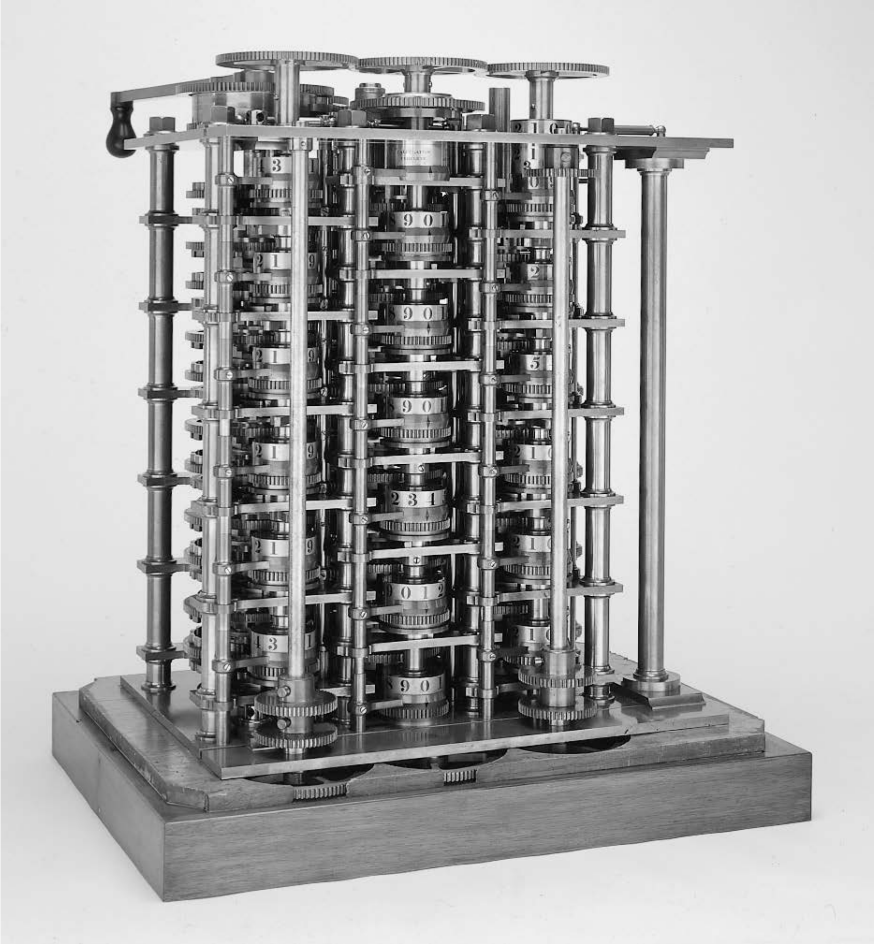
# *Lecture 1 (Introduction)*

- Why is designing digital ICs different today than it was before?
- Will it change in future?



# The First Computer

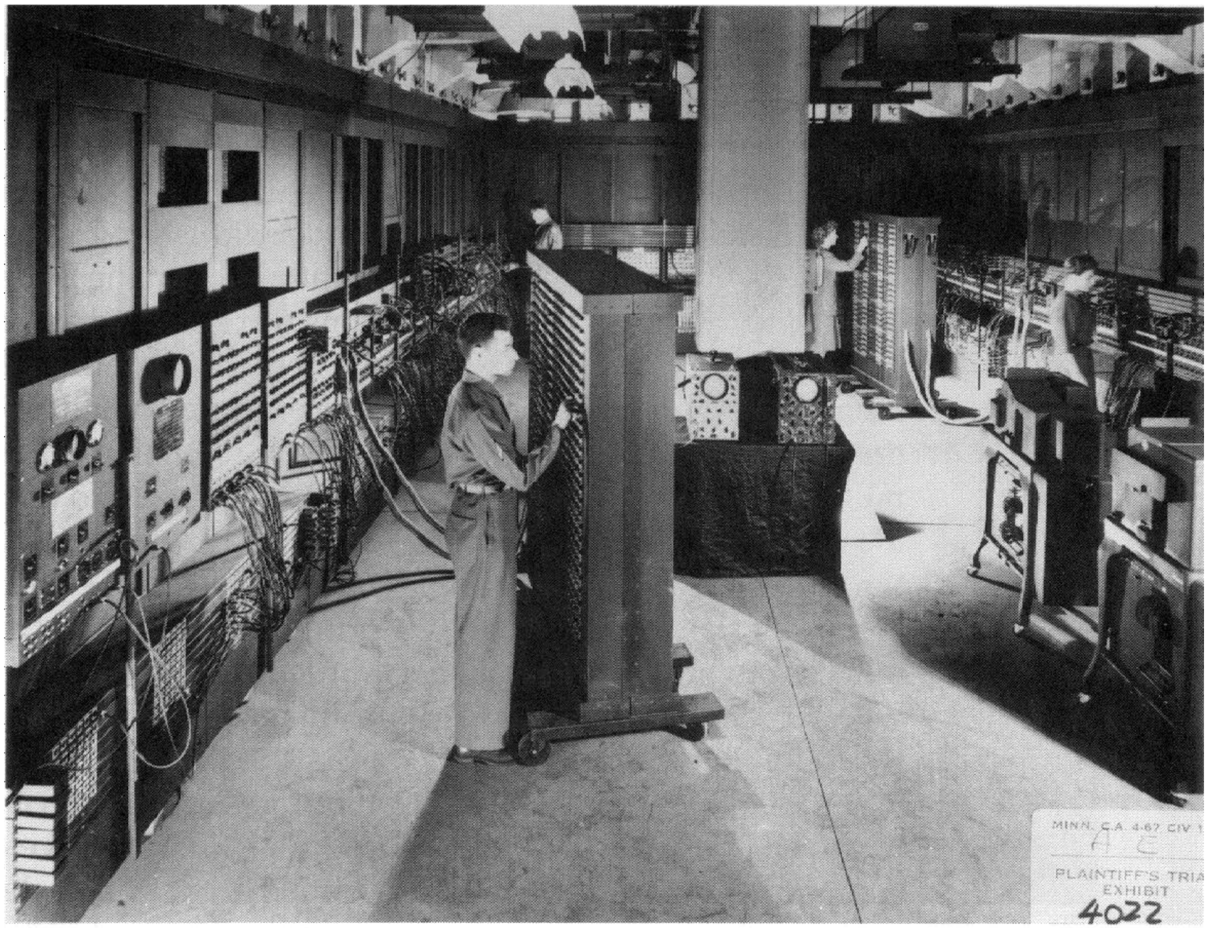


**The Babbage Difference Engine (1832)**

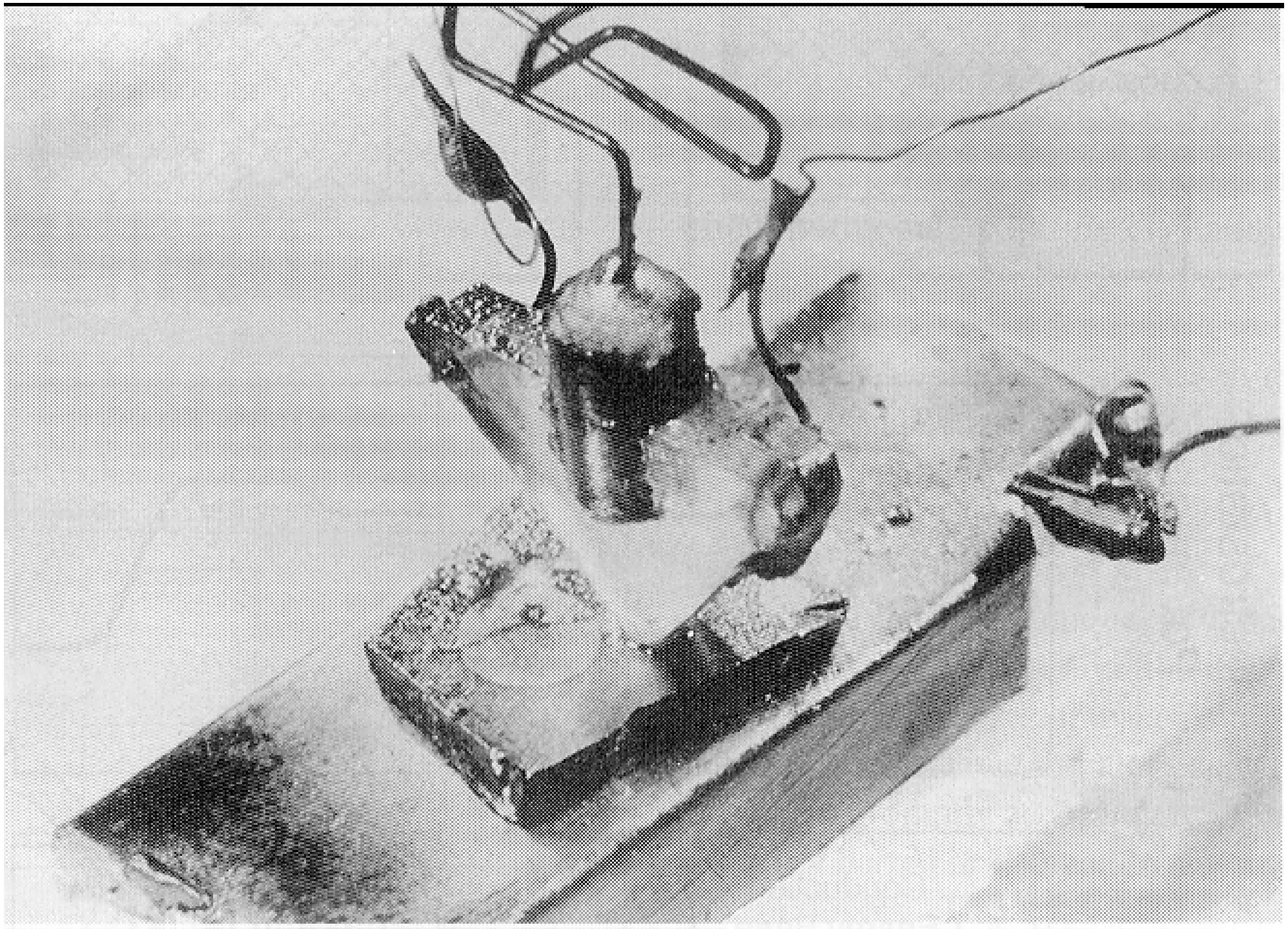
**25,000 parts**

**cost:** £17,470

# ENIAC - The first electronic computer (1946)

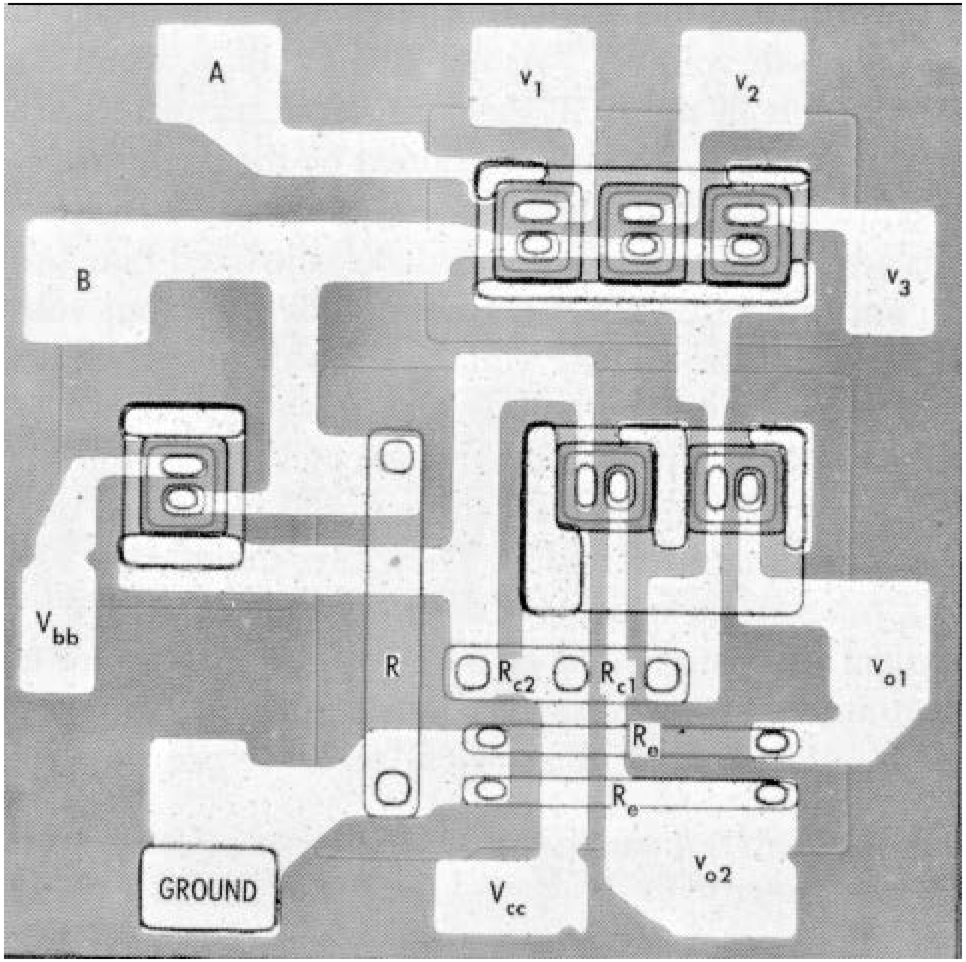


# The Transistor Revolution



First transistor
Bell Labs, 1948

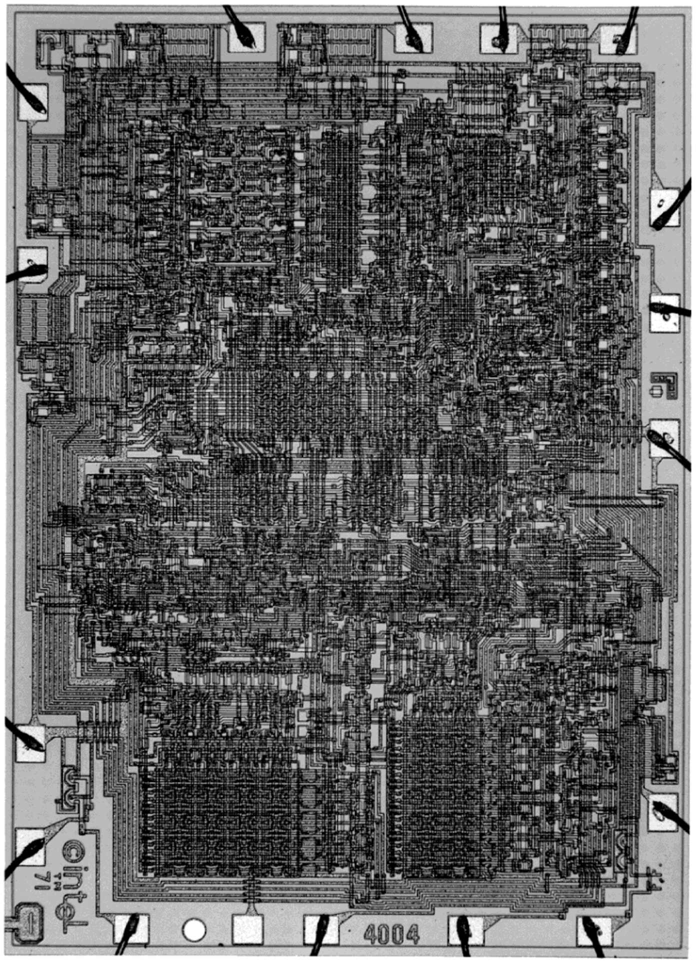
# The First Integrated Circuits




*Bipolar logic*
*1960's*

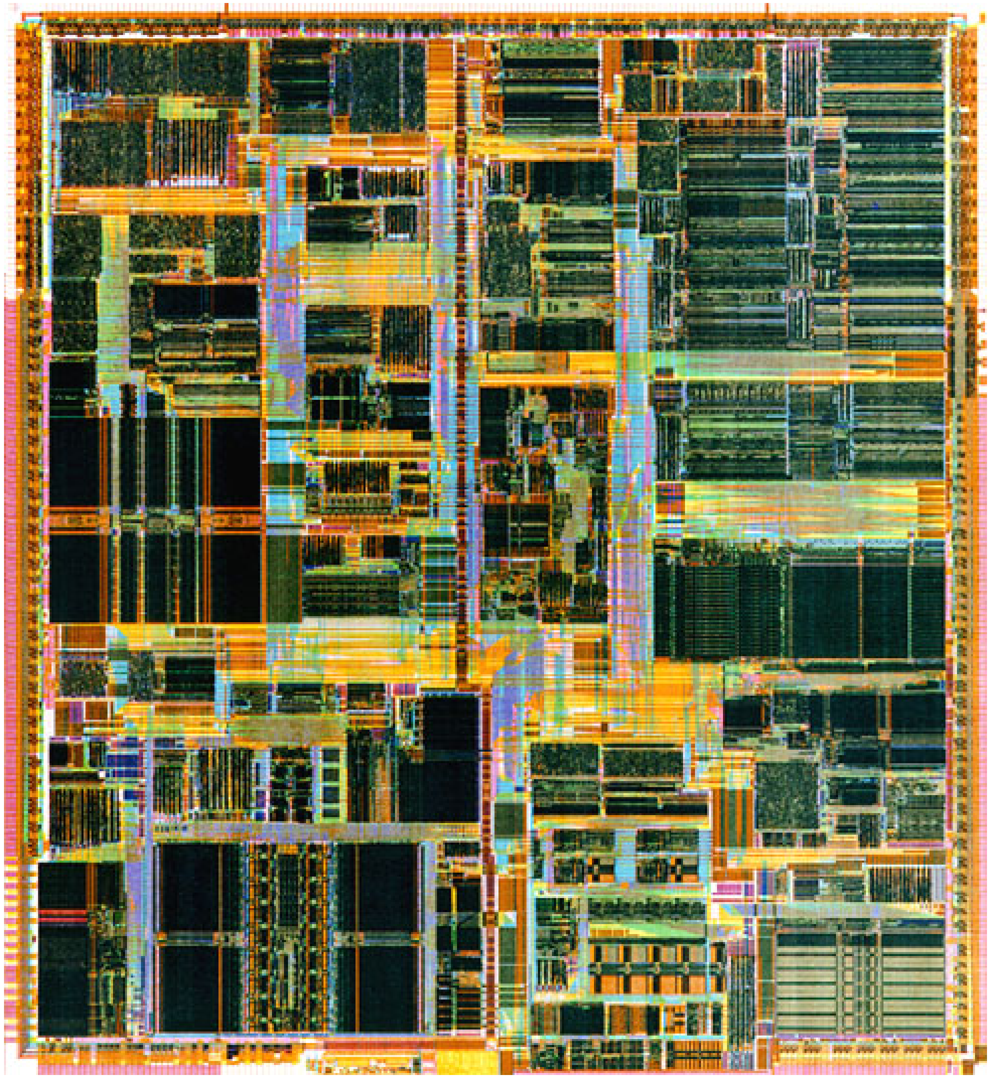
ECL 3-input Gate
Motorola 1966

# Intel 4004 Micro-Processor




1971
1000 transistors
1 MHz operation

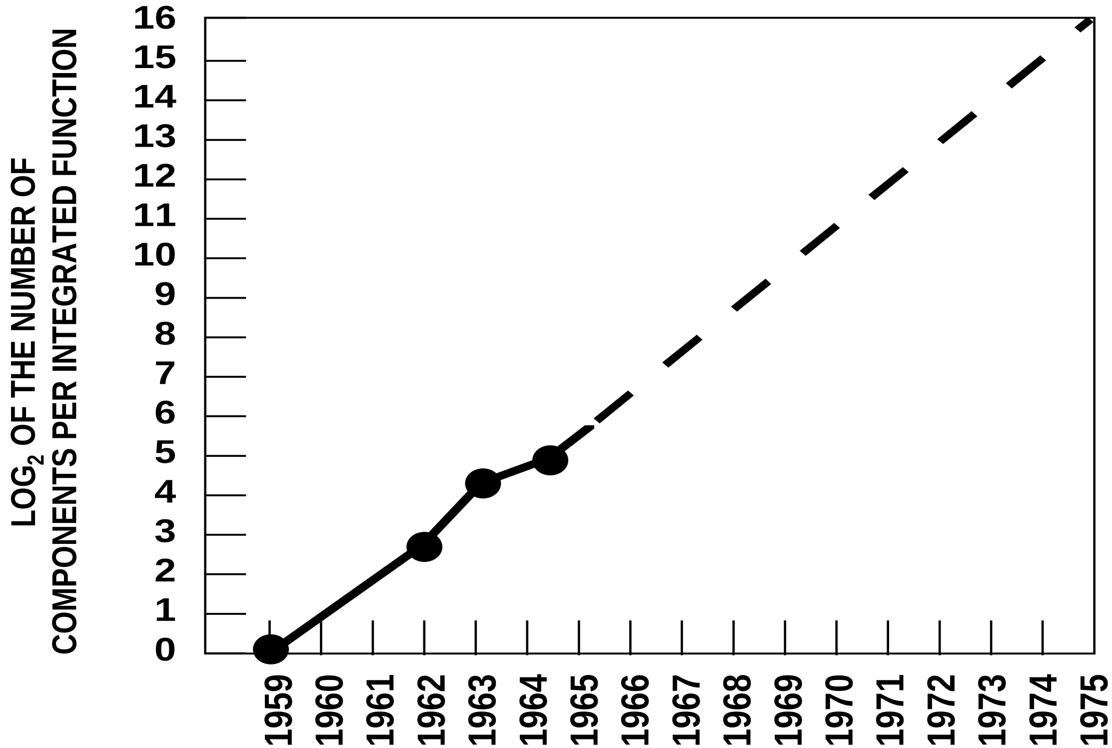
# Intel Pentium (IV) microprocessor



# *Moore's Law*

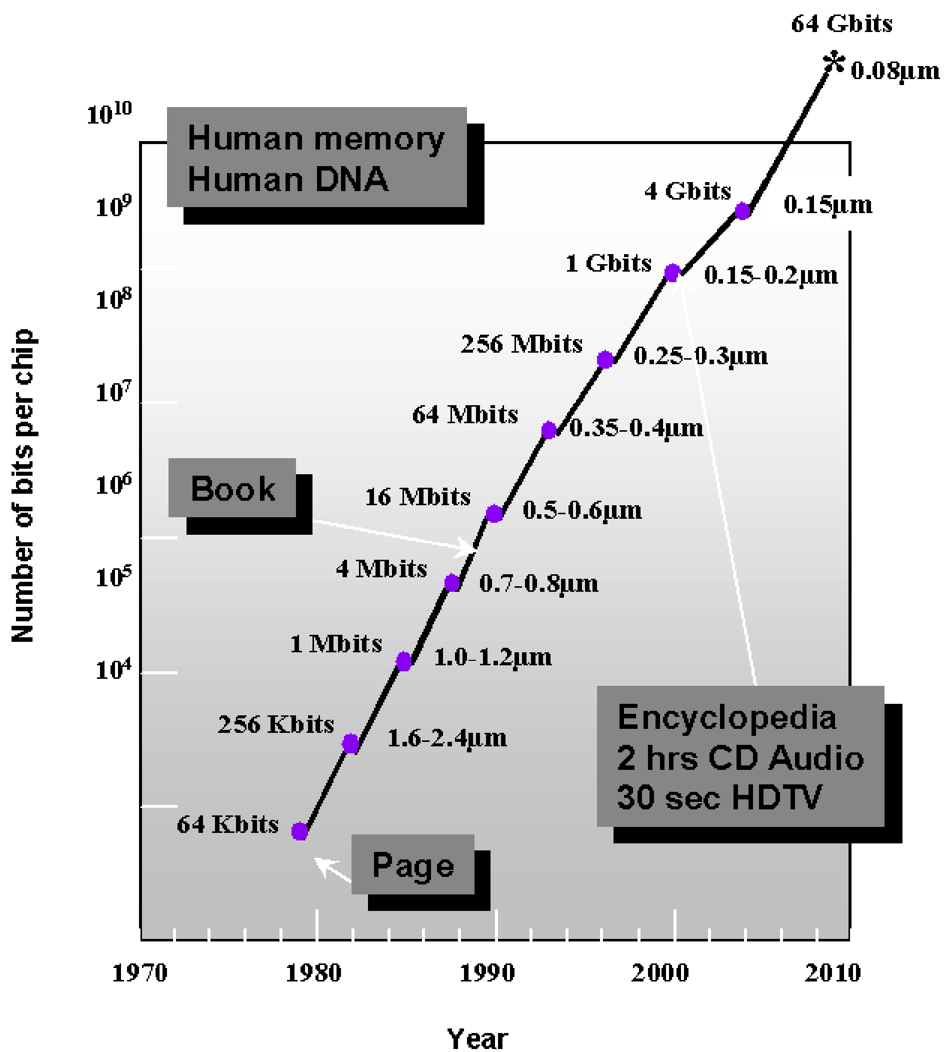
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

# Moore's Law

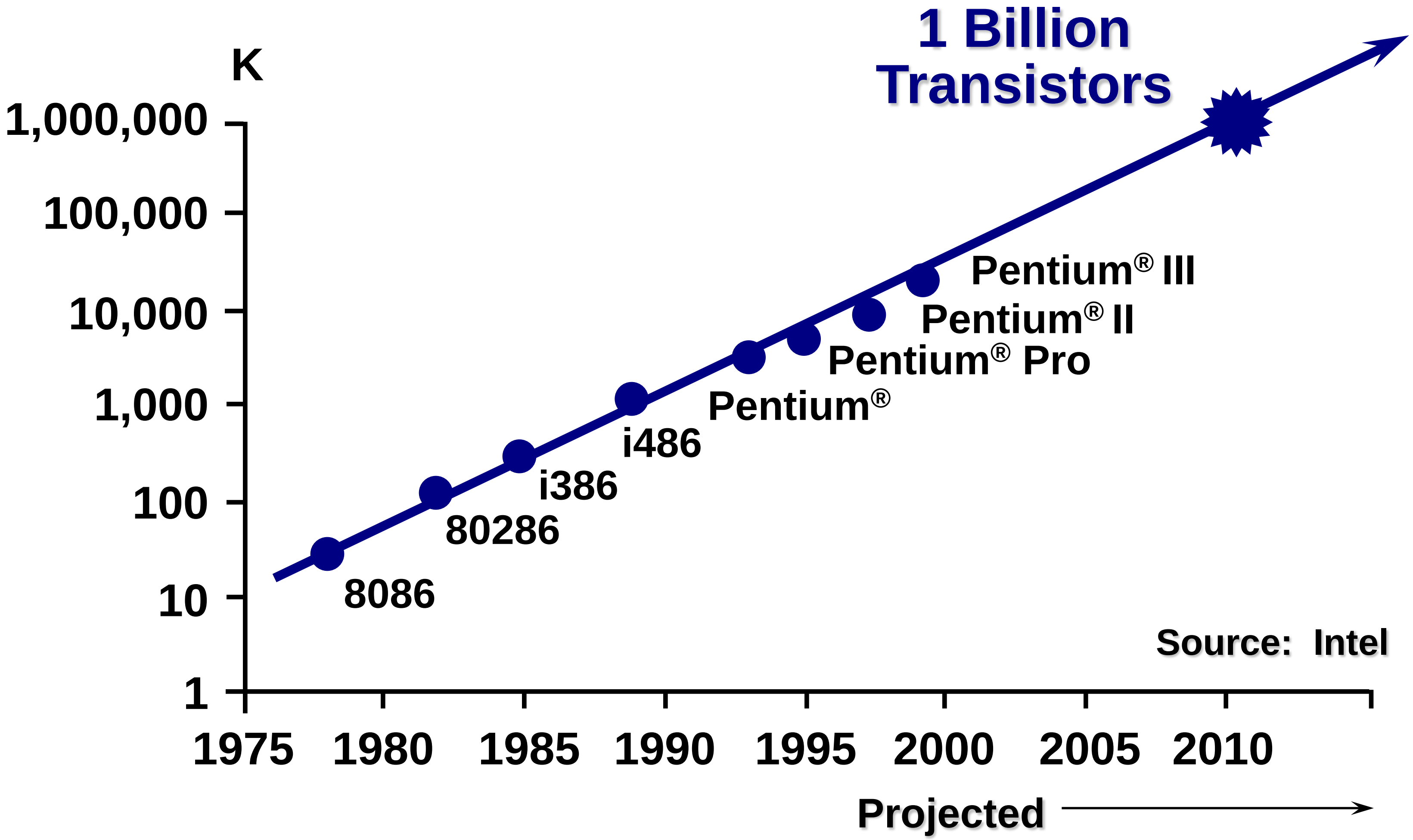



*Electronics*, April 19, 1965.

# Evolution in Complexity

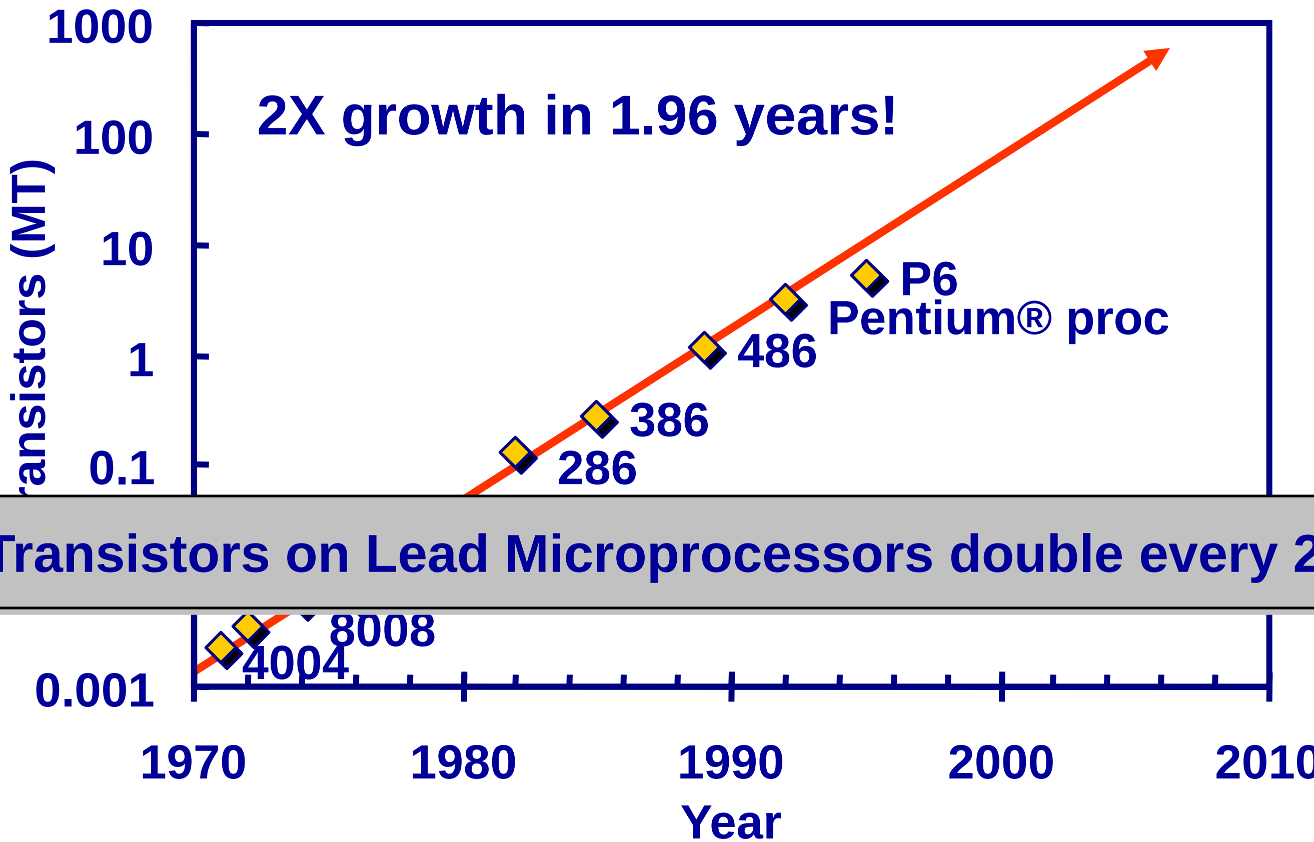


# Transistor Counts




Courtesy, Intel

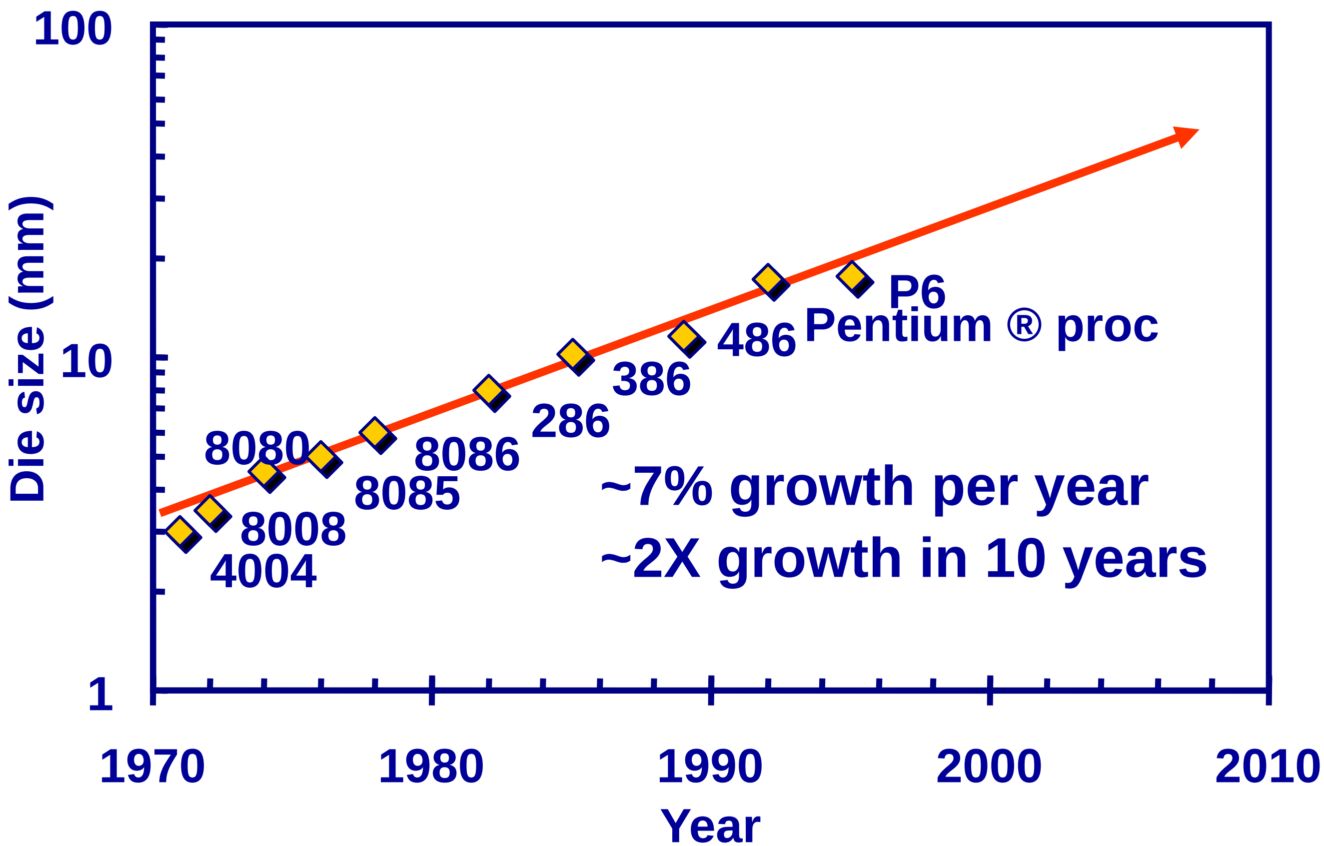
# Moore's law in Microprocessors




Transistors on Lead Microprocessors double every 2 years

Courtesy, Intel

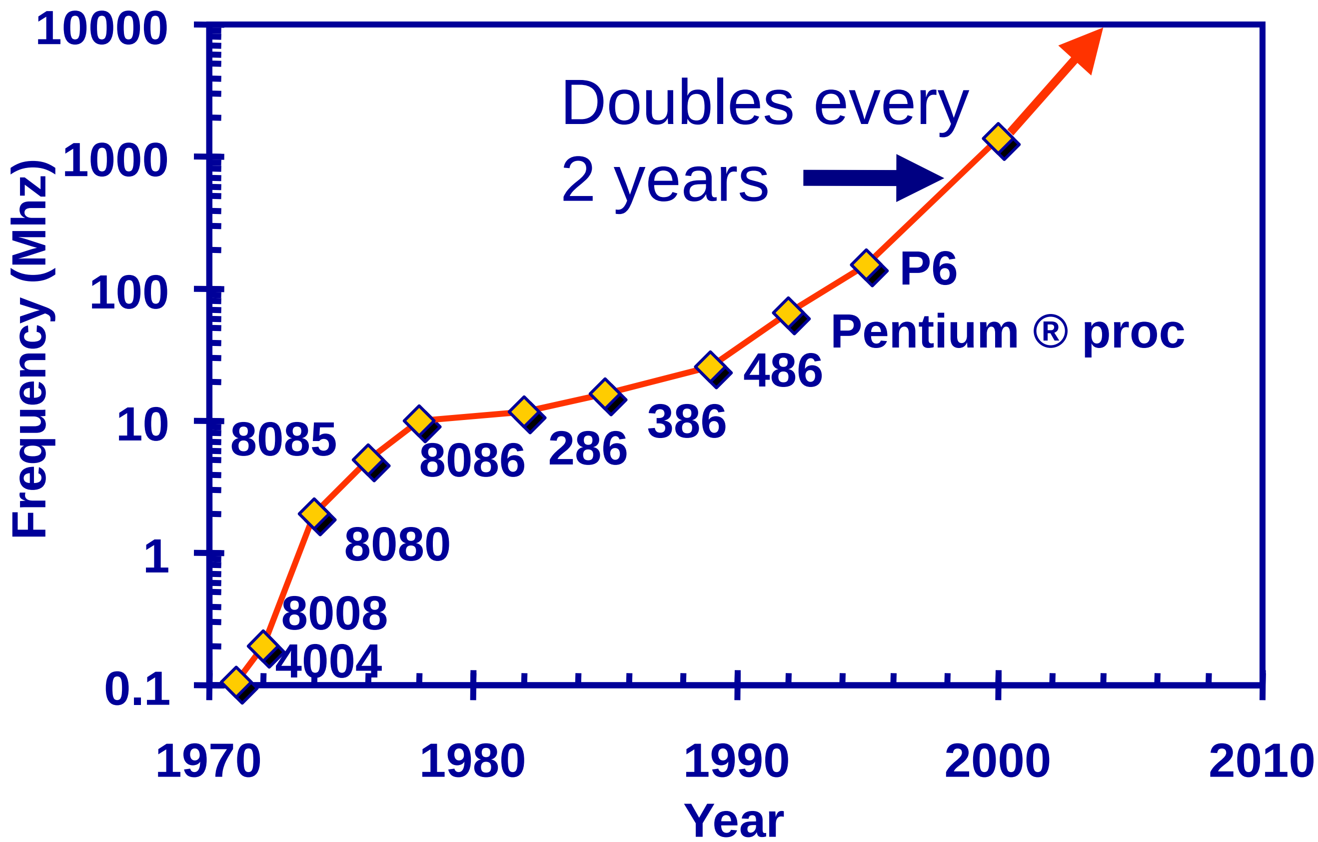
# Die Size Growth




**Die size grows by 14% to satisfy Moore's Law**

Courtesy, Intel

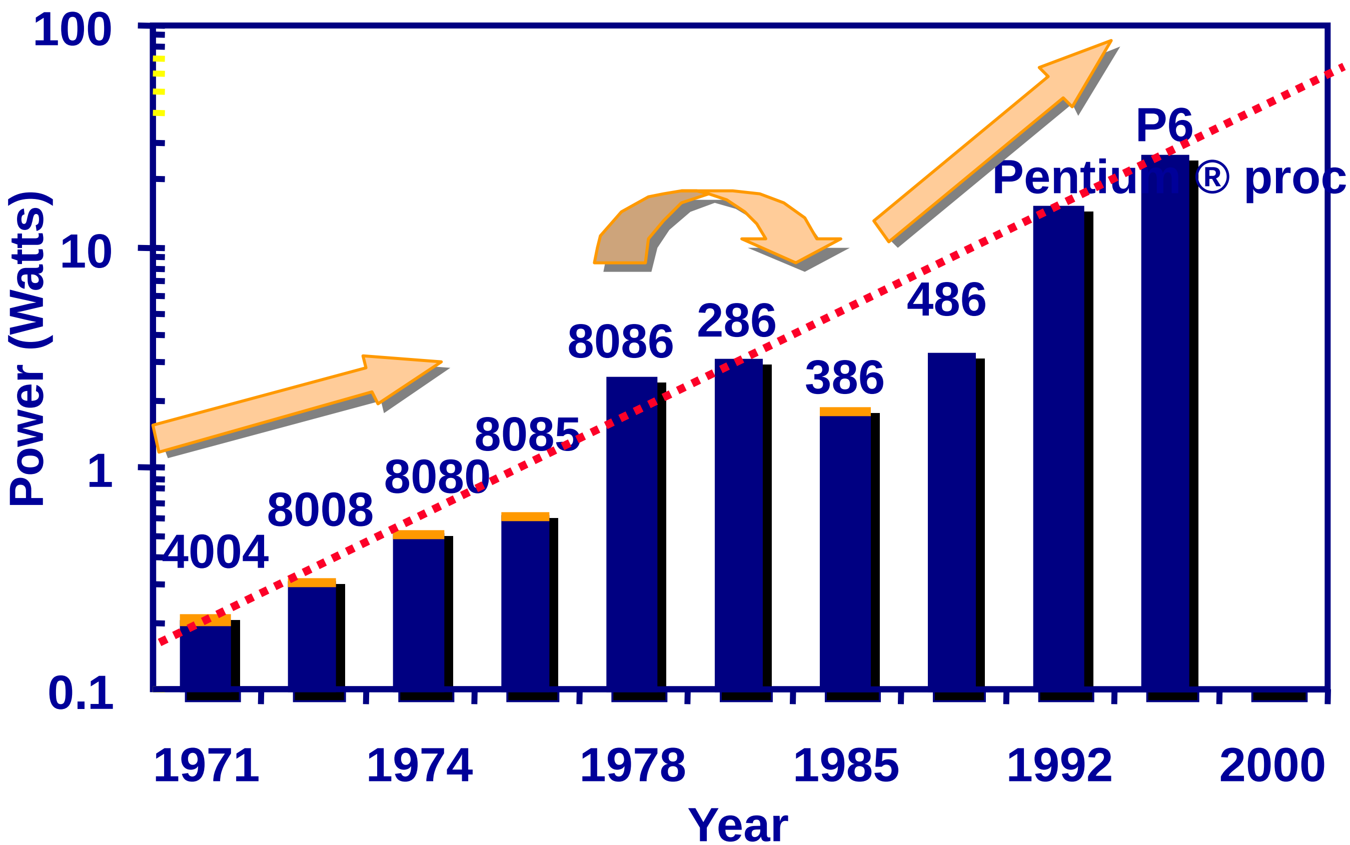
# Frequency




**Lead Microprocessors frequency doubles every 2 years**

Courtesy, Intel

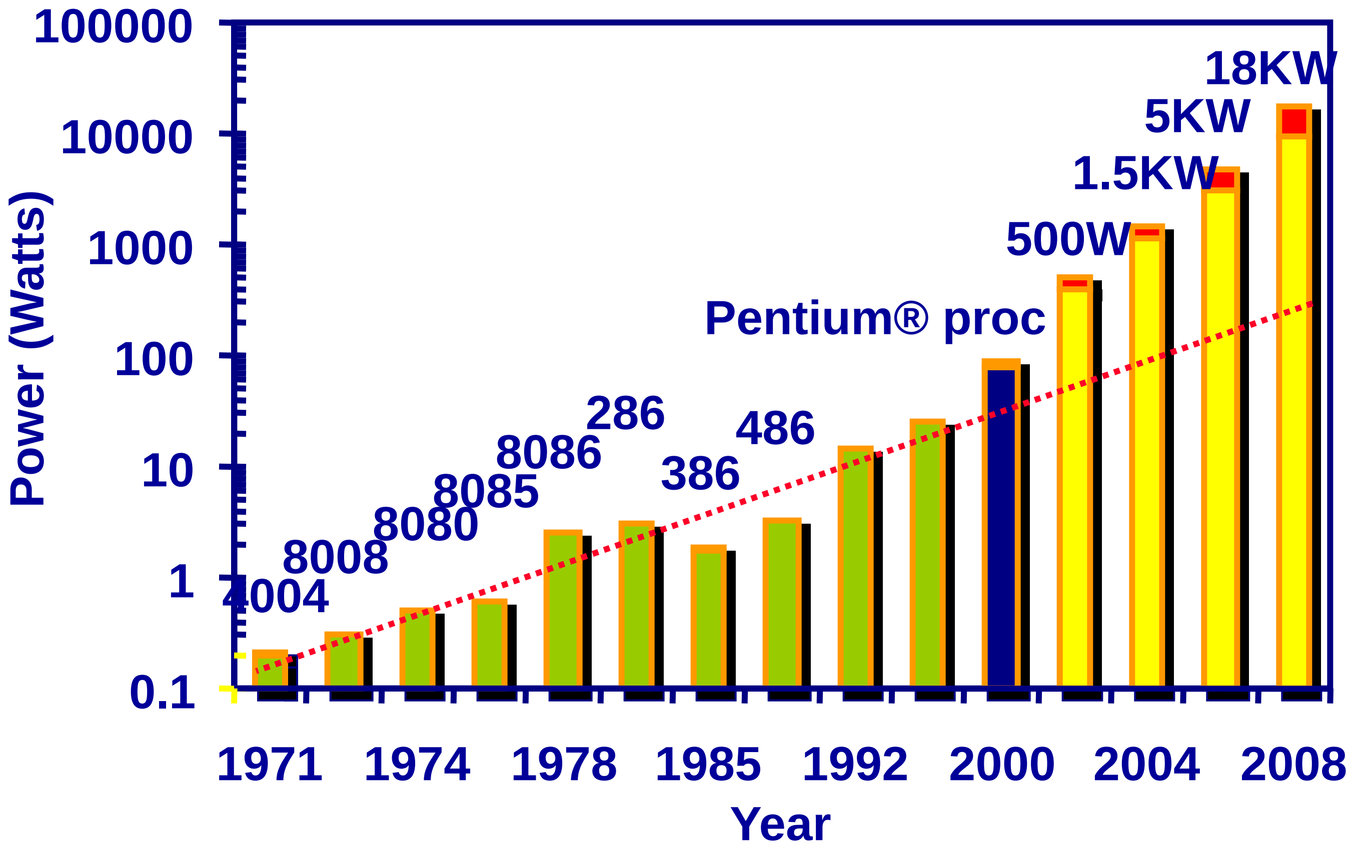
# Power Dissipation




**Lead Microprocessors power continues to increase**

Courtesy, Intel

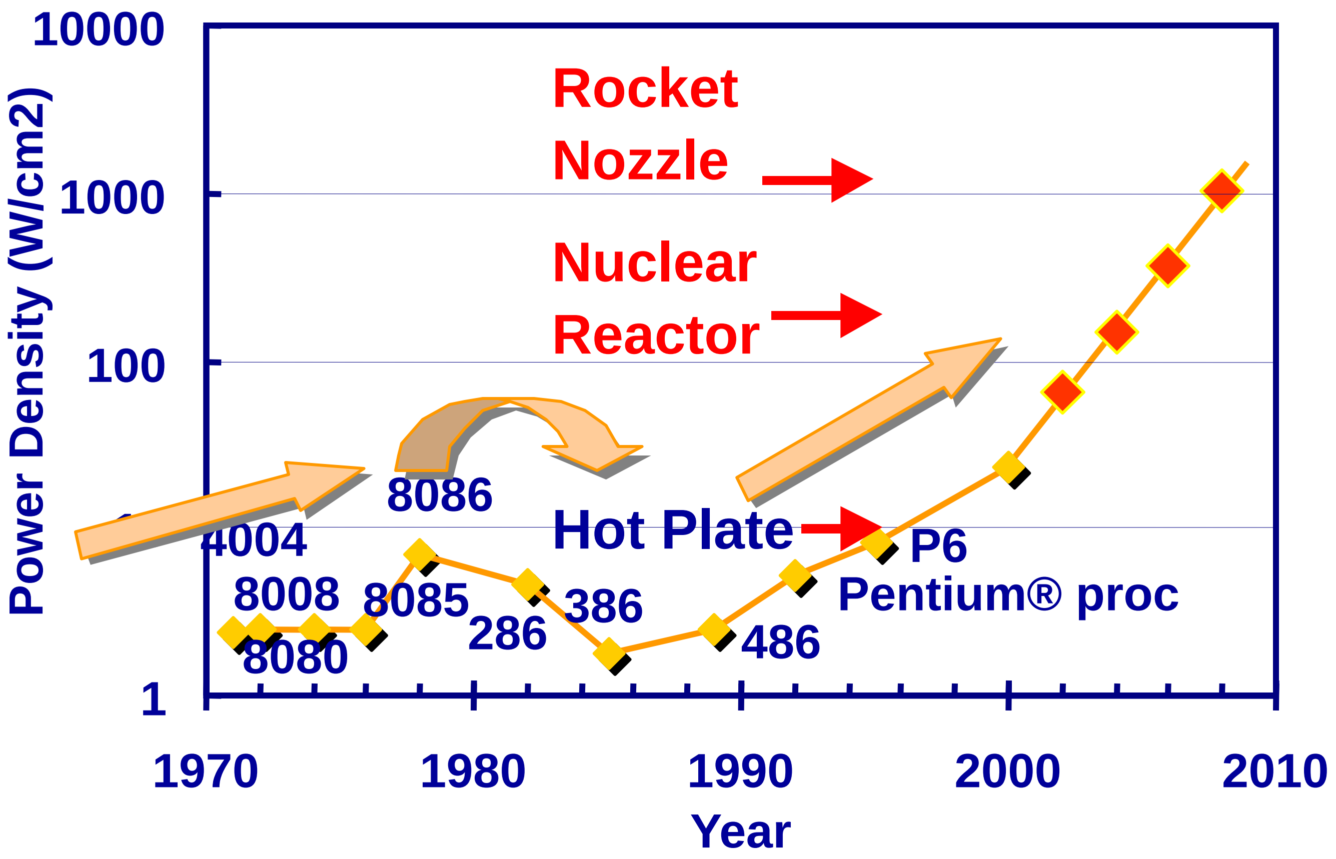
# Power will be a major problem




**Power delivery and dissipation will be prohibitive**

Courtesy, Intel

# Power density

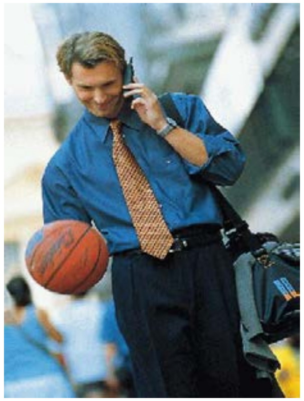


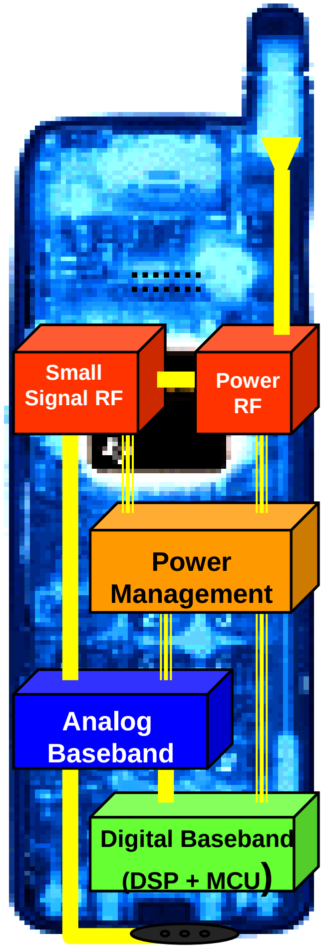

**Power density too high to keep junctions at low temp**

Courtesy, Intel

# *Not Only Microprocessors*

Cell
Phone





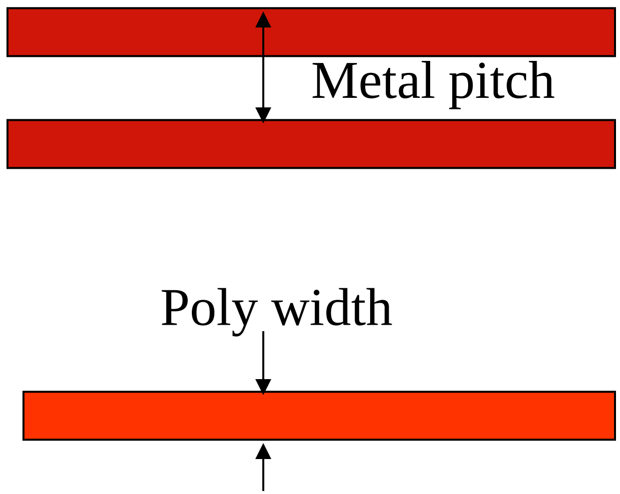

**Digital Cellular Market**
**(Phones Shipped)**

| | 1996 | 1997 | 1998 | 1999 | 2000 |
|---|---|---|---|---|---|
| Units | 48M | 86M | 162M | 260M | 435M |

**(data from Texas Instruments)**

# *MOS Transistor Scaling*
## *(1974 to present)*

Scaling factor **s**=0.7 per node (0.5x per 2 nodes)




Technology Node
set by 1/2 pitch
(interconnect)

Gate length
(transistor)

# Ideal Technology Scaling (constant field)

| Quantity | Before Scaling | After Scaling |
|---|---|---|
| Channel Length | $L$ | $L' = L * s$ |
| Channel Width | $W$ | $W' = W * s$ |
| Gate Oxide thickness | $t_{ox}$ | $t'_{ox} = t_{ox} * s$ |
| Junction depth | $x_j$ | $x'_j = x_j * s$ |
| Power Supply | $V_{dd}$ | $V_{dd}' = Vdd * s$ |
| Threshold Voltage | $V_{th}$ | $V'_{th} = V_{th} * s$ |
| Doping Density, p<br>n+ | $N_A$<br>$N_D$ | $N_A' = N_A / s$<br>$N_D' = N_D / s$ |

# Challenges in Digital Design

## ∝ DSM

**"Microscopic Problems"**

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different


?

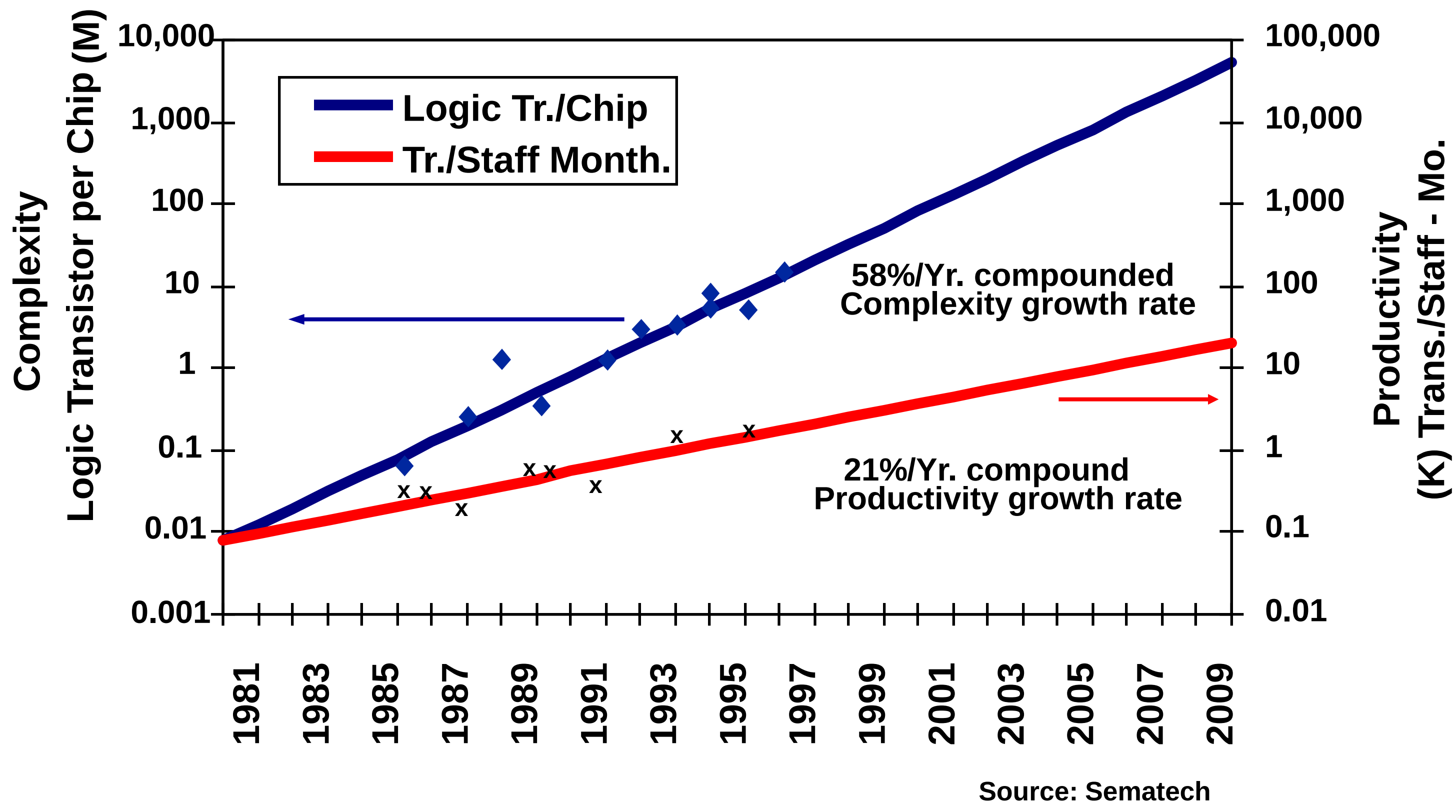
## ∝ 1/DSM

**"Macroscopic Issues"**

- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

…and There's a Lot of Them!

# Productivity Trends



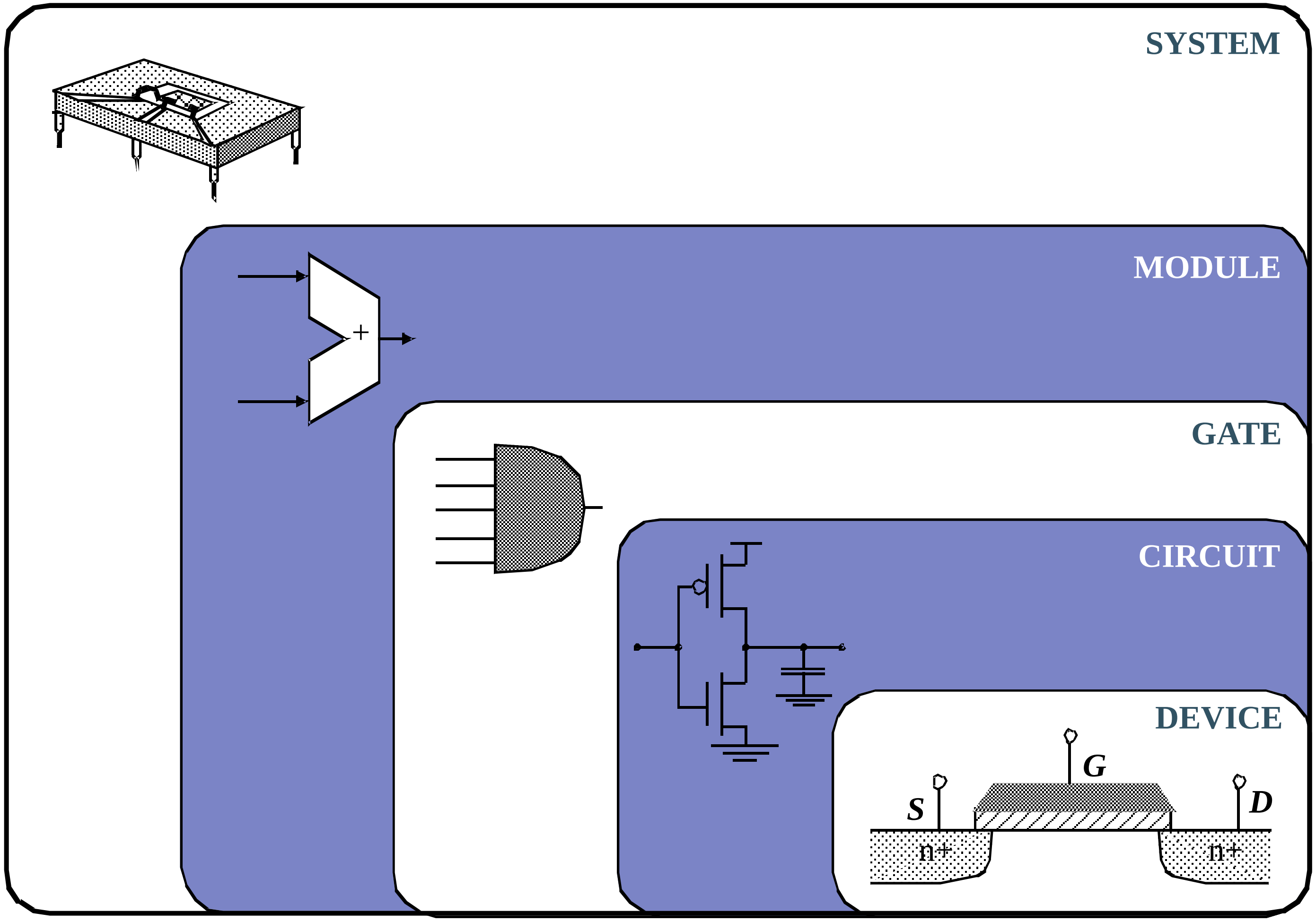

**Complexity outpaces design productivity**

Courtesy, ITRS Roadmap

# Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

# Design Abstraction Levels



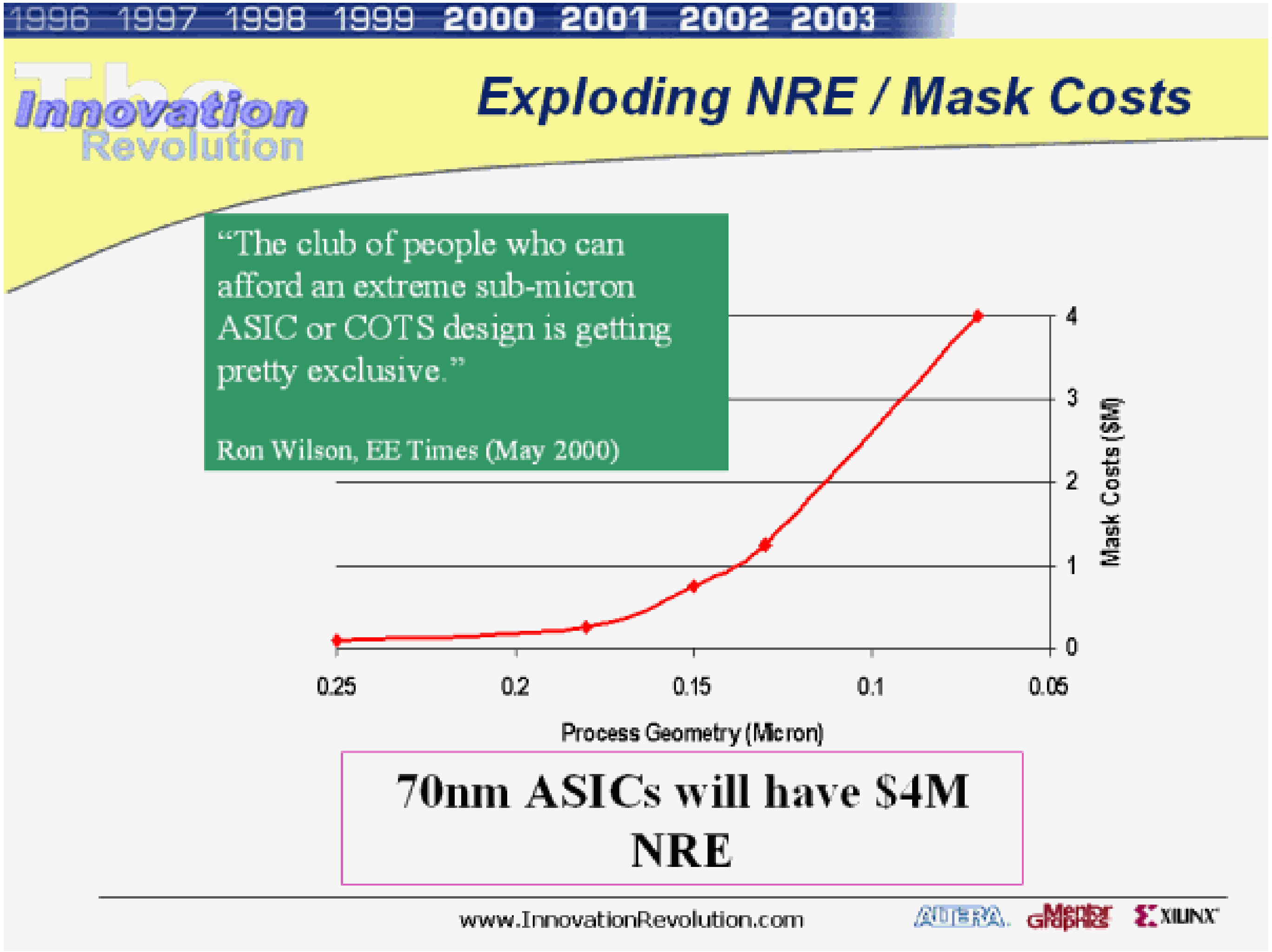
# Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

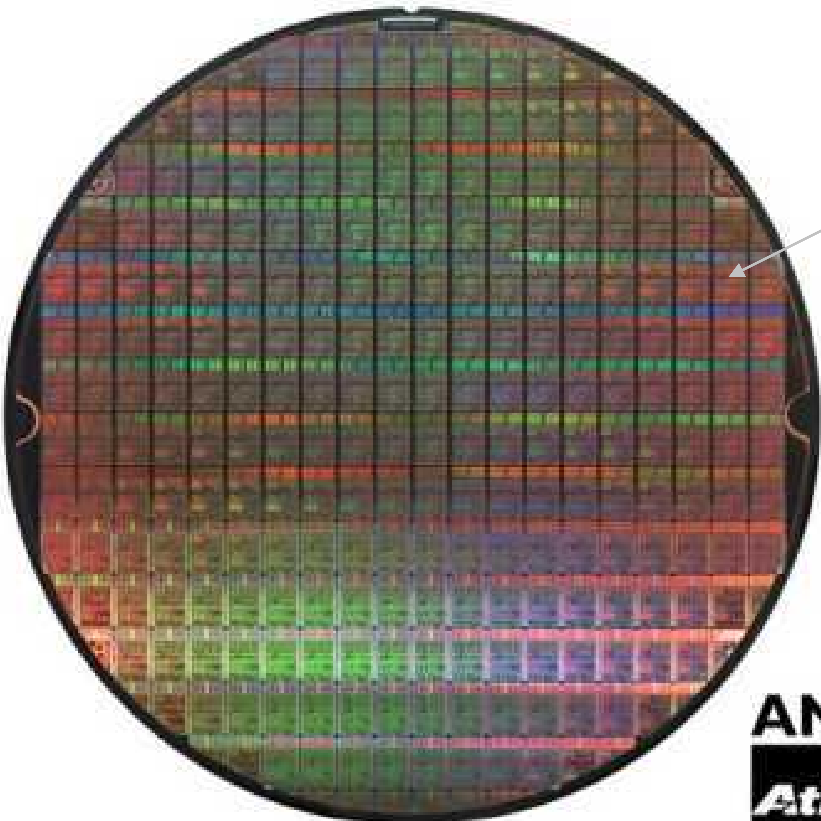
# Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area

# NRE Cost is Increasing



# Die Cost



Single die

Wafer

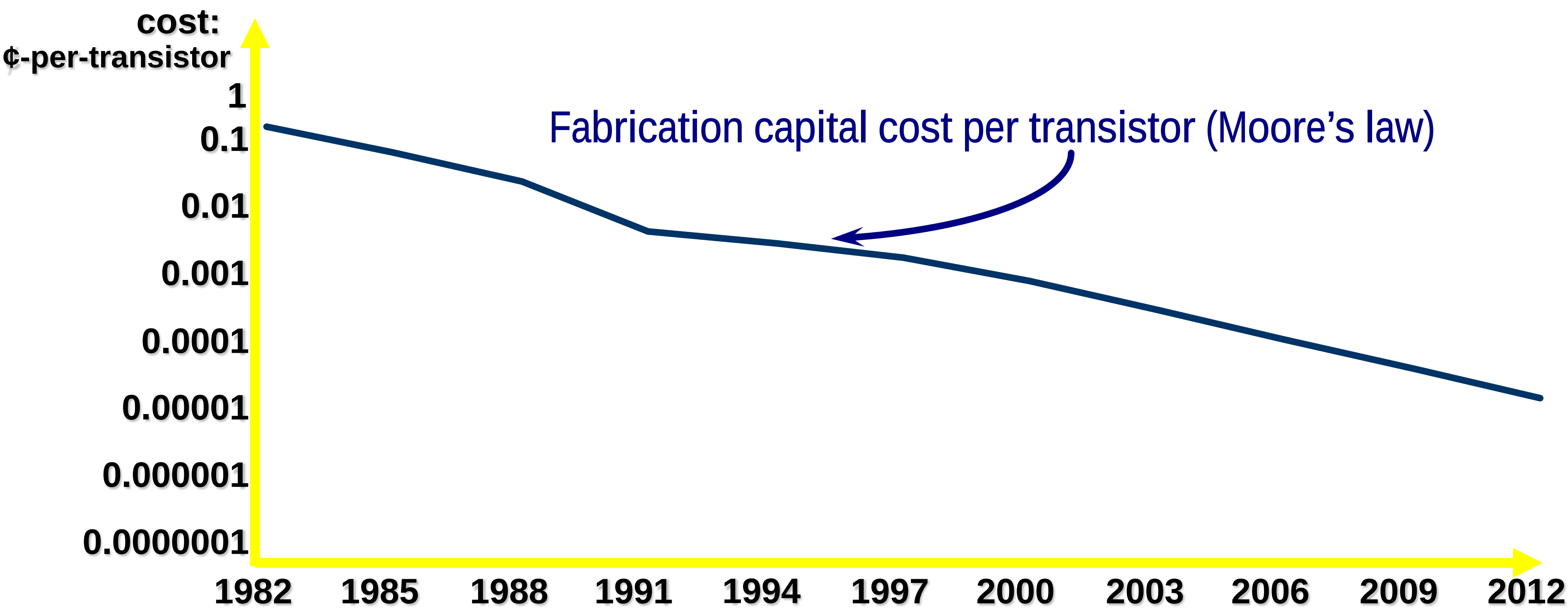
AMD

Athlon

Going up to 12" (30cm)

From http://www.amd.com

# Cost per Transistor

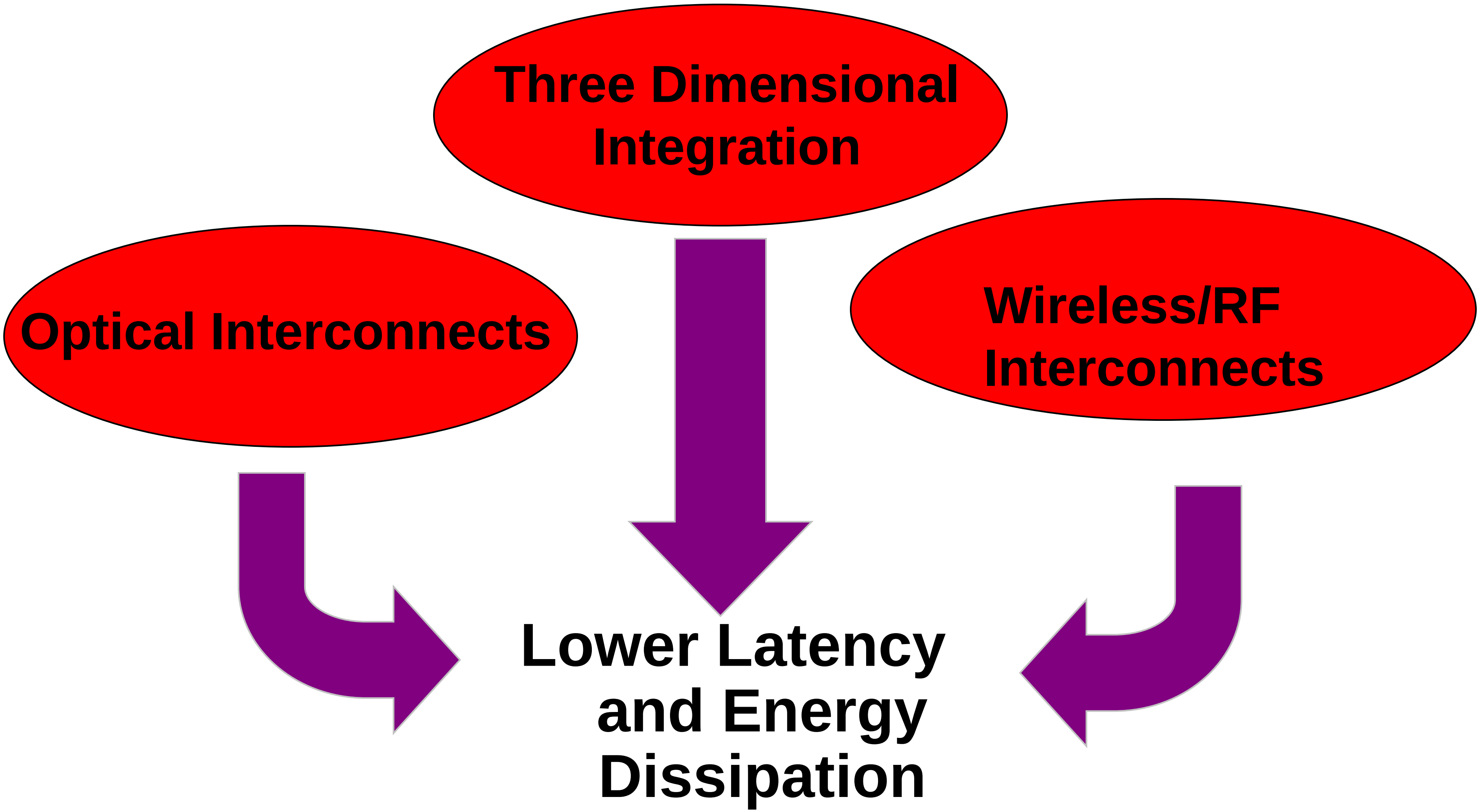


# *What about Interconnect*

- Global wires
  - Non-scalable delay
  - Delay exceeds one clock cycle

- Non-scalable interconnects
- Excessive power dissipation
- Non reliability in signal transmission

# *Emerging Interconnect Technologies*



# Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this course
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation

# Course Structure

- MOS Transistors
- MOS Inverter Circuits
- Static MOS Gate Circuits
- High-Speed CMOS Logic Design
- Transfer Gate and Dynamic Logic Design
- Semiconductor Memory Design
- Advanced Devices beyond CMOS

# *Course Structure*

- Extensive use of CAD tools
- Homework assignments
- One to two midterm exams and one final exam
- Course Project

Suite of two courses EE 466/586 and EE587 will cover various aspects starting from circuits to systems

# References

- **Textbook:**
  - CMOS VLSI Design, Weste and Harris, Fourth Edition
- **Additional Reference:**
  - Analysis and Design of Digital Integrated Circuits - In Deep Submicron Technology, Hodges, Jackson and Saleh, McGraw-Hill, Third Edition, 2004.
  - J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective. Second Edition, Prentice Hall, 2003.
- Important announcements will be posted in the course website
  - www.eecs.wsu.edu/~ee586