EE 466/586
VLSI Design

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Lecture 3

The MOS Transistor (Cont’d)

Alpha Power law Model

- *Empirically fit real data*
- *Current in saturation*

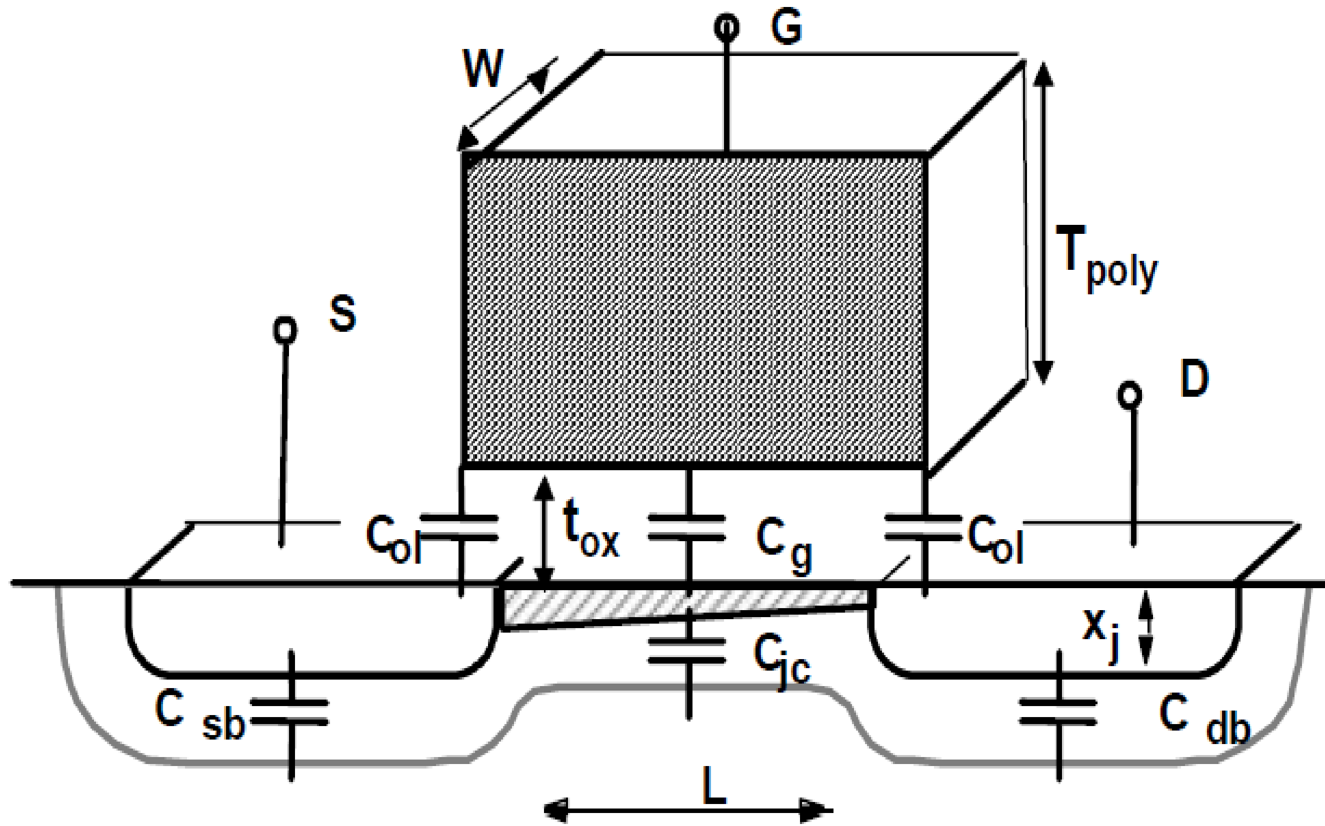
$$I_{DS} = K_S \frac{W}{L} (V_{GS} - V_T)^{\alpha}$$

- *Current in linear region*

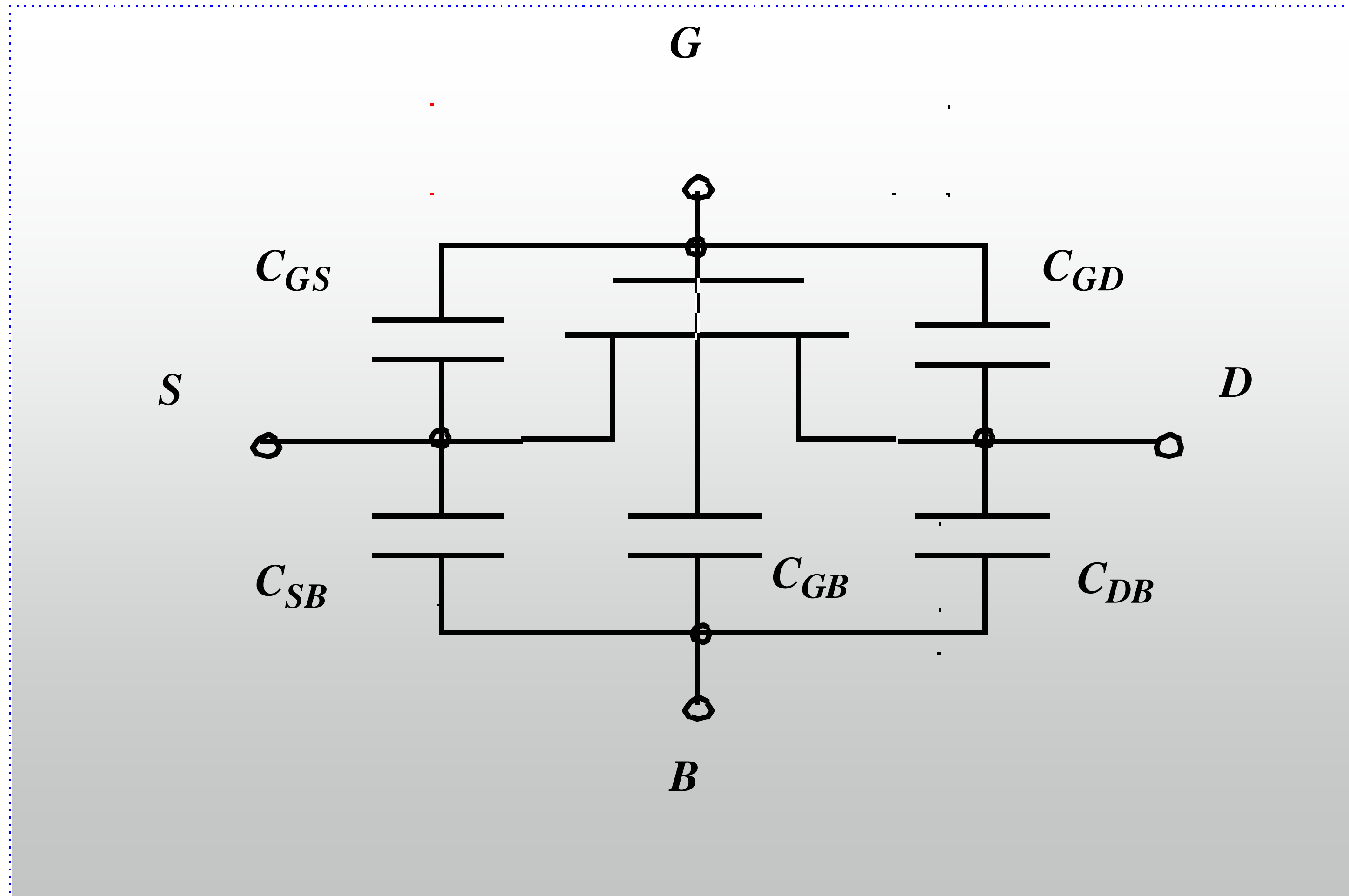
$$I_{DS} = K_L \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$V_{DSat} = \frac{K_S}{K_L} (V_{GS} - V_T)^{\alpha - 1}$$

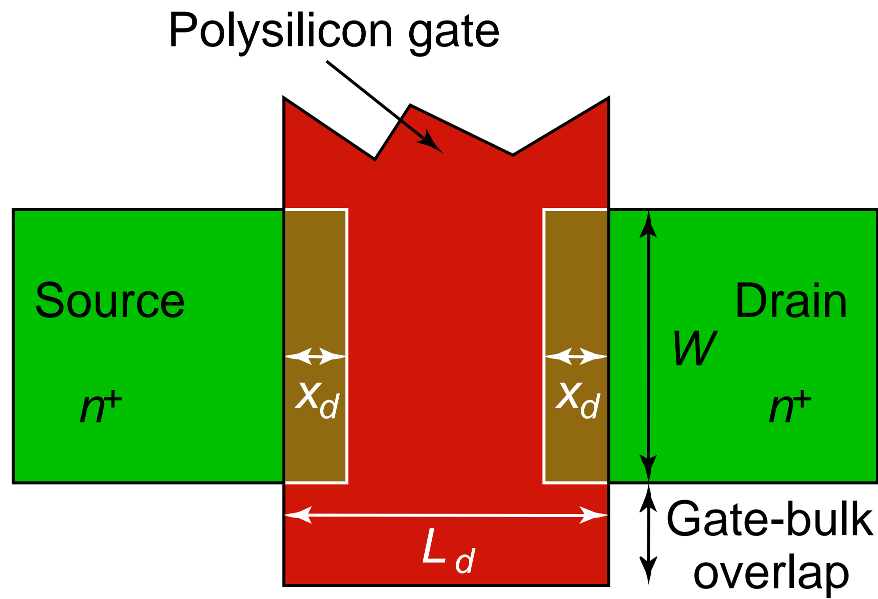
Capacitance



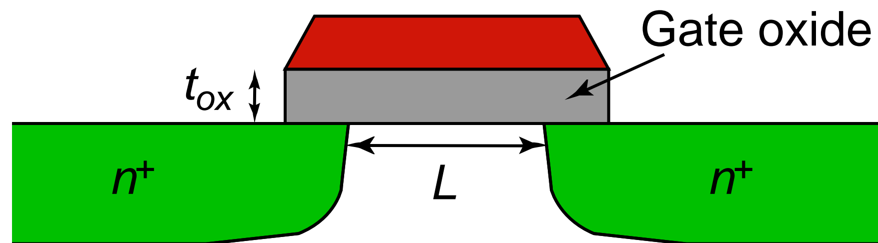
Dynamic Behavior of MOS Transistor



The Gate Capacitance



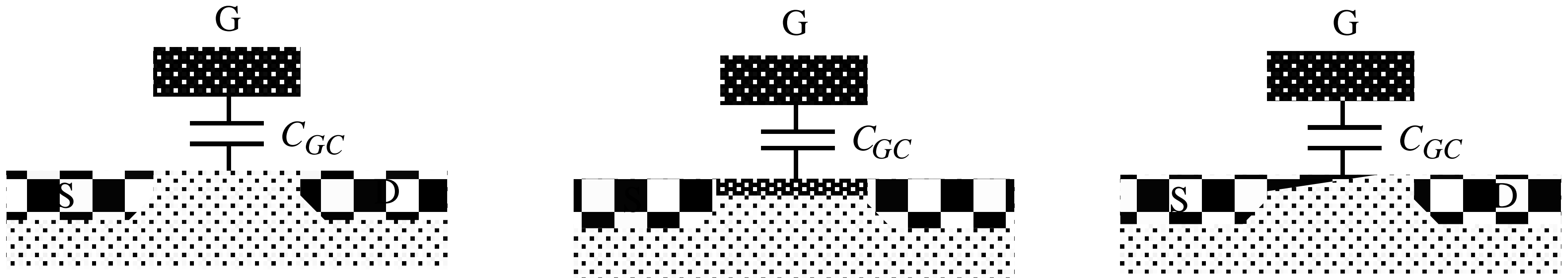
Top view



Cross section

$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

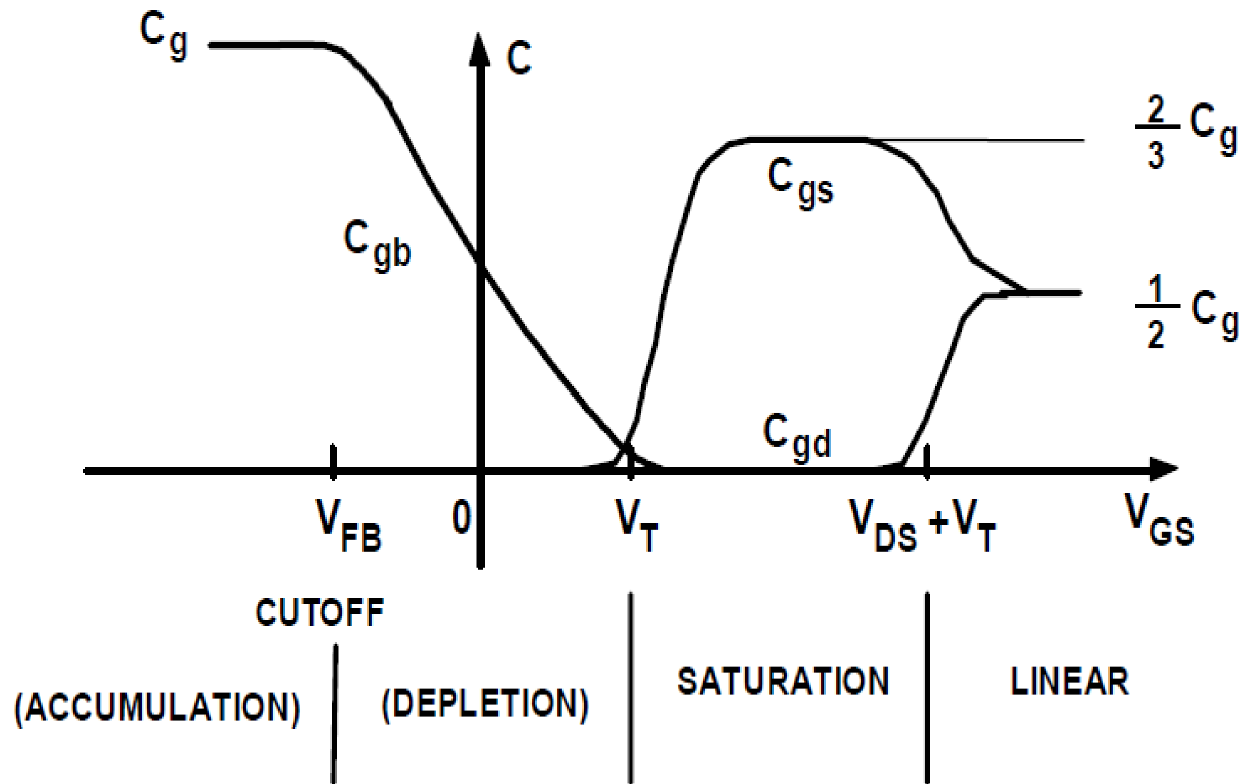
Gate Capacitance



Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

Thin Oxide Capacitance



P-N Junction Capacitance

- The capacitances *Csb* and *Cdb* are n+p source/drain junction capacitances for NMOS devices
- For PMOS devices, the capacitances are due to p+n source/drain junctions.

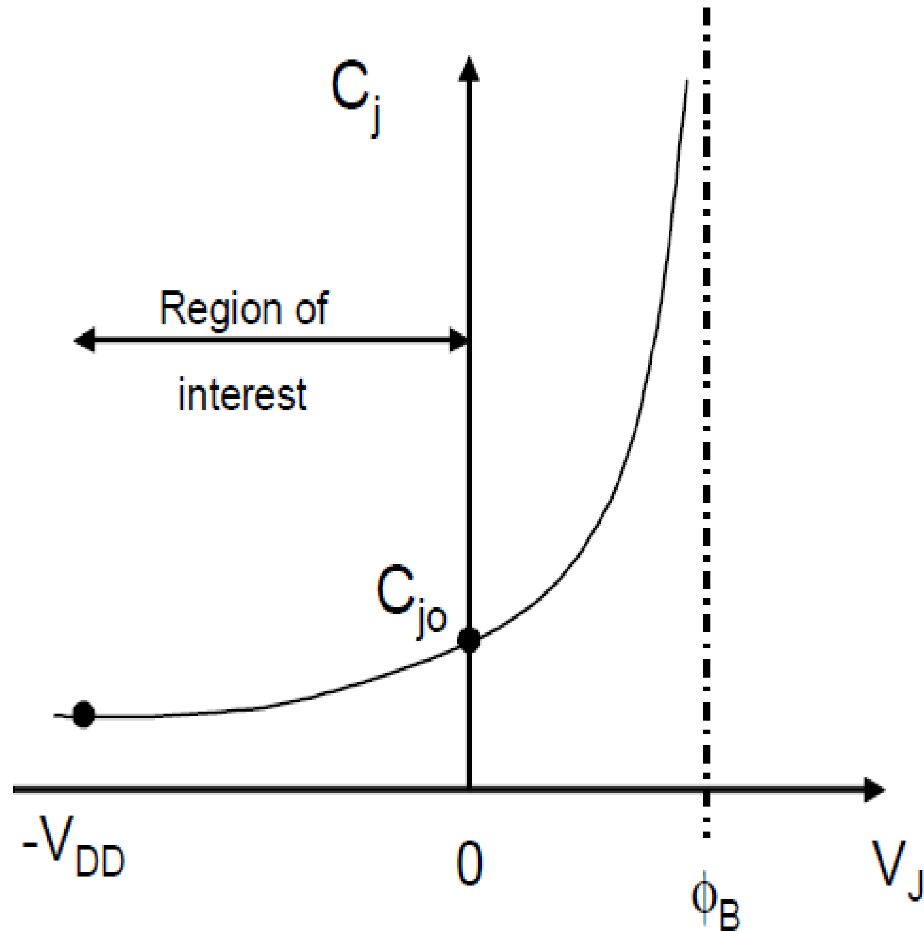
$$I_D = I_S(e^{V_J/V_{th}} - 1)$$

$$\phi_B = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}$$

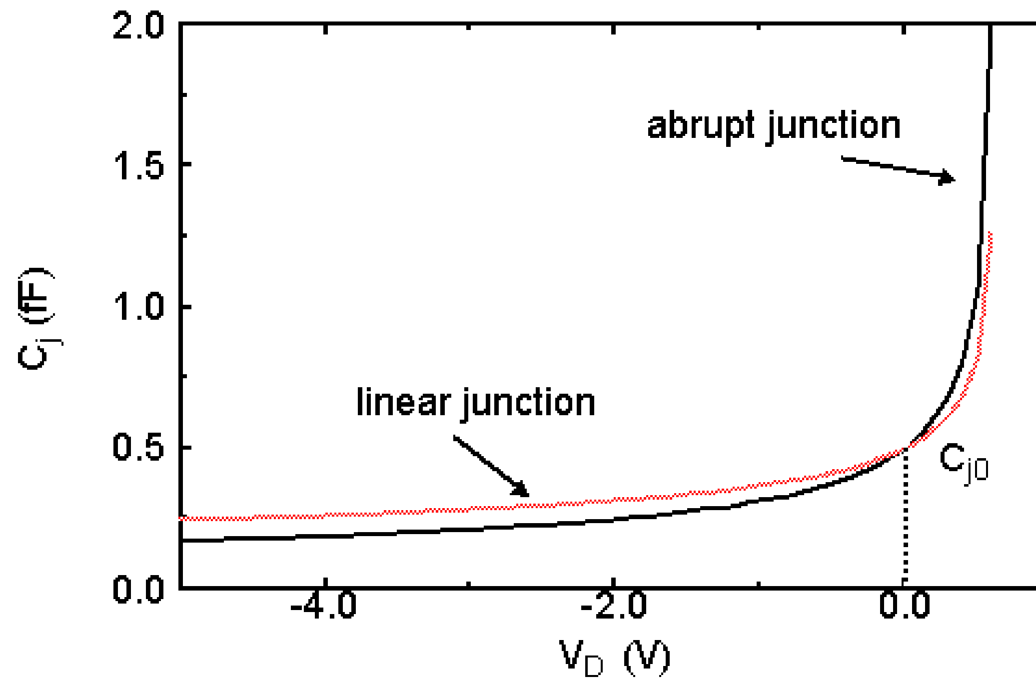
P-N Junction Capacitance

$$C_J = \frac{C_{jo} A}{(1 - \frac{V_J}{\phi_B})^m}$$

$$C_{jo} = \sqrt{\frac{\varepsilon_{si} q}{2\phi_B} \frac{N_A N_D}{N_A + N_D}}$$

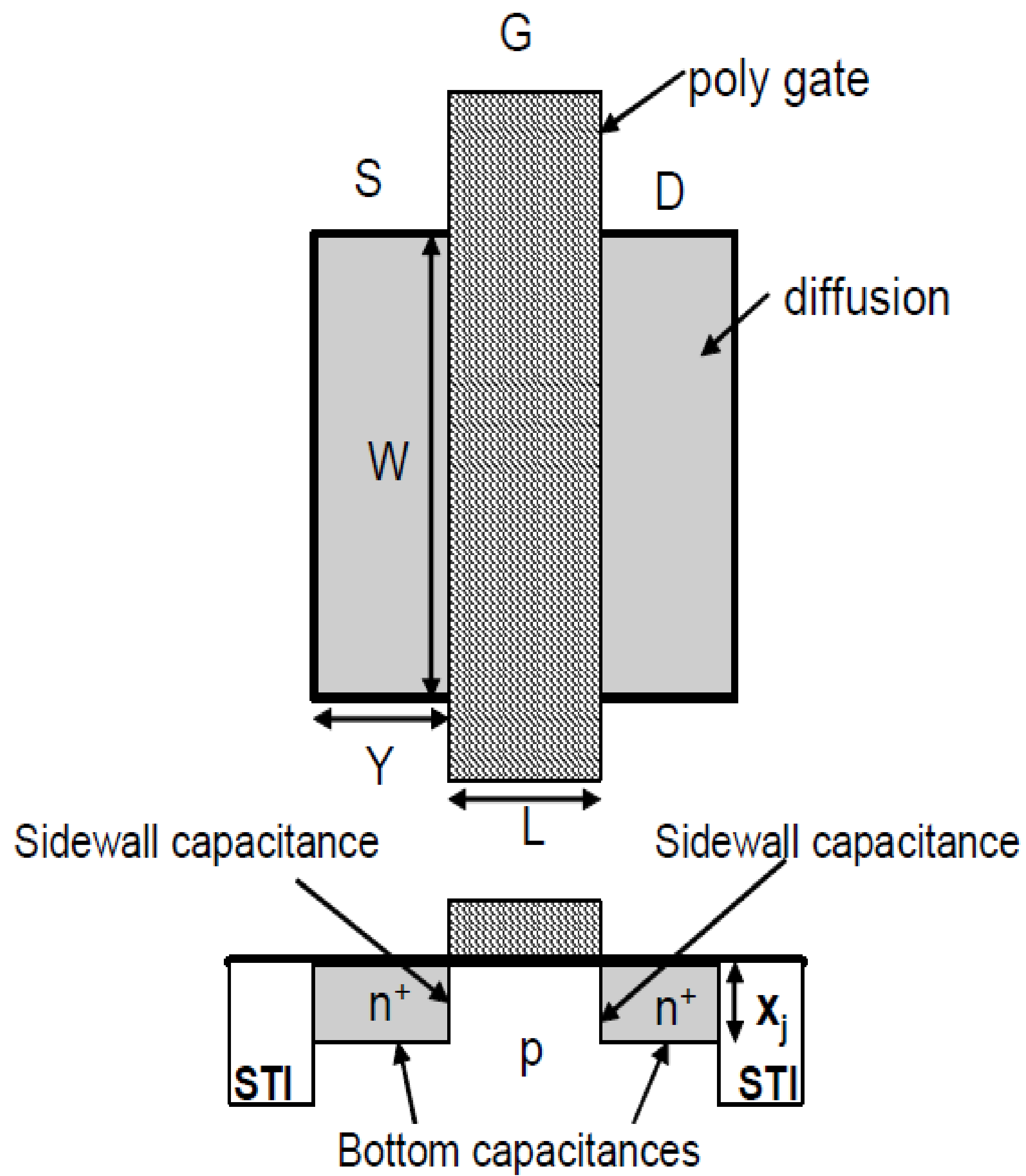


Junction Capacitance

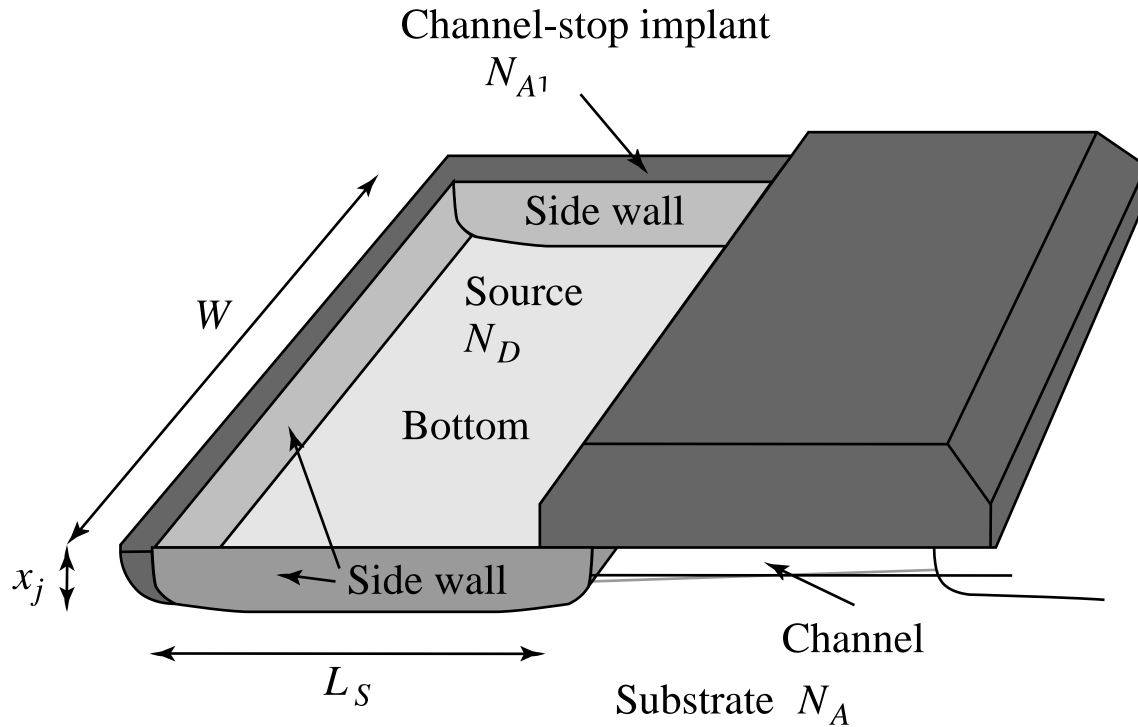


$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction


G
poly gate
S
D
diffusion
W
Y
L
Sidewall capacitance
Sidewall capacitance
n+
n+
Xj
p
STI
STI
Bottom capacitances

Diffusion Capacitance



Diffusion Capacitance (Cont'd)

$$C_J = \frac{C_{jb} A_b}{\left(1 - \frac{V_J}{\phi_{Bb}}\right)^{mj}} + \frac{C_{jsw} A_{sw}}{\left(1 - \frac{V_J}{\phi sw}\right)^{mjsw}}$$

$$A_{sw} = W x_j$$

$$A_b = WY$$

$$C_J = \frac{C_{jb} A_b + C_{jb} A_{sw}}{\left(1 - \frac{V_J}{\phi_B}\right)^{mj}} = \frac{C_{jb}(A_b + A_{sw})}{\left(1 - \frac{V_J}{\phi_B}\right)^{mj}}$$

Linearizing the Junction Capacitance

$$C_{eq} = \frac{Q_j(V_2) - Q_j(V_1)}{V_2 - V_1} = \frac{\Delta Q}{\Delta V}$$

$$\Delta Q = \int_{V_1}^{V_2} C(V)\,dV = \int_{V_1}^{V_2} C_{jb}\left(1 - \frac{V}{\phi_B}\right)^{-m} dV$$

$$C_{eq} = -\frac{C_{jb}\phi_B}{(V_2 - V_1)(1-m)}\left[\left(1 - \frac{V_2}{\phi_B}\right)^{1-m} - \left(1 - \frac{V_1}{\phi_B}\right)^{1-m}\right]$$

Final Expression

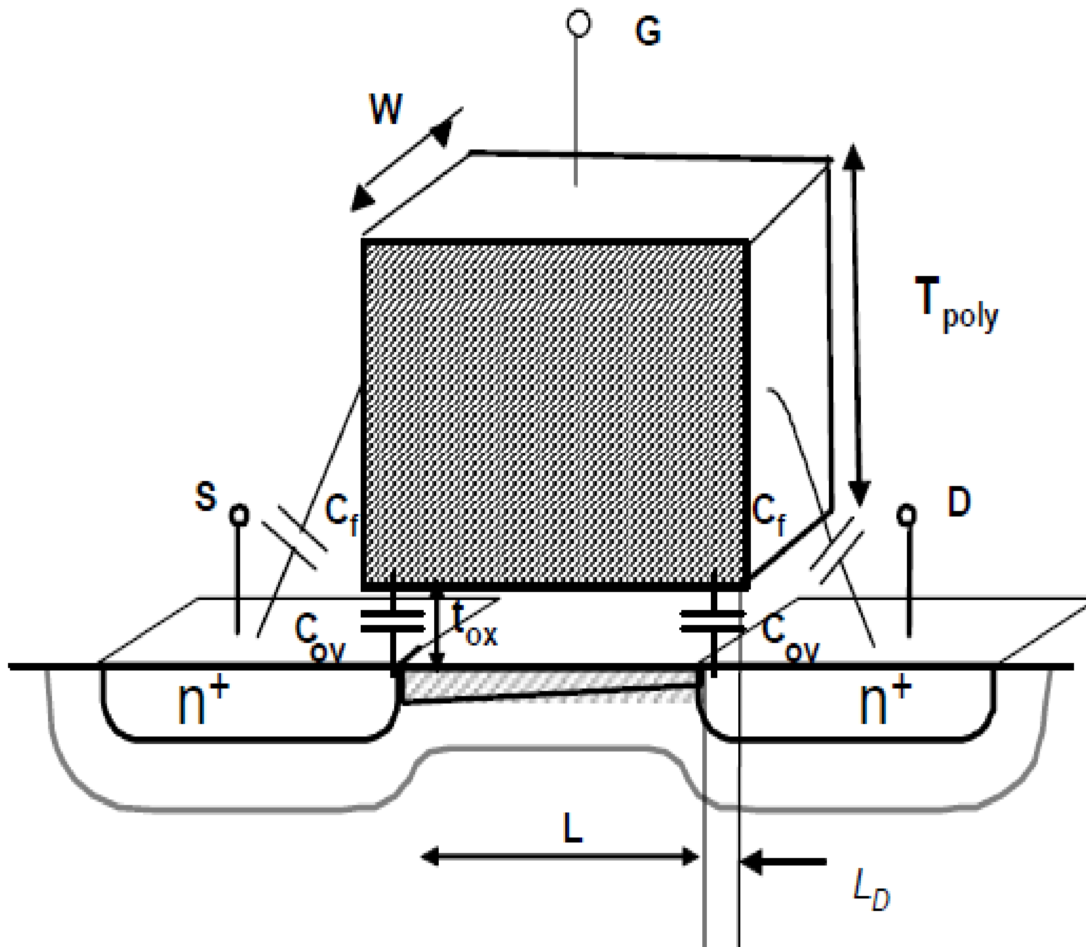
$$C_J = K_{eq}(C_{jb}WY + C_{jb}x_jW) = K_{eq}(C_{jb}Y + C_{jb}x_j)W = K_{eq}C_{jb}(Y + x_j)W$$

$$C_J = K_{eq}C_{jb}(Y + x_j)W = C_jW$$

Capacitances in 0.25 μm CMOS process

	C_{ox} (fF/μm²)	C_O (fF/μm)	C_j (fF/μm²)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Overlap Capacitance

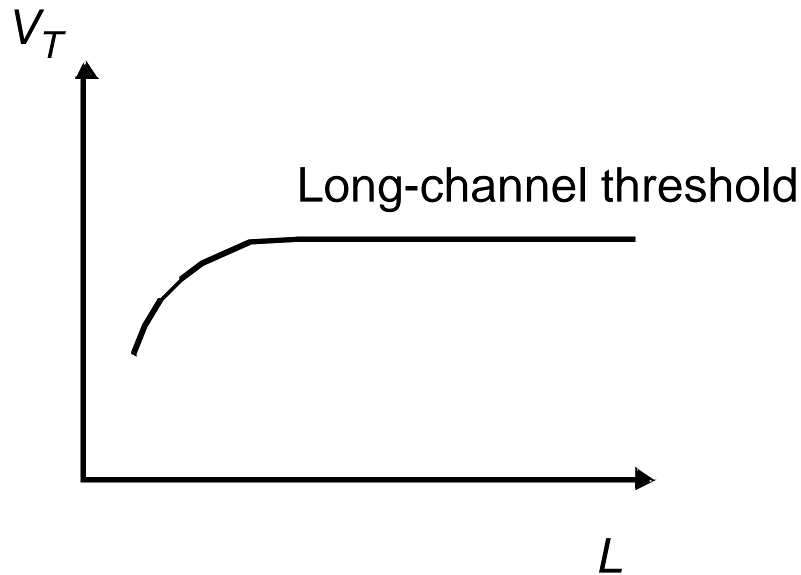


- *Lateral diffusion and fringing*
- *Diffusion of the heavily-doped source and drain regions under the gate.*
- *fringing capacitance, between the sidewall of the Polysilicon and the surface of the drain and source*

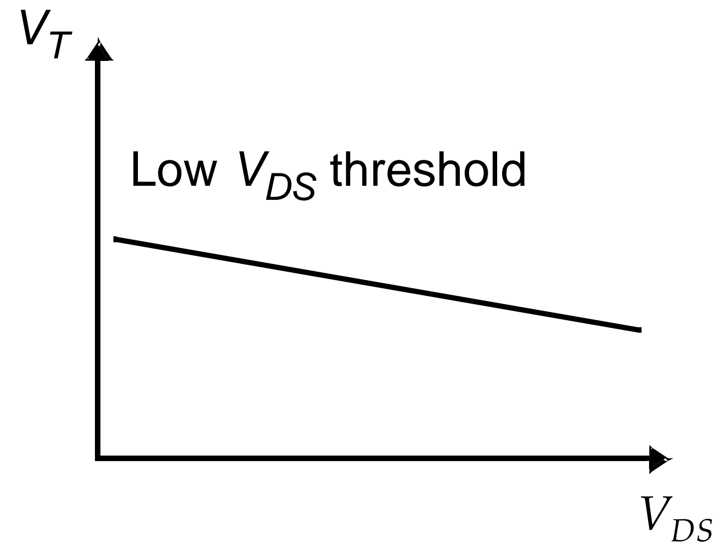
The Sub-Micron MOS Transistor

- Threshold Variations
- Subthreshold Conduction
- Parasitic Resistances

Threshold Variations



Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Part of the region below the gate is already depleted

Sub-Threshold Conduction

- Diffusion of minority carriers
- MOS transistor behaves more like a (lateral) bipolar transistor.
- The substrate is the base region, while the source and drain act as the emitter and collector, respectively.

$$I_{sub} = I_s e^{\frac{q(V_{GS} - V_T - V_{offset})}{nkT}} (1 - e^{\frac{-qV_{DS}}{kT}})$$

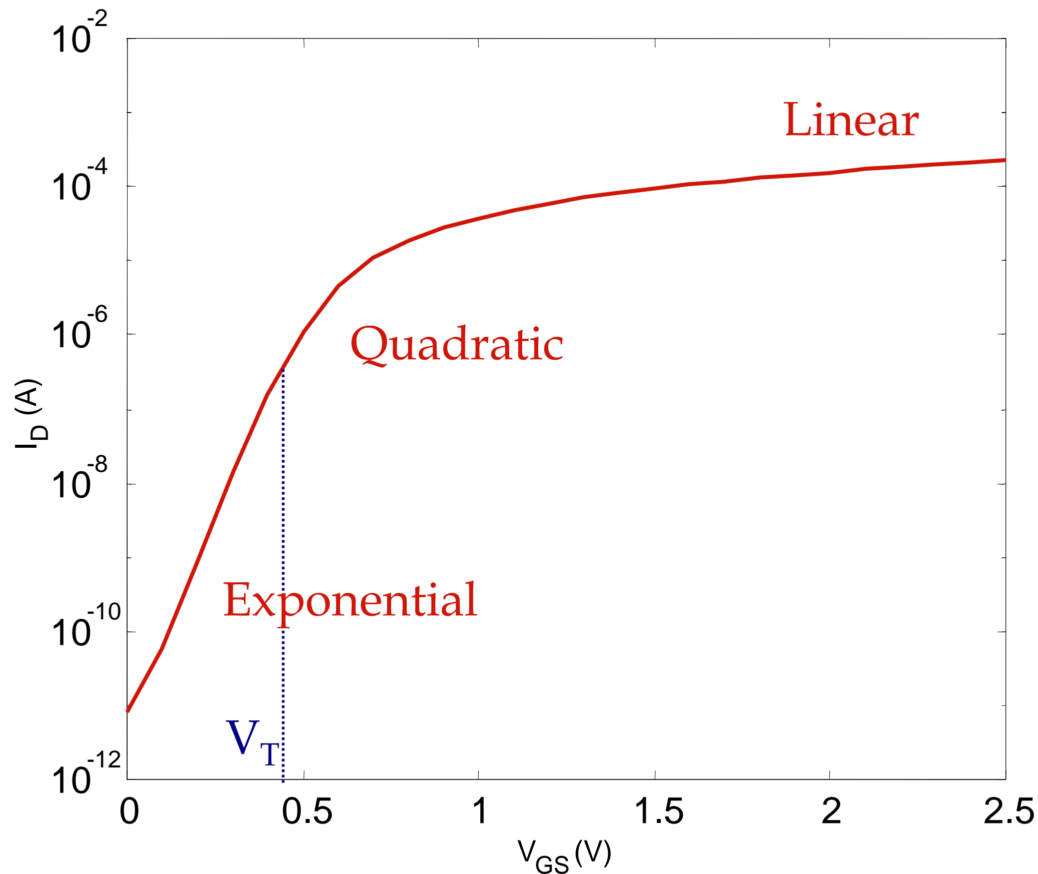
Sub-Threshold Conduction

$$\frac{10I_{sub}}{I_{sub}} = \frac{I_s e^{\frac{q(V_{GS1}-V_T-V_{offset})}{nkT}}(1-e^{\frac{-qV_{DS}}{kT}})}{I_s e^{\frac{q(V_{GS2}-V_T-V_{offset})}{nkT}}(1-e^{\frac{-qV_{DS}}{kT}})}$$

$$\therefore 10 = \frac{e^{\frac{q(V_{GS1}-V_T-V_{offset})}{nkT}}}{e^{\frac{q(V_{GS2}-V_T-V_{offset})}{nkT}}} = e^{\frac{q(V_{GS1}-V_{GS2})}{nkT}}$$

$$S = \Delta V_{GS} = \frac{nkT}{q}\ln(10)$$

Sub-Threshold Conduction



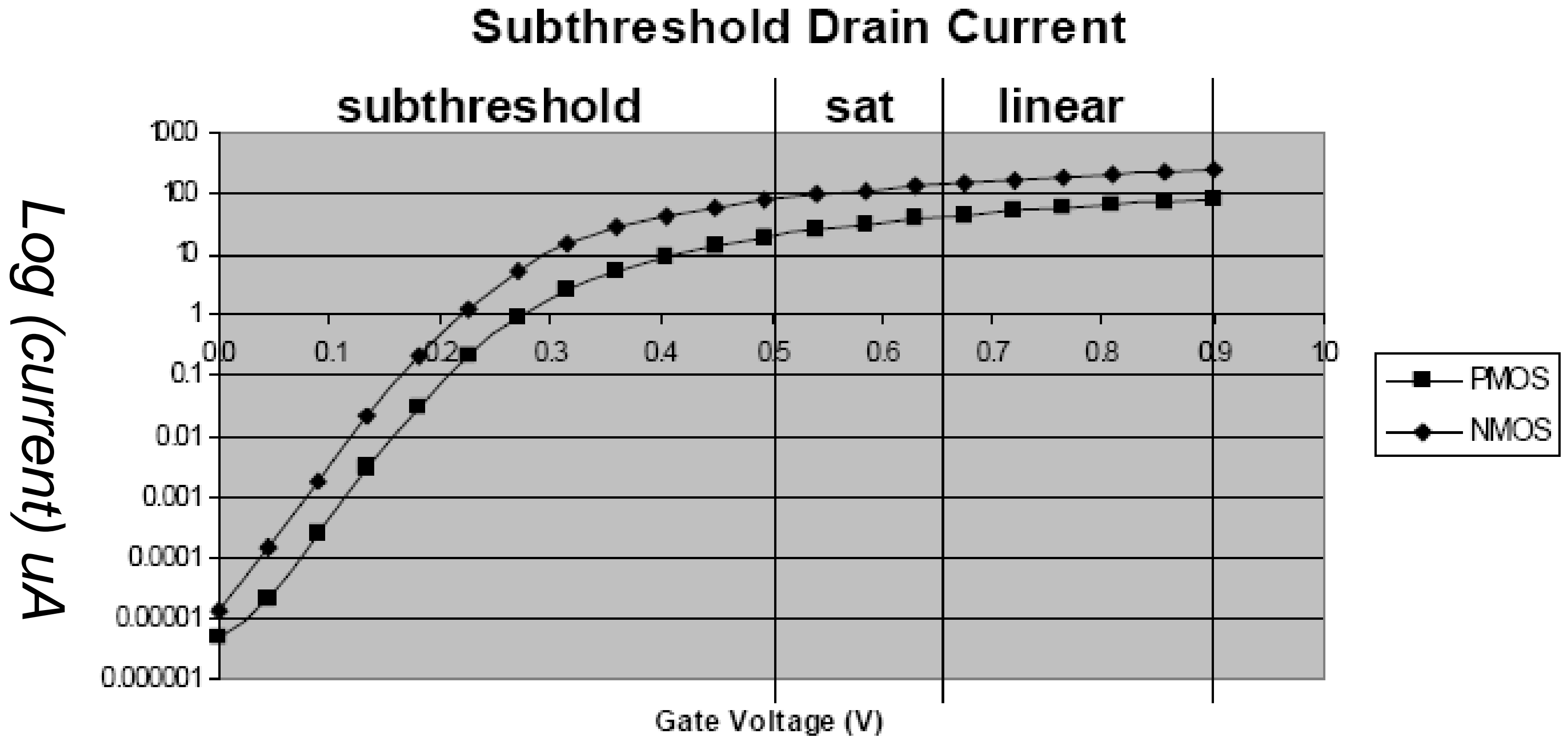
The Slope Factor

S is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

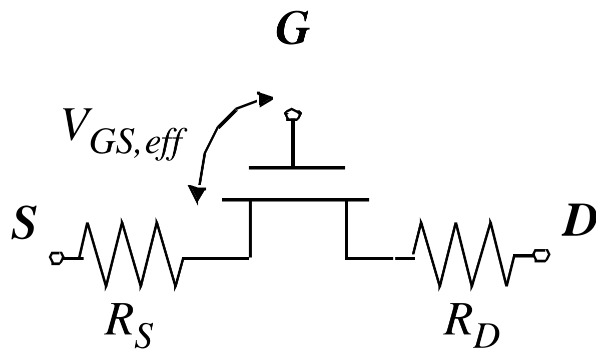
Sub-Threshold Conduction

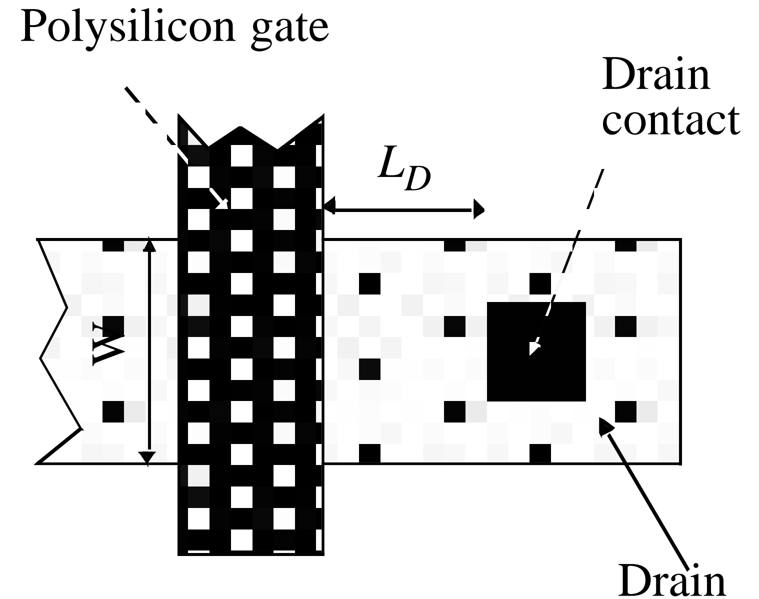


Summary of MOSFET Operating Regions

- Strong Inversion $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
  - Exponential in V_{GS} with linear V_{DS} dependence

Parasitic Resistances





Shallower junctions and smaller contact openings