EE 466/586
VLSI Design

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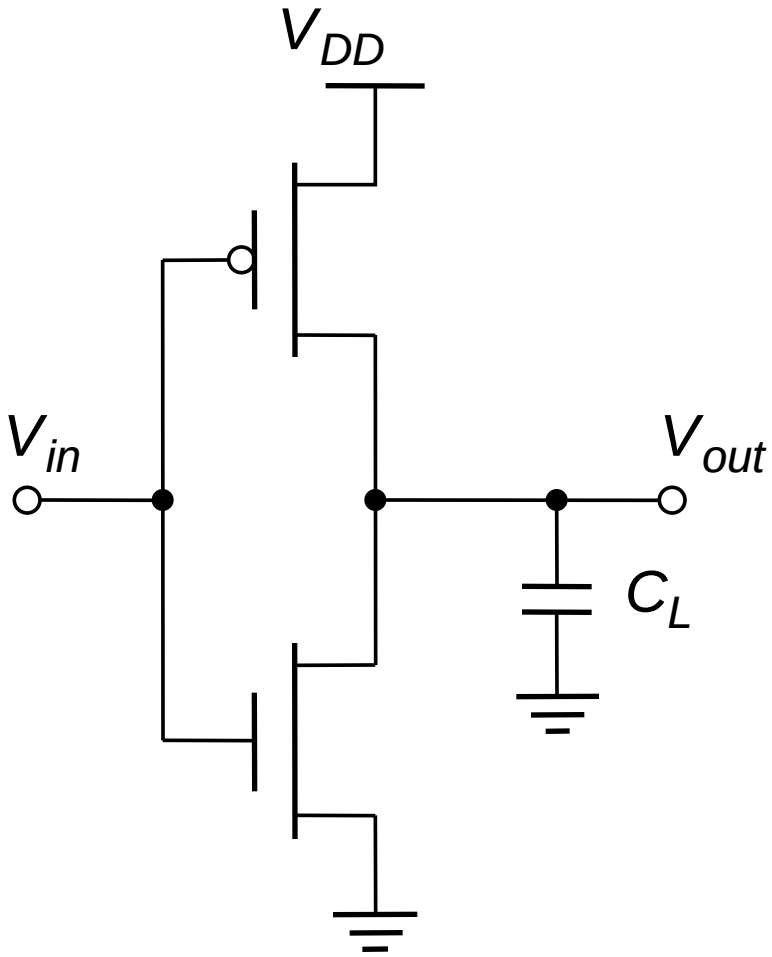
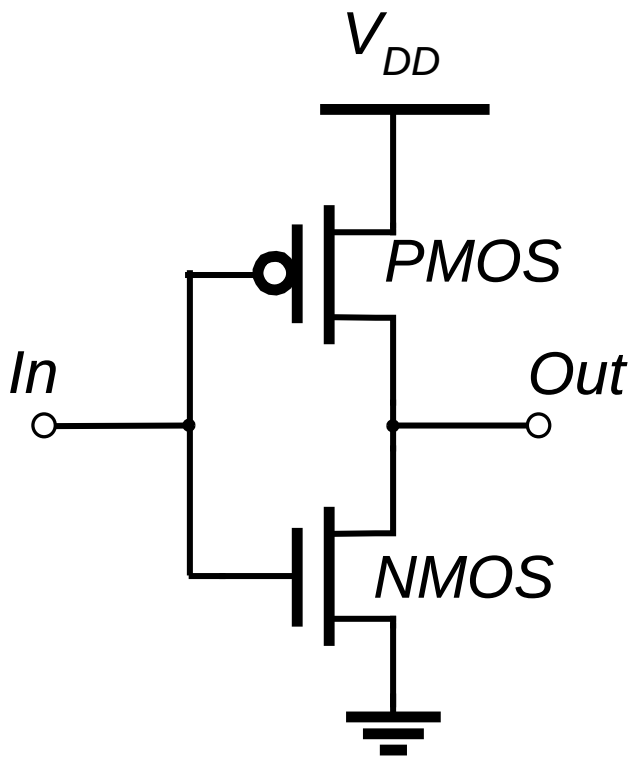
Lecture 6

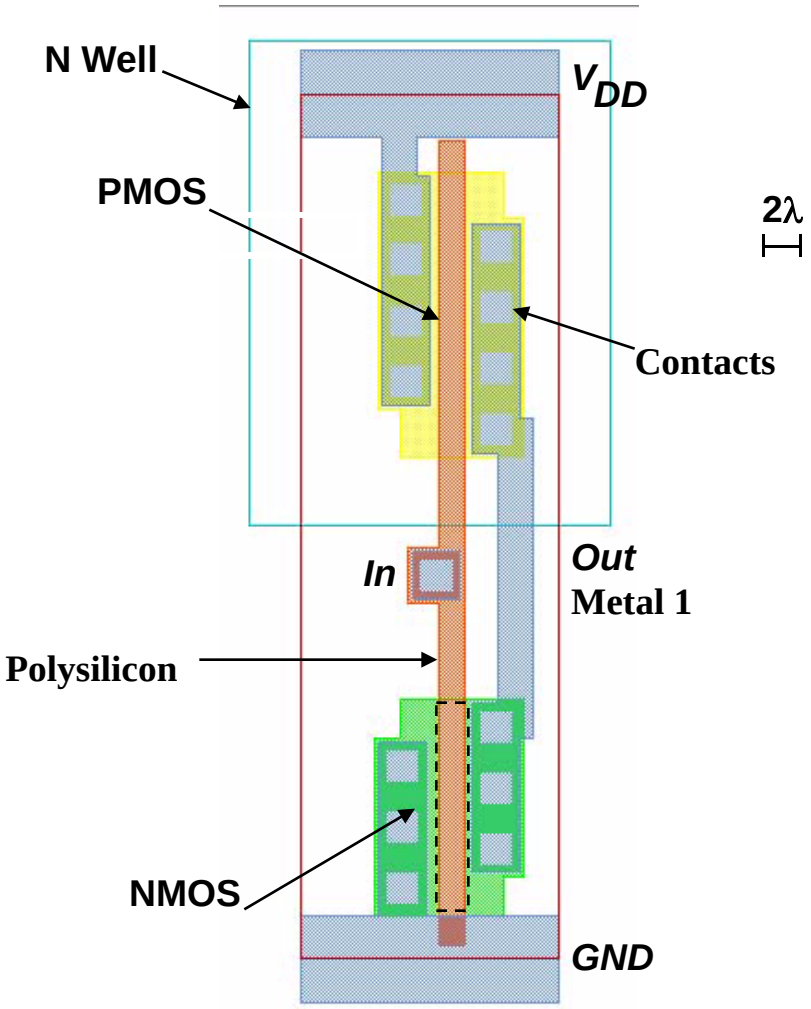
MOS Inverter Circuits

The CMOS Inverter: A First Glance



CMOS Inverter

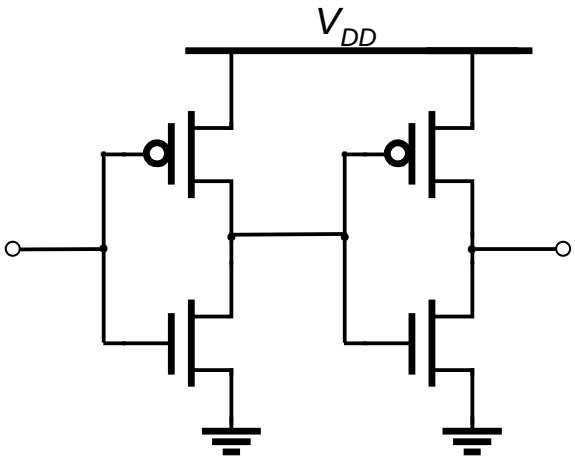


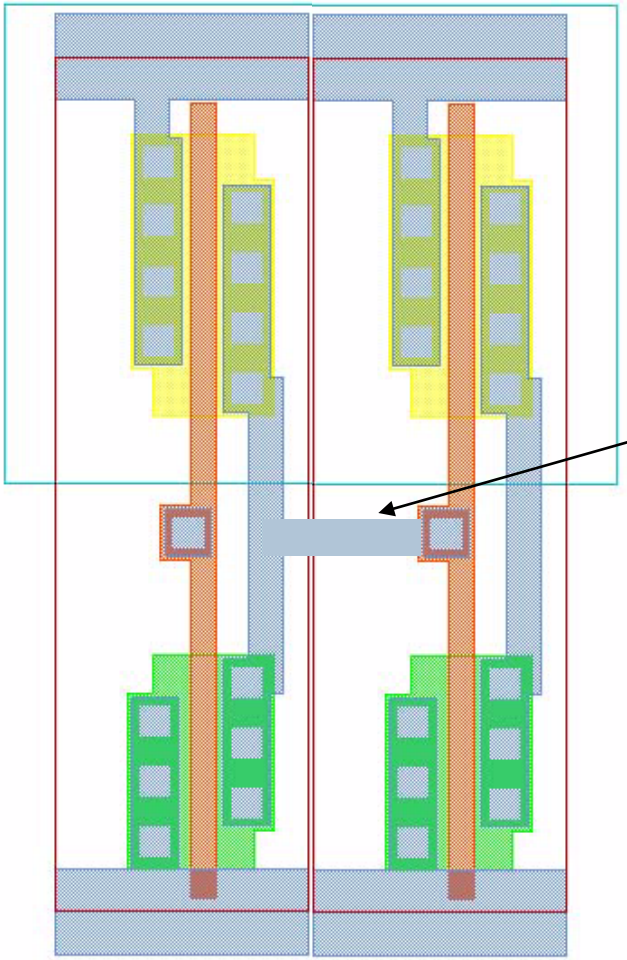


Two Inverters

Share power and ground

Abut cells



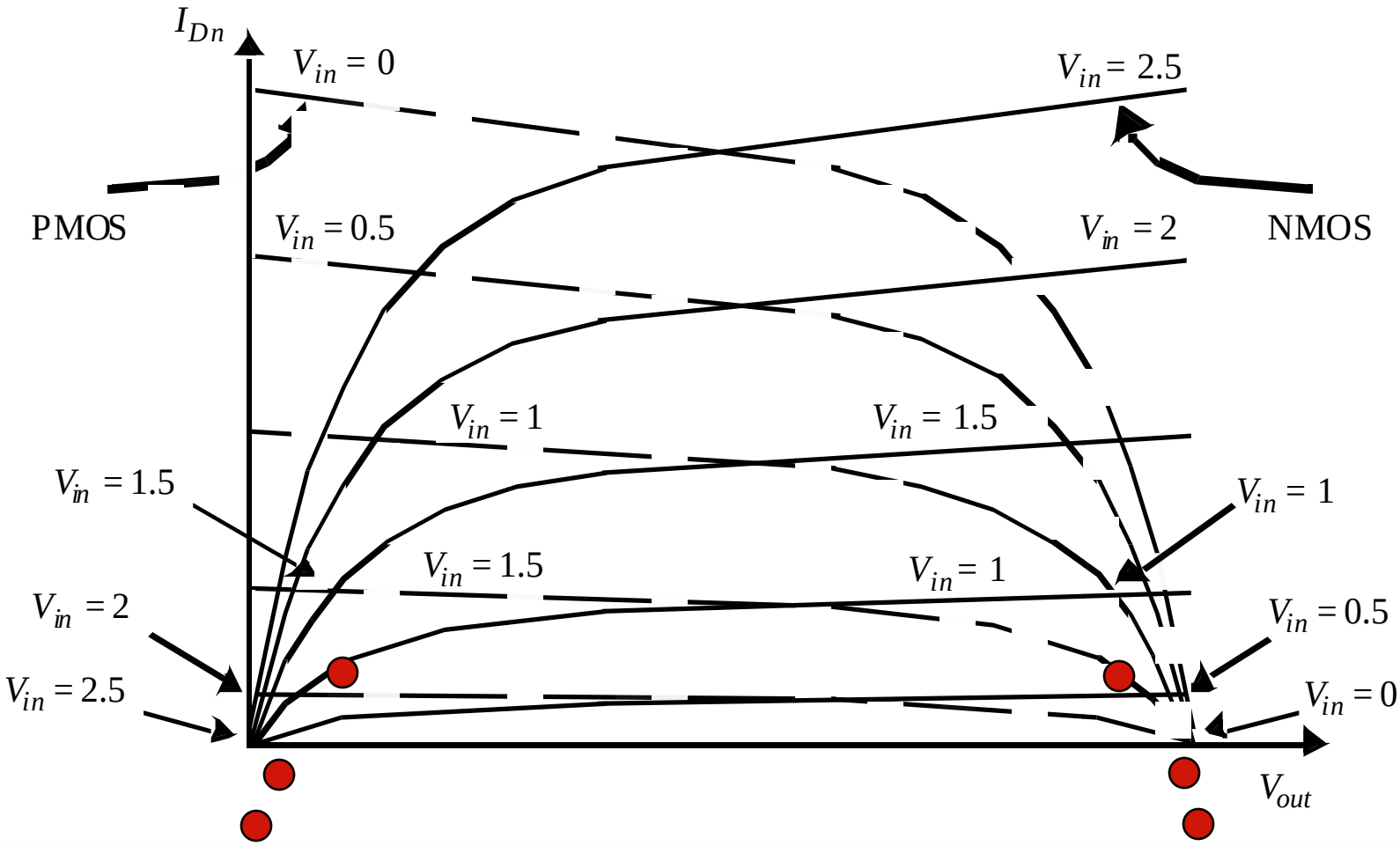


Connect in Metal

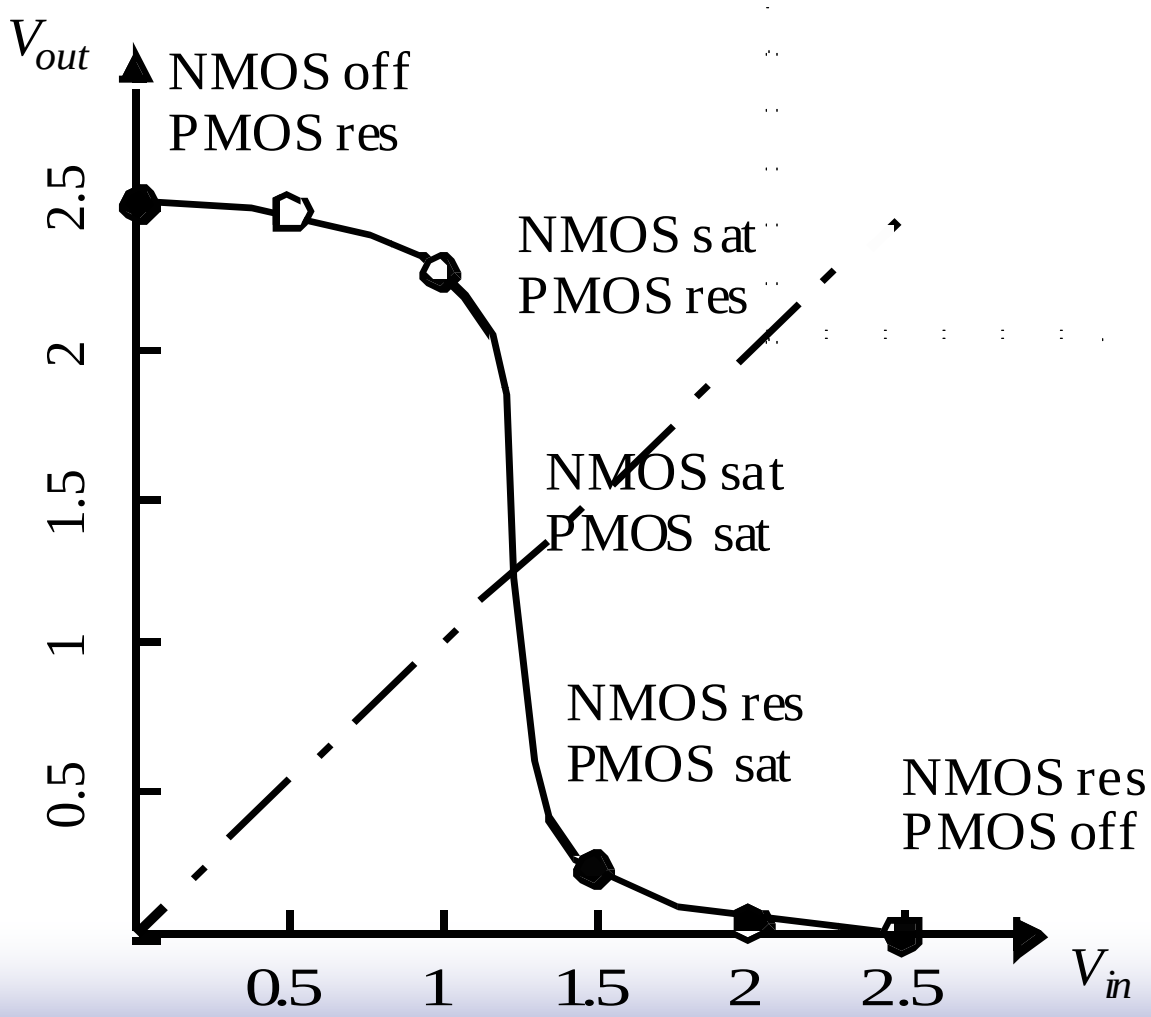
Principle of Operation

- *When the input is at V_{DD}, the NMOS device is conducting while the PMOS device (which has V_{GS}=0 V) is cut off*
- *V_{out} is approximately 0 V*
- *When the input is at ground, the NMOS device is cut off while the PMOS device is conducting. Only the small leakage current of the NMOS can flow, so V_{out} is very close to V_{DD}*
  - *$V_{OH} = V_{DD}$ and V_{OL}=0 v*
  - *Large noise margin*

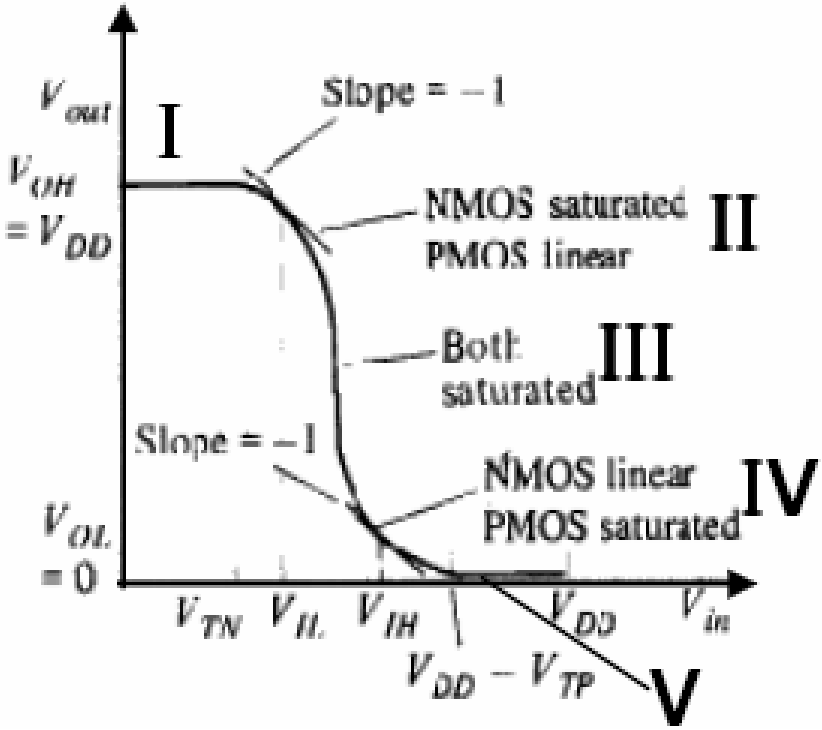
CMOS Inverter Load Characteristics

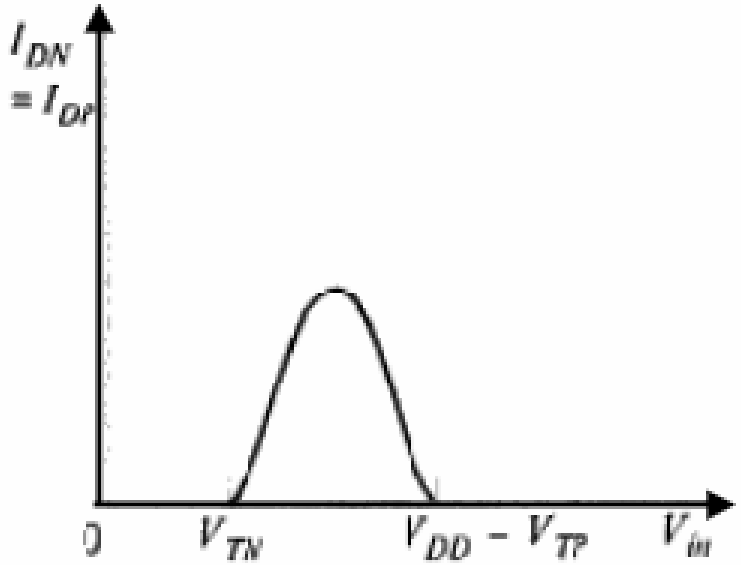


CMOS Inverter VTC



CMOS Inverter Characteristics





Region I: n-off, p-lin

- The NMOS device is off while the PMOS device is linear.
- The output remains at $V_{OH} = V_{DD}$ up to the point when $V_{in} = V_{TN}$

Region II: n-sat, p-lin

- The NMOS device is on and in saturation, while the PMOS device is still in the linear region since its V_{DS} is relatively small.
- I_{DN} (*sat*)=I_{DP}(*lin*)
- Obtain V_{IL} from here
- Follow board notes

Region III: n-sat, p-sat

- This involves the nearly vertical segment of the VTC where both transistors are saturated.
- Follow board notes
- Skewed Inverter

Region IV: n-lin, p-sat

- The NMOS device is on and in the linear region since V_{DS} is small
- PMOS device is still in saturation
- Determine V_{IH}
- Follow board notes

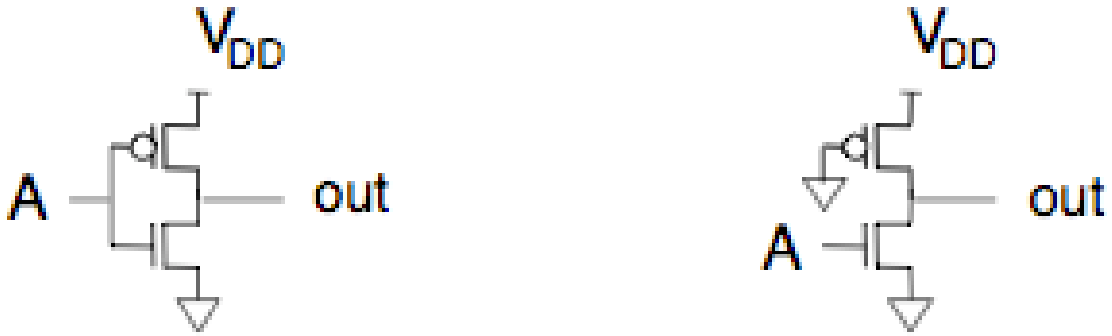
Region V: n-lin, p-off

- The applied input voltage is above V_{DD}-$|V_{TP}|$, so the output is now 0 V and will remain that way up to and beyond V_{in}=V_{DD}.

Pseudo-NMOS Inverter

- The saturated-enhancement NMOS load inverter suffers from a lower V_{OH} than the other configurations.
- The “linear”-enhancement NMOS load inverter requires two voltage supplies to produce $V_{OH}=V_{DD}$.
- One Advantage
  - when designing multi-input gates, we only require one load regardless of the number of inputs.
  - Because of the *push-pull arrangement in standard CMOS, it needs roughly twice as many transistors to implement multi - input gates.*

Pseudo-NMOS Inverter (Cont'd)



- The gate of the PMOS device is connected to ground so that the transistor is always on.
- This device is able to pull the output to VDD when the NMOS device is off without the need for additional supplies.
- However, it will fight the NMOS transistor when it is on.
- it must be sized along with the NMOS device to deliver the desired V_{OL}
- Ratioed Structure
- When the output is low, power is dissipated in the pseudo-NMOS inverter

VTC of Pseudo-NMOS

- $V_{OH} = V_{DD}$
- For V_{OL}
  - I_P(Sat) = I_N *(Lin)*
  - *Follow board notes*

Sizing of Inverters

- Selecting W/L ratio of the pull-up and pull-down devices
- Follow board notes