EE 466/586
VLSI Design

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Lecture 8

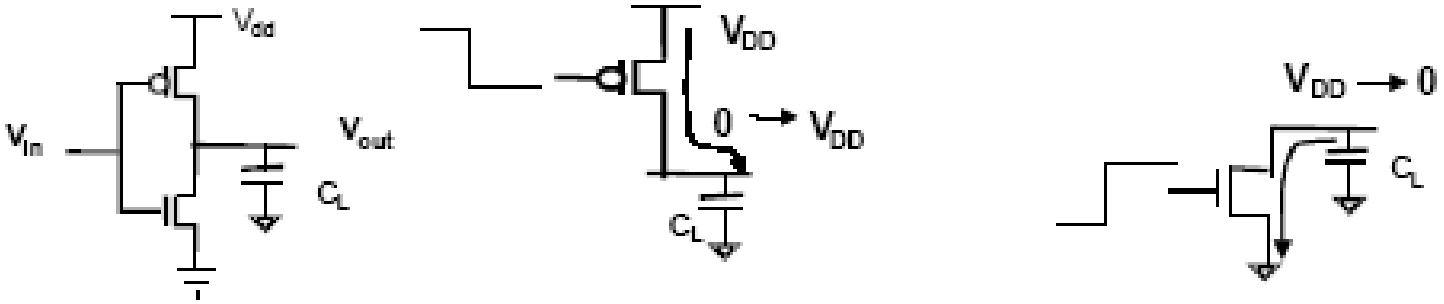
Power Dissipation in CMOS Gates

Power in CMOS gates

- Dynamic Power
  - Capacitance switching
  - Crowbar current flowing from V_{dd} to GND during switching
  - Power due to glitches at the output
- Static Power
  - Leakage current (subthreshold current and source/drain junction reverse-bias current)
  - DC standby current (Pseudo NMOS with low output)

Dynamic Power consumption

- Dynamic power consumption comes from switching behavior
  - Follow board notes

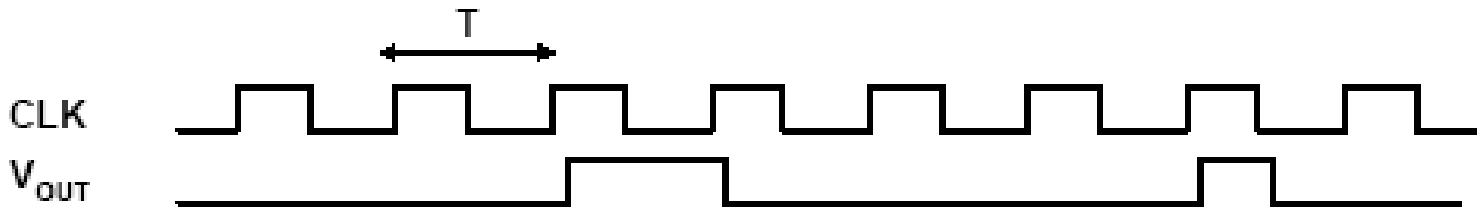


Dynamic Power consumption

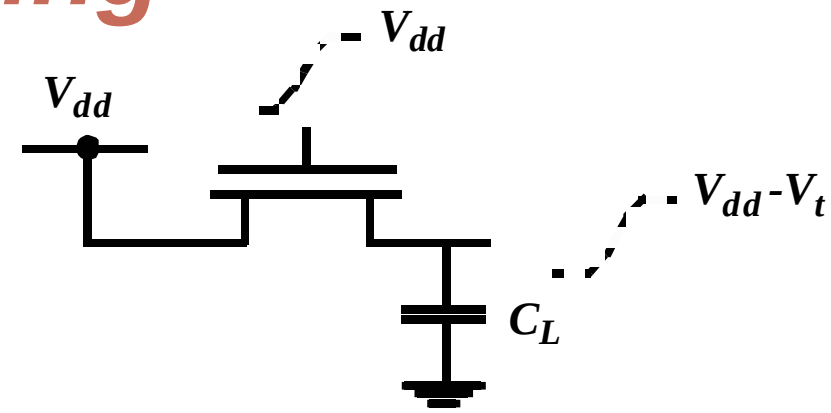
- Most of the chip power today is due to the charging and discharging of capacitances in the circuit as a result of logic switching events
- When switching events occur, the supply current acts to charge the output load capacitance on one part of the cycle, and current flowing to Gnd discharges the capacitance on the other half of the cycle
- Effectively, we have current flowing from V_{DD} to Gnd (albeit on different parts of the cycle) and this leads to power dissipation
- The frequency of switching, *f*, determines the actual power that is consumed.

Dynamic Power consumption

- A single cycle requires one charge and one discharge of capacitor: $E = C_L(V_{DD} - V_{SS})^2$.
- Clock frequency f = 1/t.
- Energy $E = C_L(V_{DD} - V_{SS})^2$.
- Power = E x f = f $C_L(V_{DD} - V_{SS})^2$.



Modification for Circuits with Reduced Swing



$$E_{0 \rightarrow 1} = C_L \bullet V_{dd} \bullet (V_{dd} - V_t)$$

- Can exploit reduced swing to lower power (e.g., reduced bit-line swing in memory)

Switching Activity

- The clock switches every cycle
- If we refer to a transition from high-to-low or low-to-high as a *toggle*, then it follows that we need two toggles to have power dissipation
- Most logic gates do not switch on every cycle
- The average frequency of operation can be specified using an activity factor that is multiplied by the clock frequency f . The power equation can be modified to include

Node Transition Activity and Power

- Consider switching a CMOS gate for *N* clock cycles

$$E_N = C_L \bullet V_{dd}^2 \bullet n(N)$$

E_N : the energy consumed for *N* clock cycles

$n(N)$: the number of 0->1 transition in *N* clock cycles

$$P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \bullet f_{clk} = \left(\lim_{N \to \infty} \frac{n(N)}{N} \right) \bullet C_L \bullet V_{dd}^2 \bullet f_{clk}$$

$$\alpha_{0 \to 1} = \lim_{N \to \infty} \frac{n(N)}{N}$$

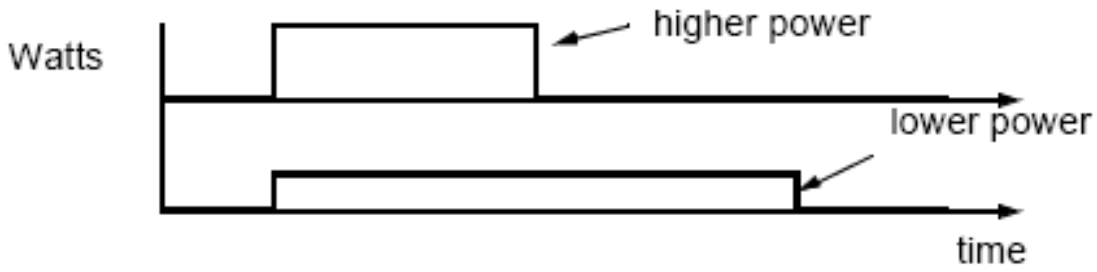
$$P_{avg} = \alpha_{0 \to 1} \bullet C_L \bullet V_{dd}^2 \bullet f_{clk}$$

Transition Probability

- Follow board notes

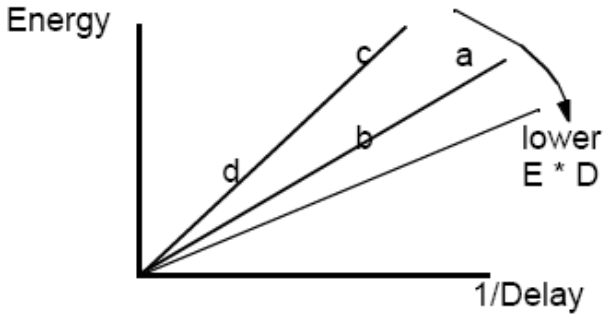
Observations on power consumption

- Resistance of pullup/pulldown drops out of energy calculation.
- Power consumption depends on operating frequency.
  - Slower-running circuits use less power (but not less energy to perform the same computation).

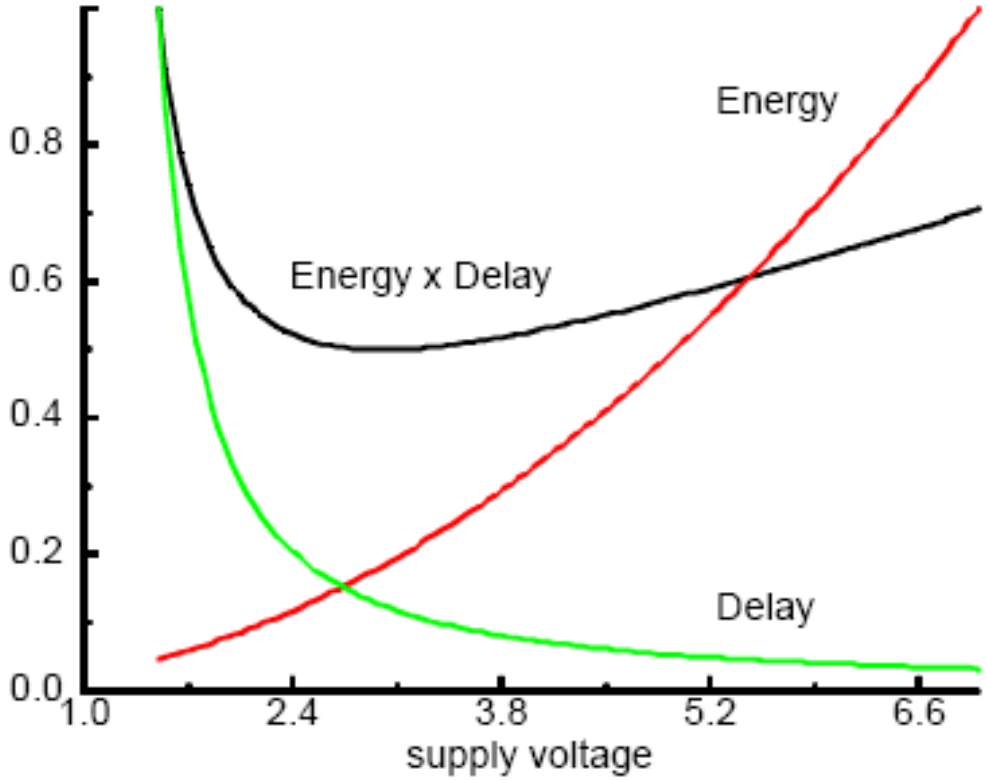


Power delay product

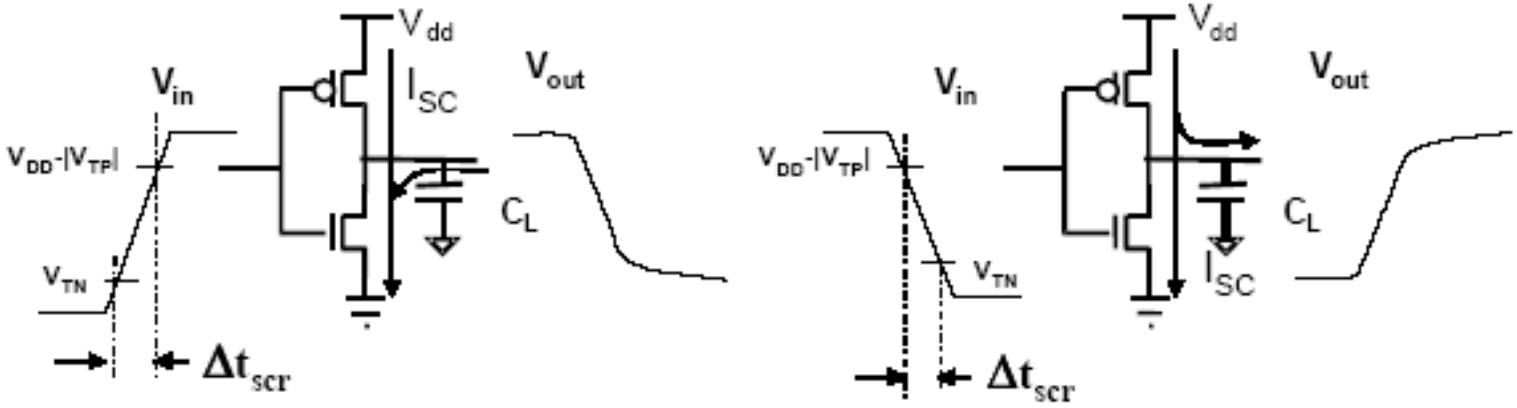
- Also known as power-delay product.
- Helps measure quality of a logic family.
- For static CMOS:
  - $SP = P/f = CV^2$.
- Static CMOS speed-power product is independent of operating frequency.
  - Voltage scaling depends on this fact.
  - Considers only dynamic power.



Energy vs. Delay



Switching Current

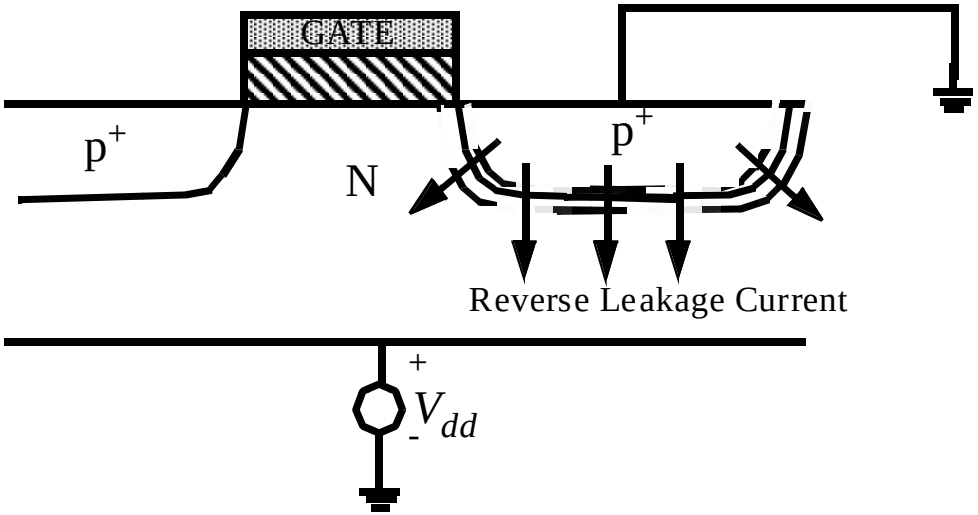


- ***Crowbar current is the current that flows directly from VDD to Gnd during switching events.***
- ***The reason why short-circuit flows is that both transistors are on simultaneously; that is, |VGS| > |VT| for both devices.***
- ***If we apply a step input, only one device would be on at any given point in time, and we would not observe any short circuit current. However, since all inputs have a finite slope, both devices are on when VTN < Vin < VDD – |VTP|.***

Static Power

- Subthreshold leakage
  - Close proximity of the source and drain
  - This results in a bipolar transistor action, where the substrate is the base of the bipolar transistor, while the source and drain act as the emitter and collector, respectively
  - Subthreshold current is due to diffusion current of minority carriers across the channel region
- reverse-bias source and drain junctions

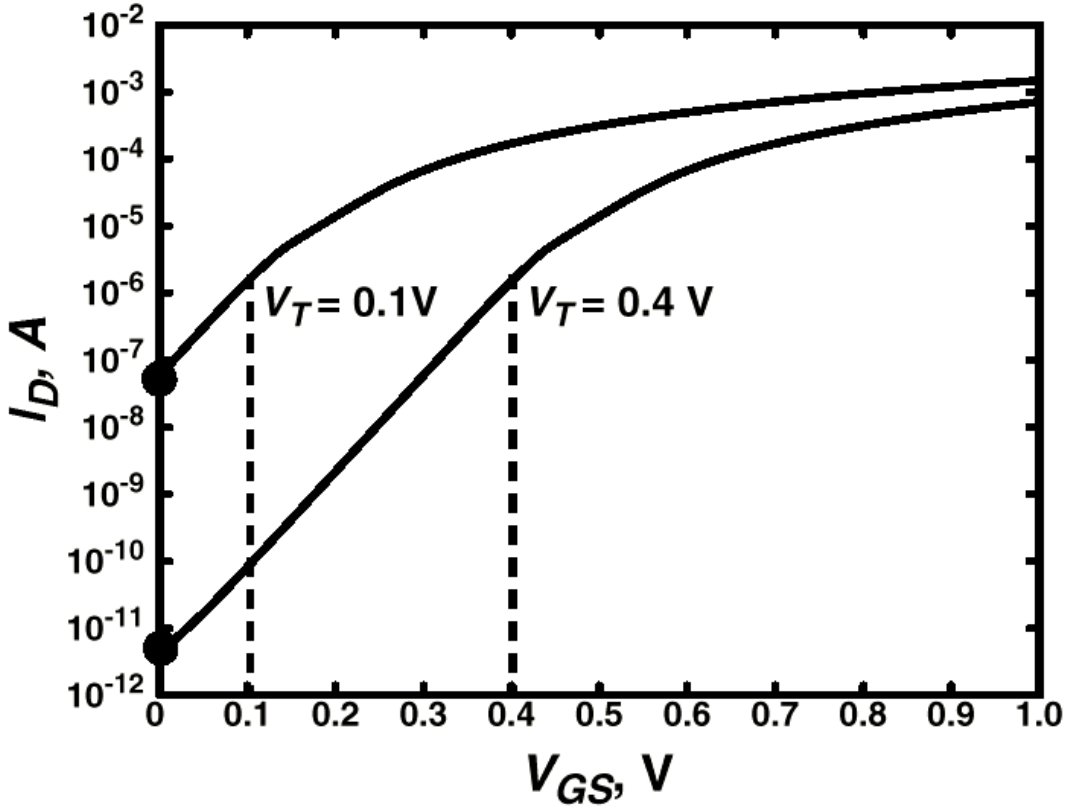
Reverse-Biased Diode Leakage

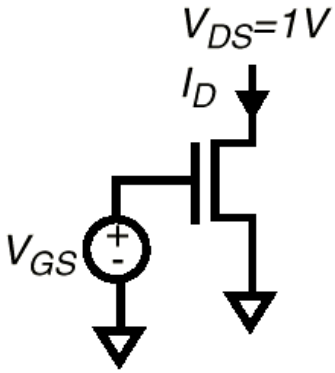


$$I_{DL} = J_S \times A$$

***JS* = 10-100 pA/μm2 at 25 deg C for 0.25μm CMOS**
***JS* doubles for every 9 deg C!**

Subthreshold Leakage Component





- Leakage control is critical for low-voltage operation

Principles for Power Reduction

- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 … 0.9 V by 2010!)
- Reduce switching activity
- Reduce physical capacitance

Power in CMOS Gates

$$P_{total} = \underbrace{\alpha C\, Vdd\, \Delta V f_{clk}}_{\text{Dynamic}} + \underbrace{Vdd \cdot I_{short\text{-}circuit}}_{\text{Short-circuit}} + \underbrace{Vdd \cdot I_{leakage}}_{\text{Leakage}}$$

- Power in an inverter is governed by the 3 part equation above
  - Dynamic CV^2f (switching) power
    - Currently the largest part, but percentage getting smaller
  - Leakage Power
    - Subthreshold conduction – getting bigger due to aggressive scaling, temperature, etc.
    - Reverse leakage of diodes (relatively small)
    - Possible gate tunneling current in future technologies
  - Short-circuit (crowbar) current
    - Both pull-up and pull-down devices are partially conducting for a small, but finite amount of time
    - Can be modeled as some fraction of dynamic current

Intel Pentium-II Power Distribution