EE 466/586
VLSI Design

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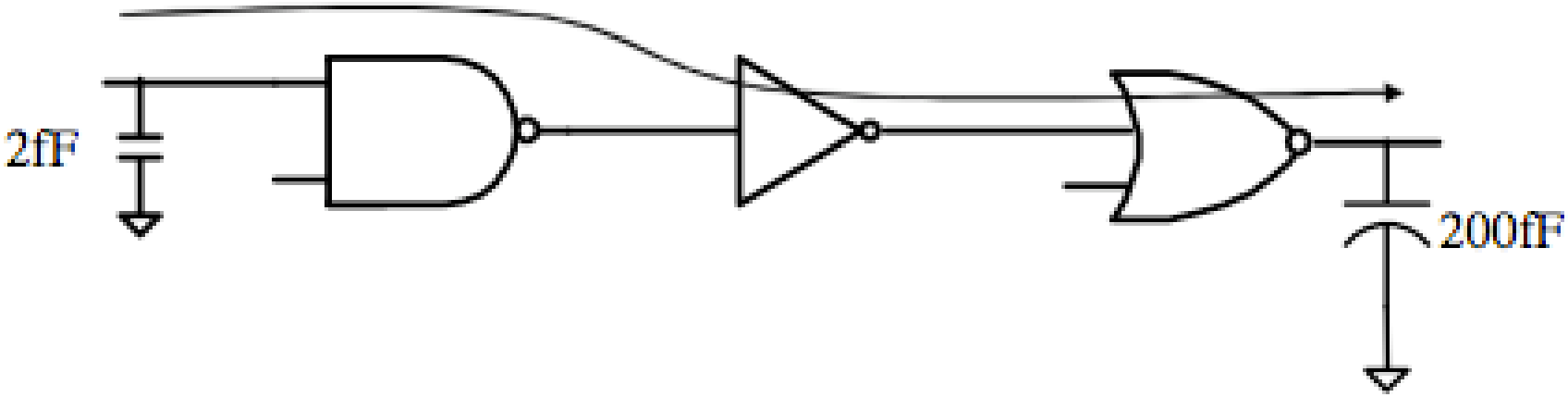
Lecture 12

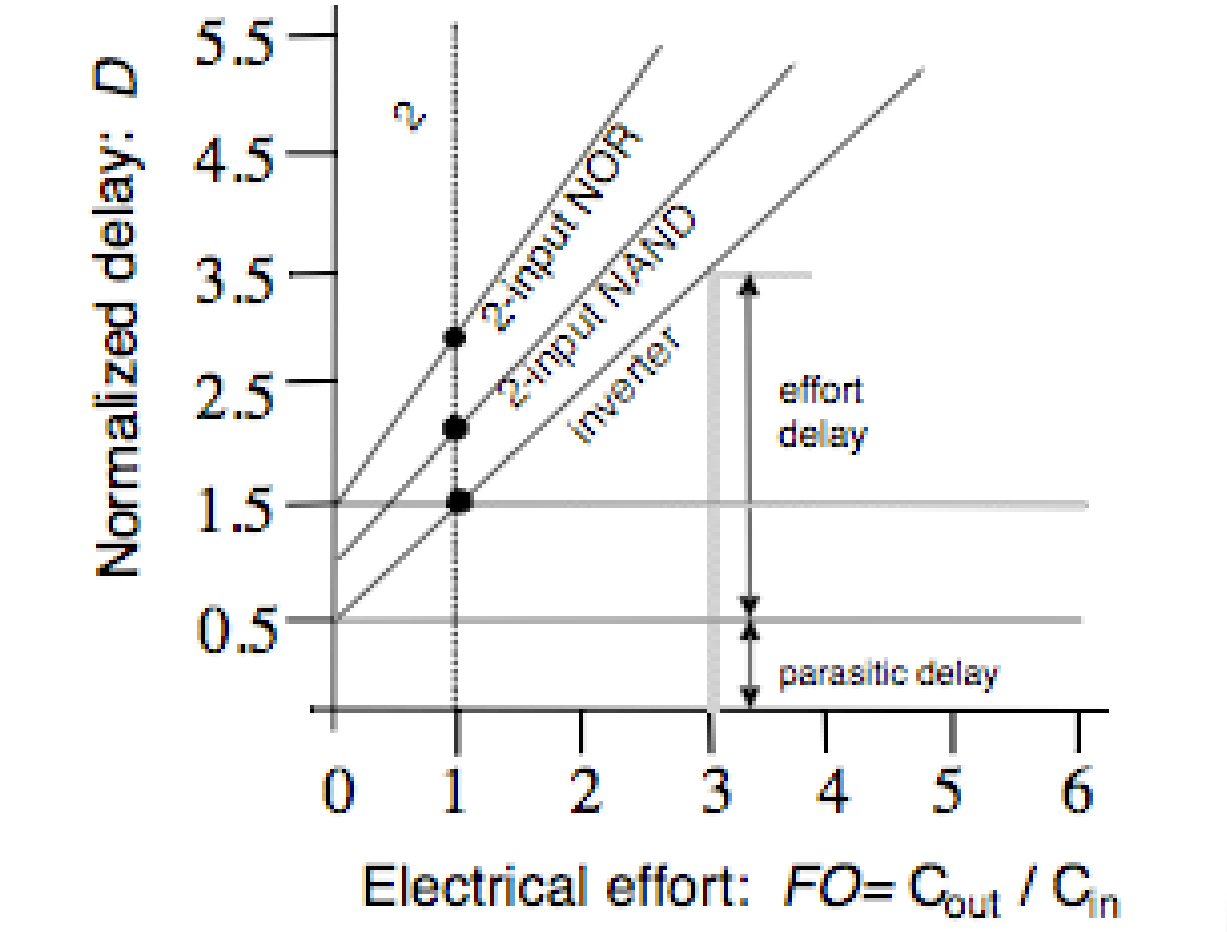
Logical Effort (Cont'd)

Path Optimization using LE

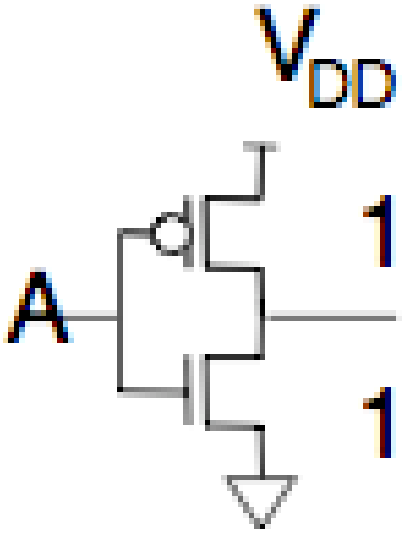


- *Introduce the concept of **stage effort***

Practical Interpretation

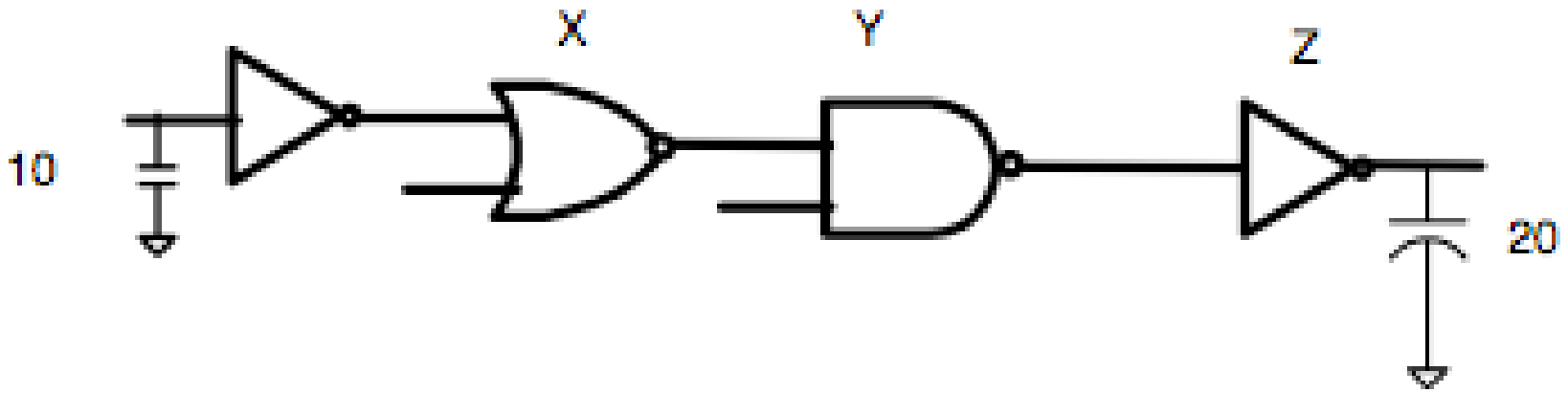


LE for a skewed inverter



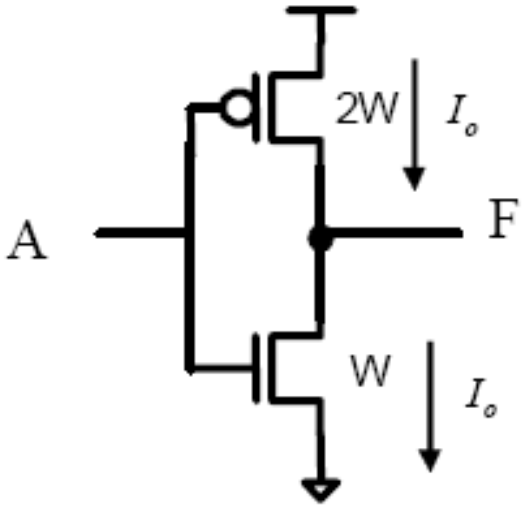
- *Follow board notes*
- *LE will be different for rising and falling cases*

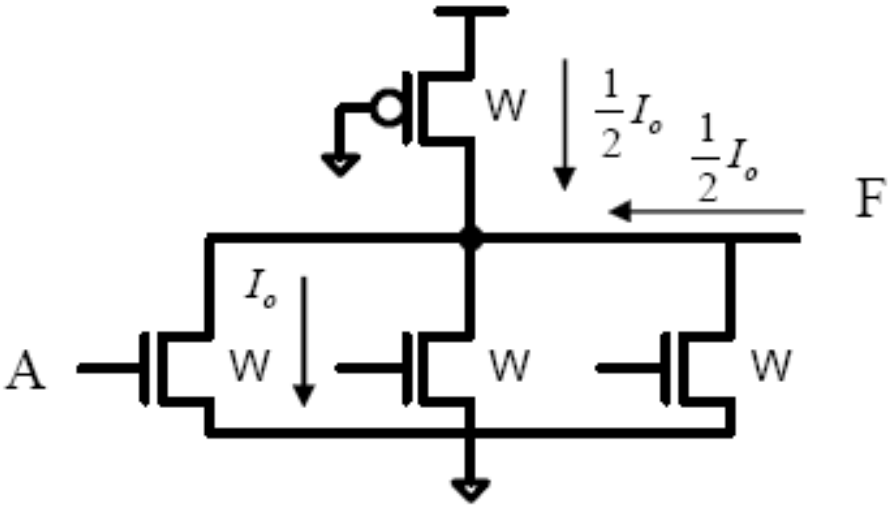
Path Optimization using LE



- *Follow board notes*

LE of Pseudo-NMOS gates

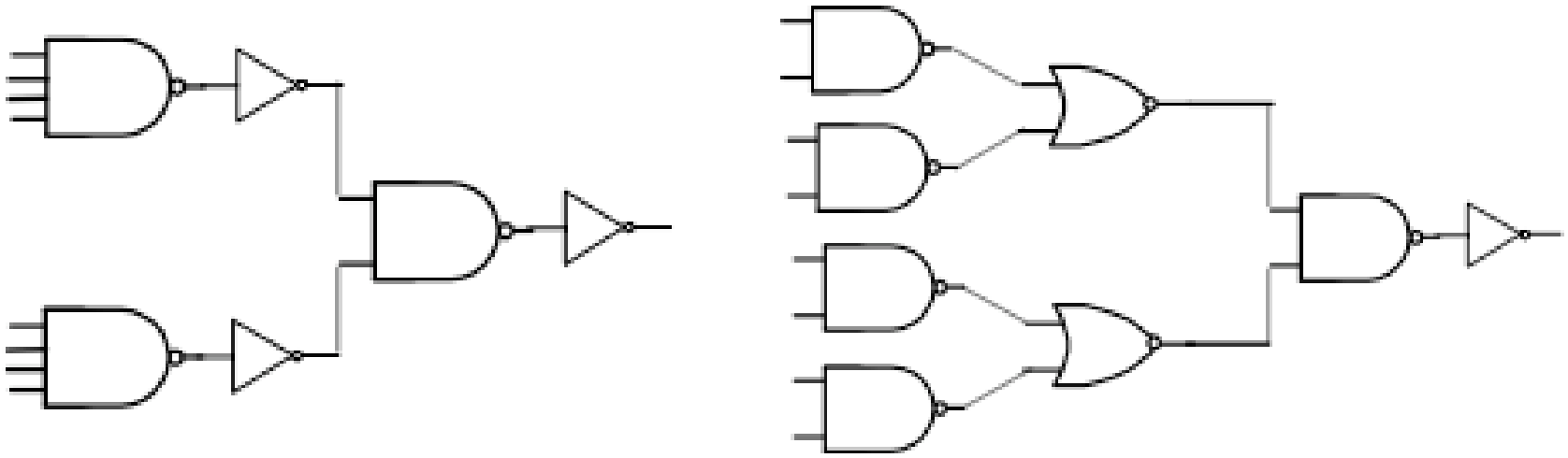




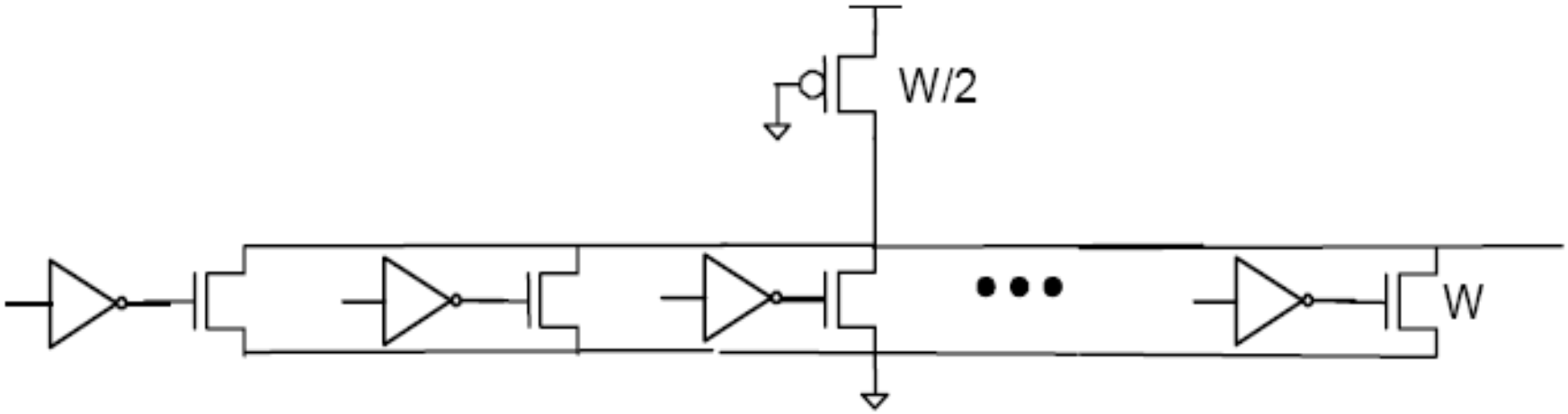
$$LE = \frac{(C_{in} \times delay)_{gate}}{(C_{in} \times delay)_{inv}} = \frac{(C_{in} \times \Delta t)_{gate}}{(C_{in} \times \Delta t)_{inv}} = \frac{(C_{in} \times C_{out} \Delta V / I)_{gate}}{(C_{in} \times C_{out} \Delta V / I)_{inv}}$$

High fan-in gates

- An 8-input AND gate is to be designed to drive a load of 200 fF, with an input capacitance of 20 fF



Pseudo-NMOS Implementation

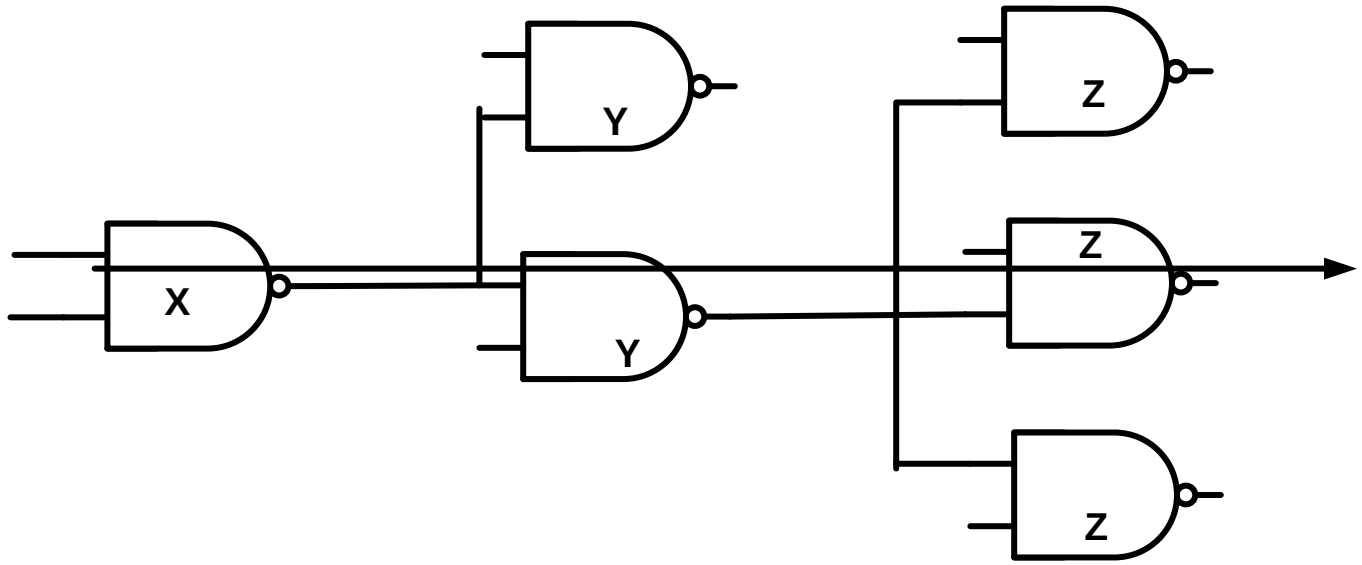


- *Which one is faster?*

Note: The LE of the gates in a logic path, by themselves, do not tell us which configuration is faster. A delay calculation must be performed to make the determination.

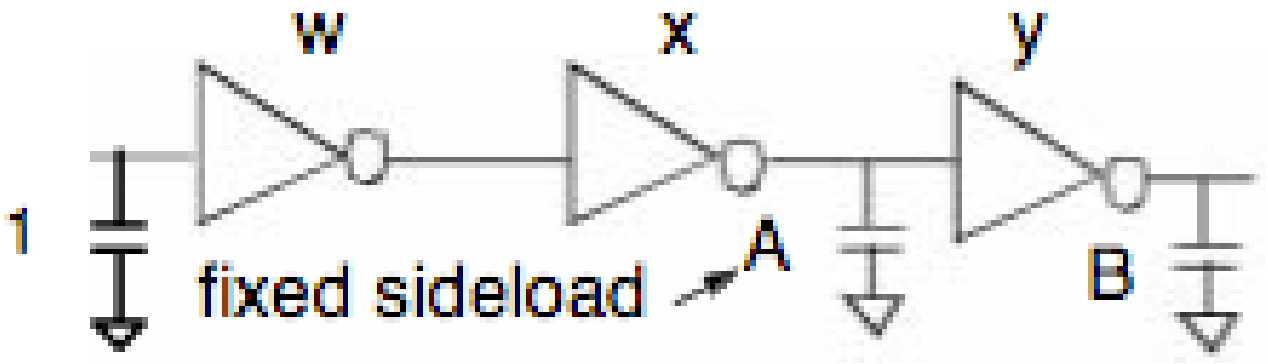
Branching Effort

- *Suppose there are one or more branches from a given node*



$$total\_path\_effort = \prod LE \times BE \times FO = (\prod LE \times BE) \times \frac{C_{load}}{C_{in}}$$

Side loads



- *First solve without the side loads*
- *Add side load. Remove gates beyond side load but including their loading effects. Solve sub problem.*
- *Combine two solutions.*

Side loads