EE 466/586
VLSI Design

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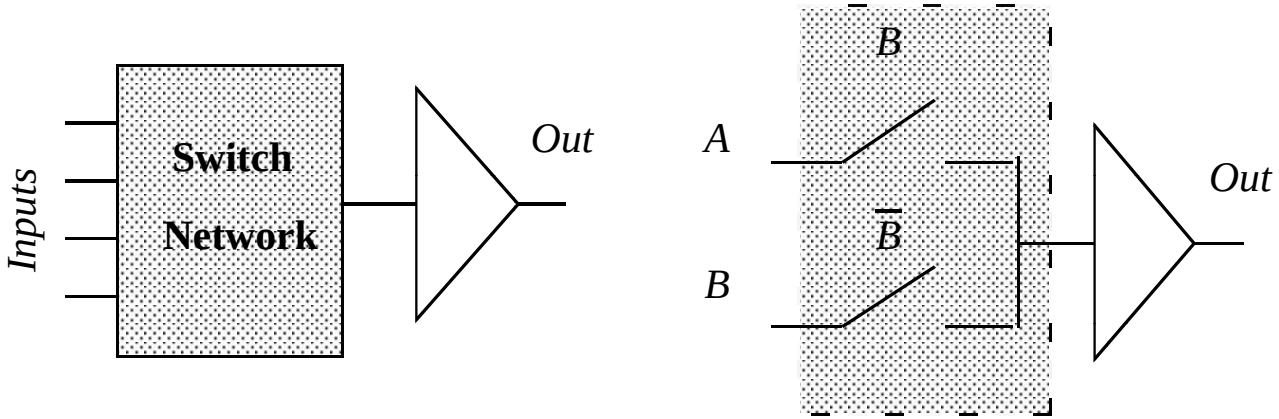
Lecture 14

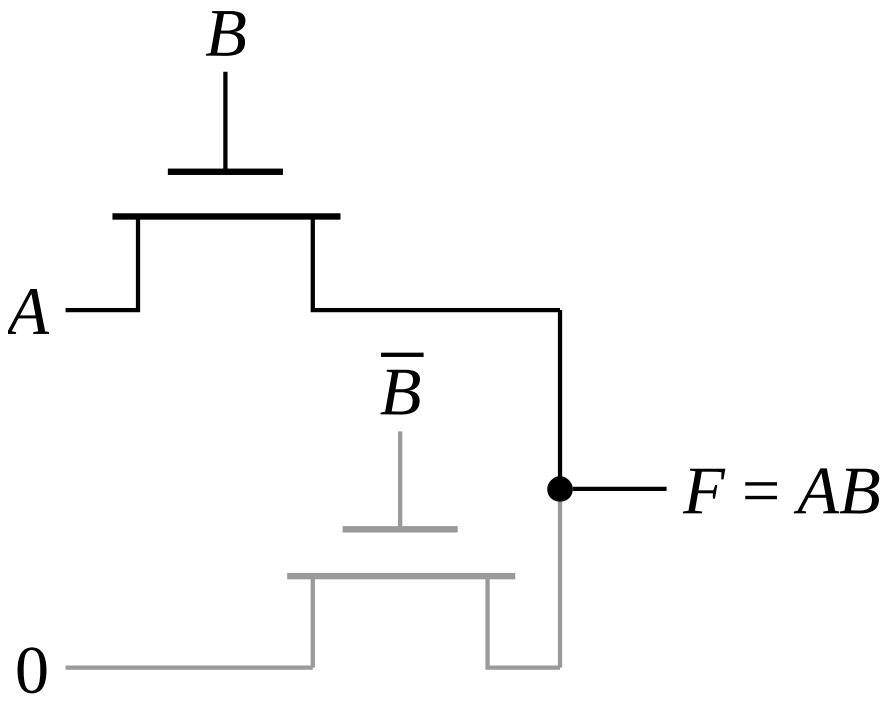
Pass Transistor Logic

Pass Transistor Logic

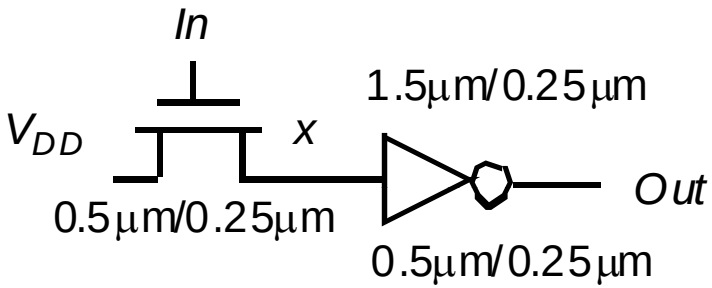


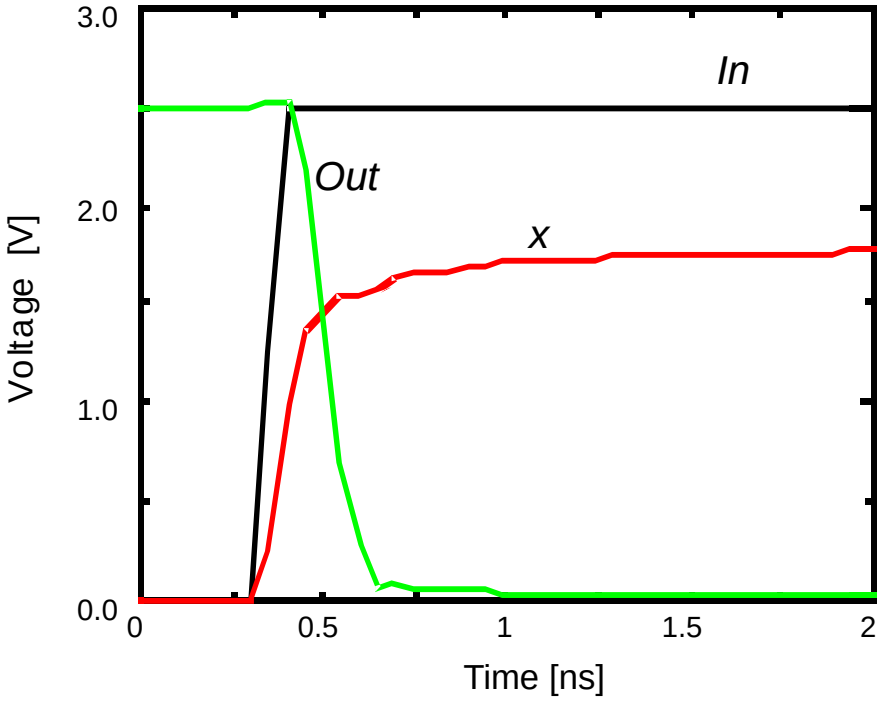
- **N transistors**
- **No static consumption**

Example: AND Gate



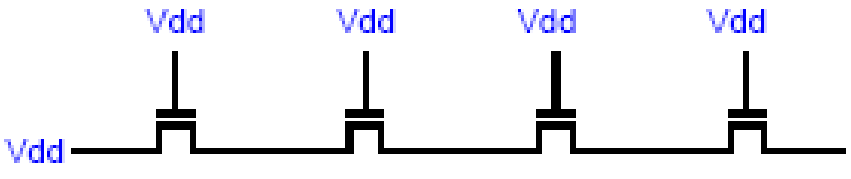
NMOS-Only Logic

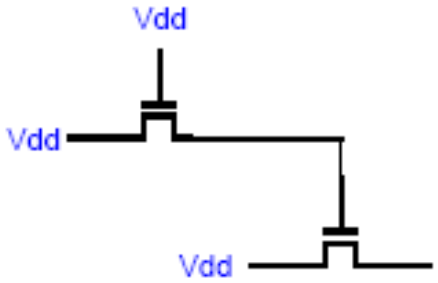




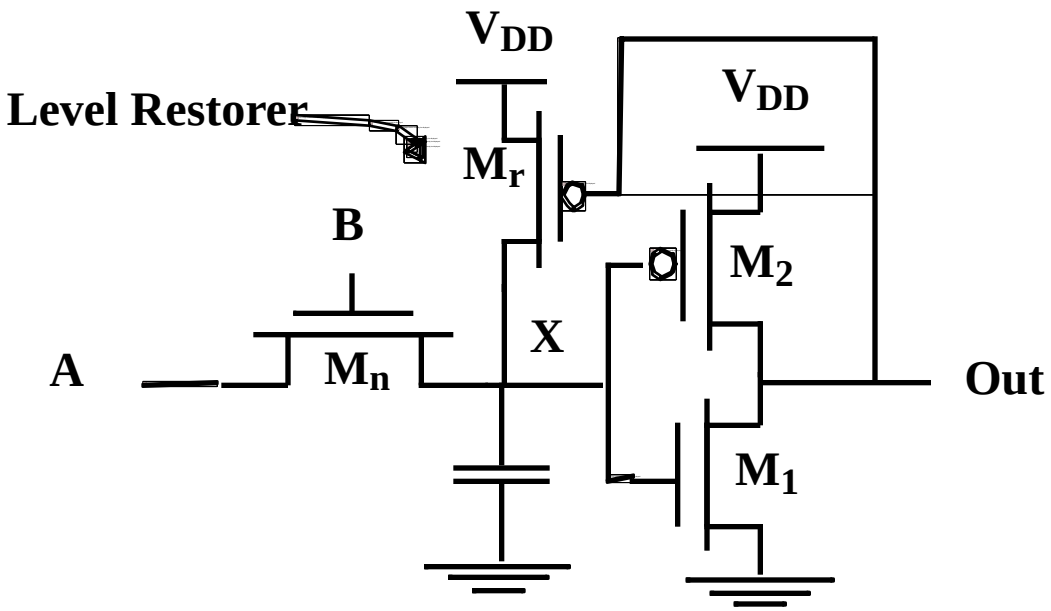
Issues with Pass Transistor Logic

- Threshold drop
- Capacitive feed through
- Charge sharing
- Follow board notes



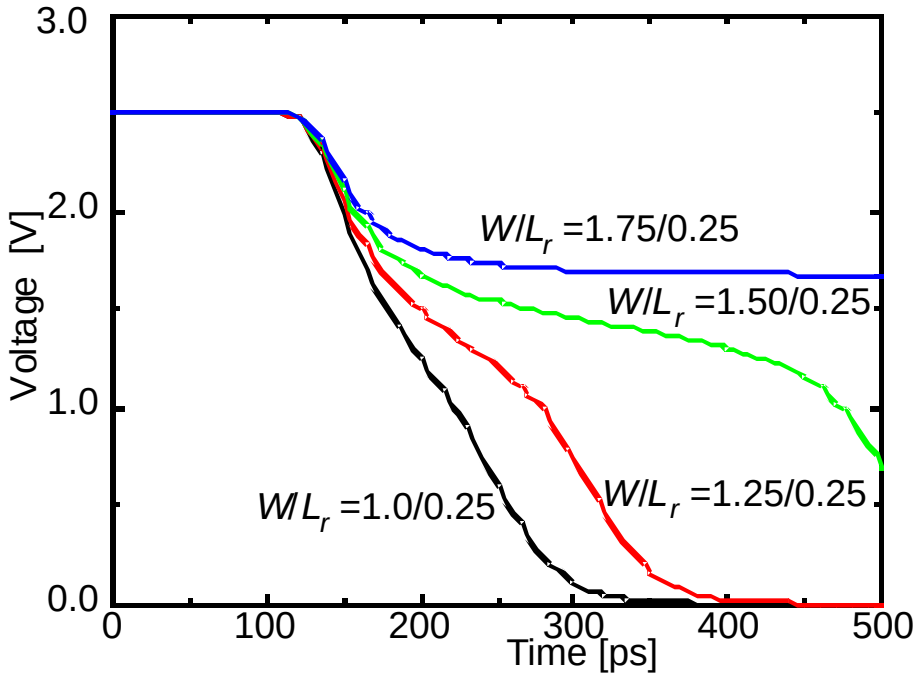


NMOS Only Logic: Level Restorer



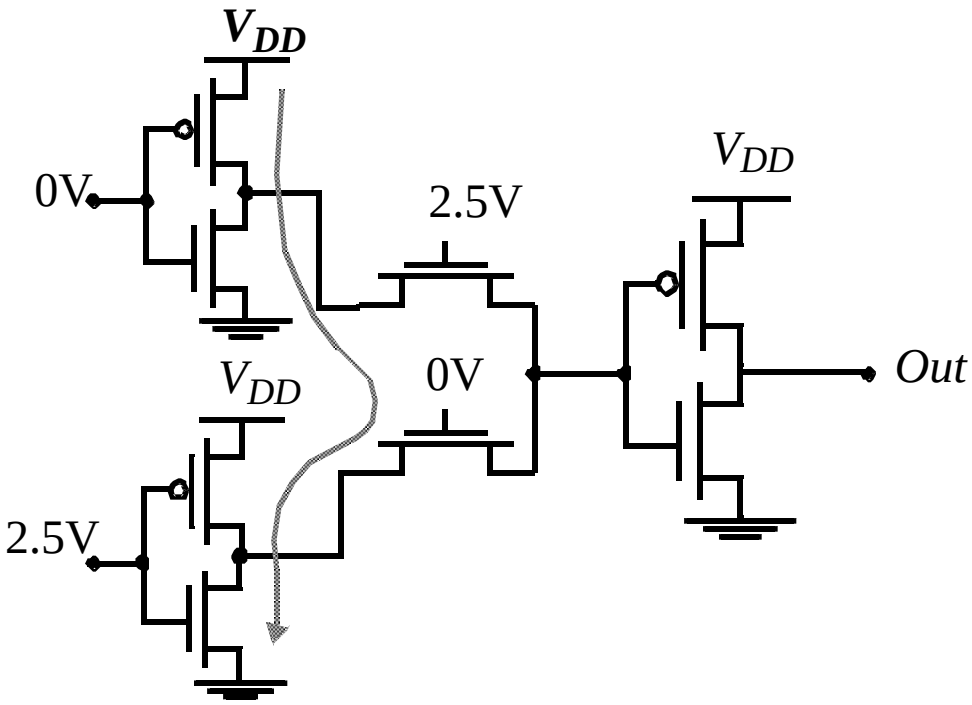
- Advantage: Full Swing
  - Restorer adds capacitance, takes away pull down current at X
  - Ratio problem

Restorer Sizing



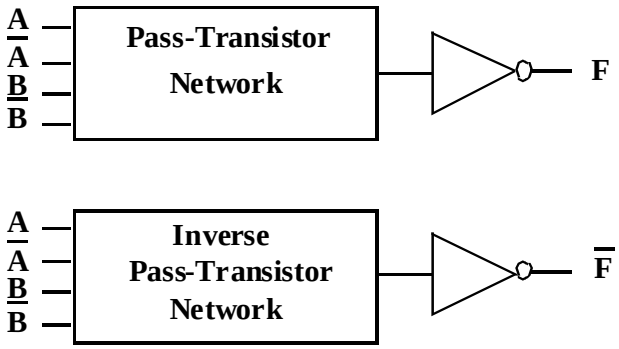
- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

Solution 2: Single Transistor Pass Gate with $V_T=0$

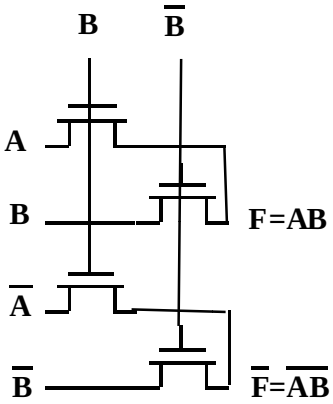


WATCH OUT FOR LEAKAGE CURRENTS

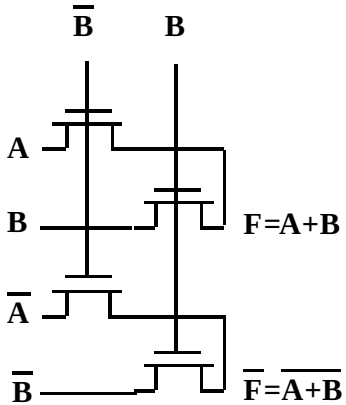
Complementary Pass Transistor Logic



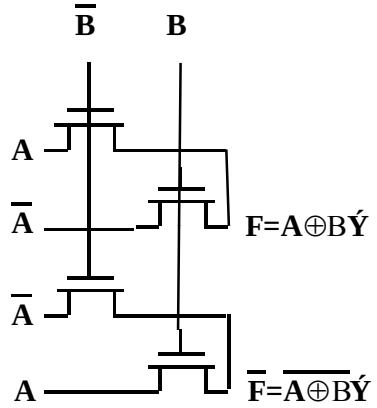
(a)



AND/NAND



OR/NOR



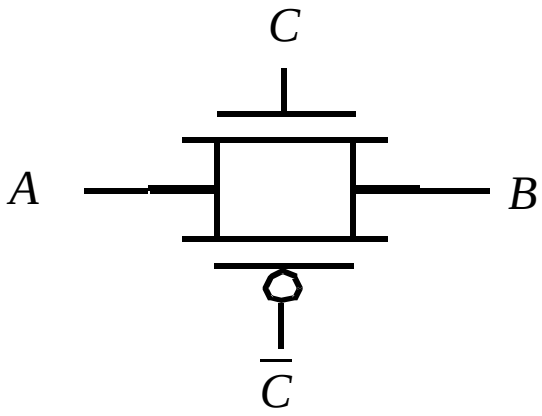
EXOR/NEXOR

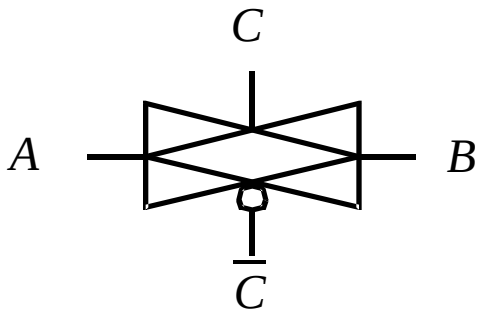
(b)

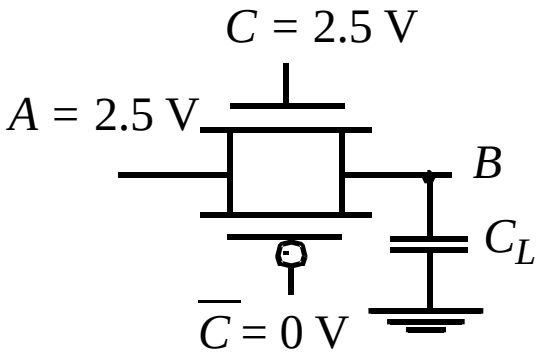
Advantages of CPL

- Circuits are *Differential*
- Static Gate. Advantageous for noise resilience
- Modular design

Solution 3: Transmission Gate

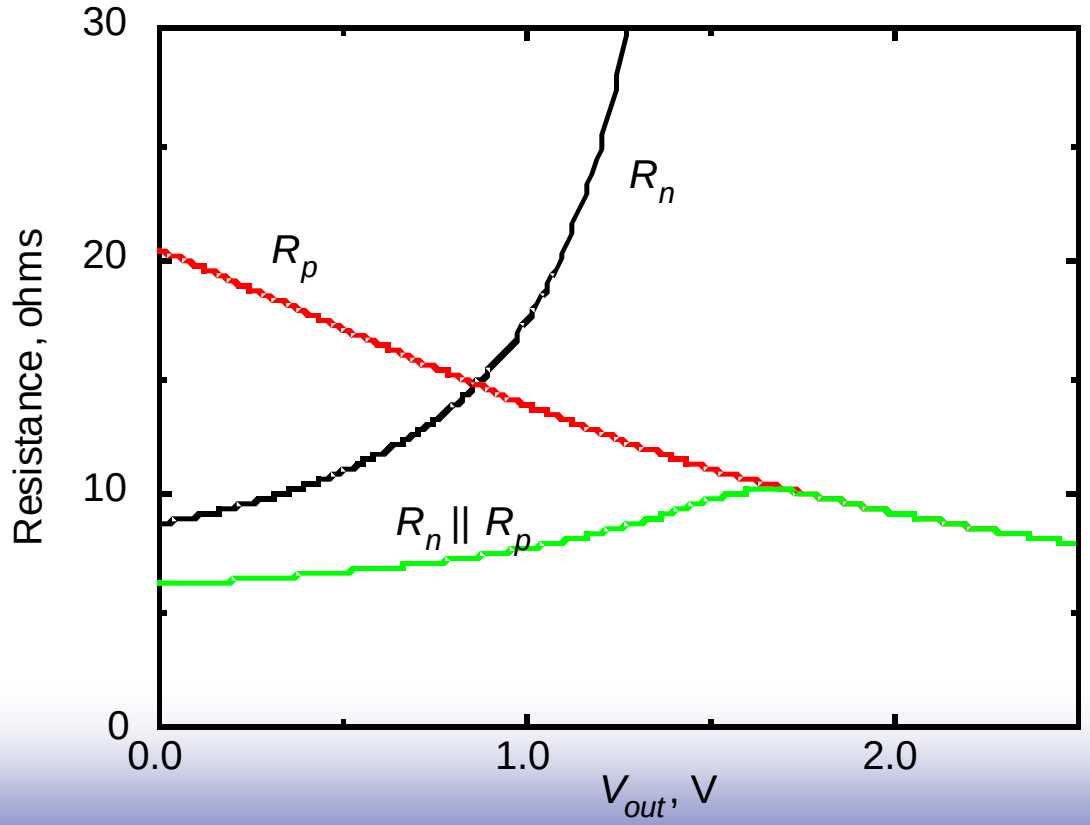


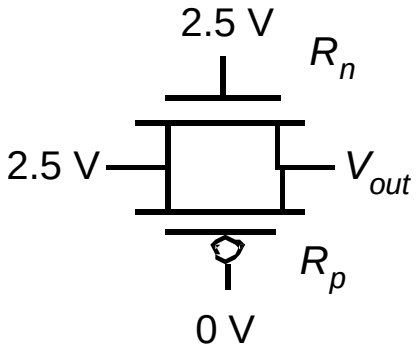




Resistance of Transmission Gate

- *Follow board notes*

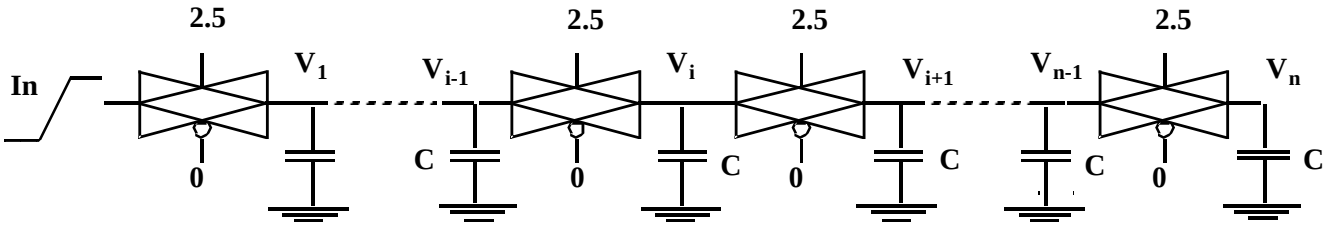




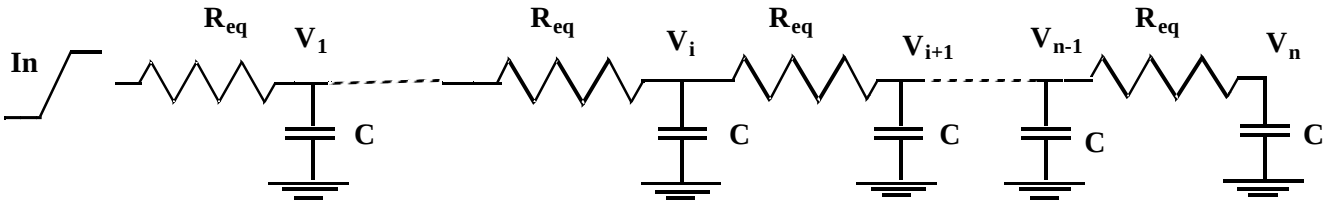
Transfer gate Capacitances

- Follow board notes

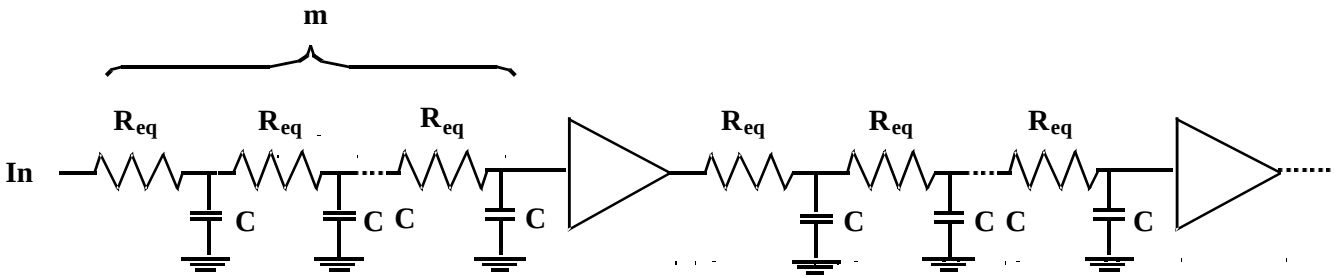
Delay in Transmission Gate Networks



(a)

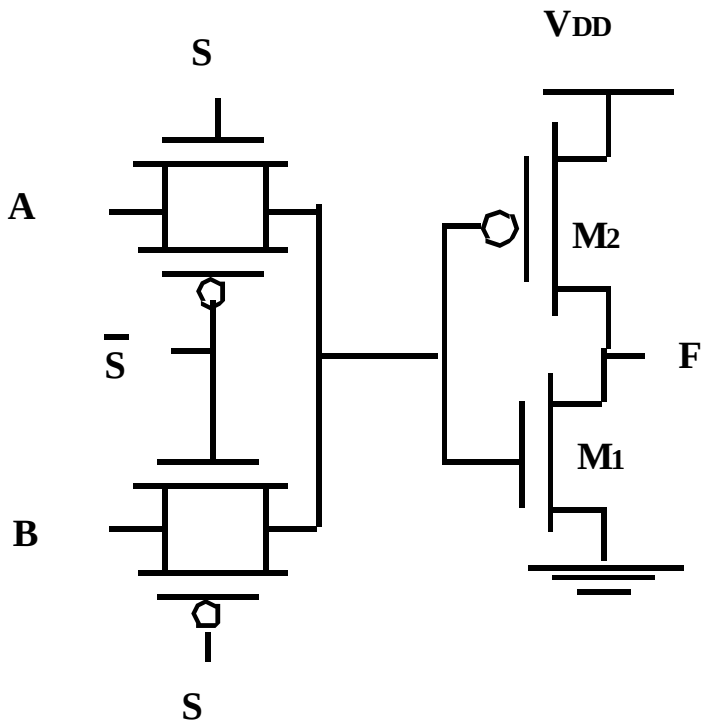


(b)



(c)

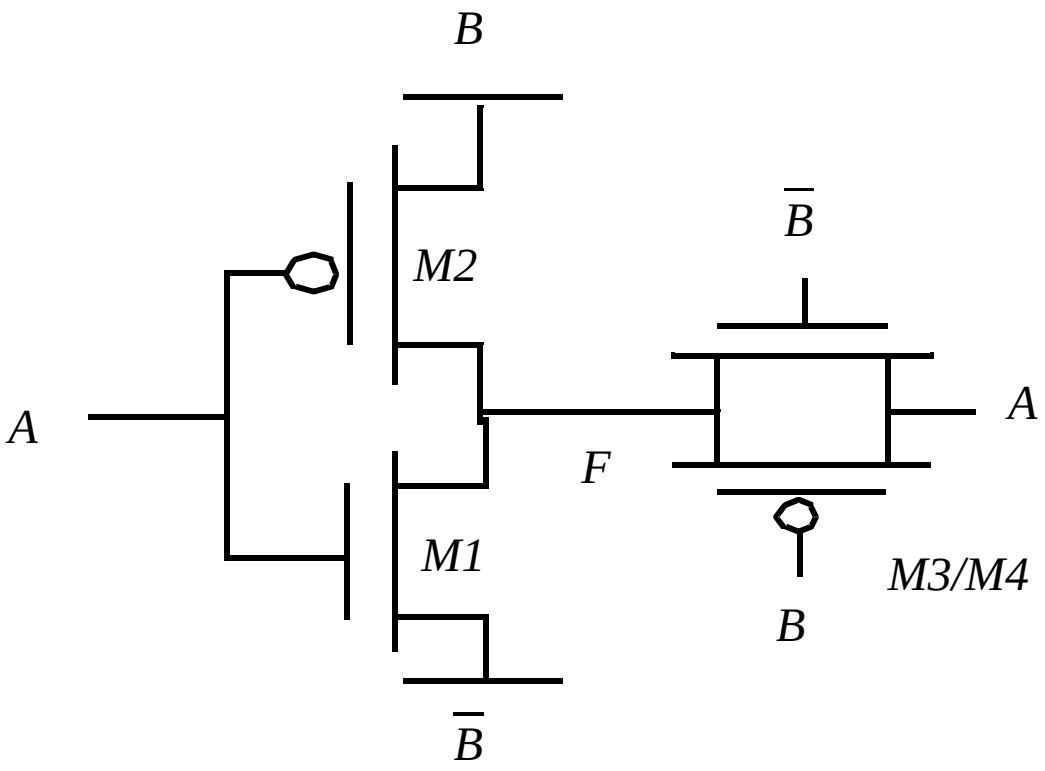
Pass-Transistor Based Multiplexer



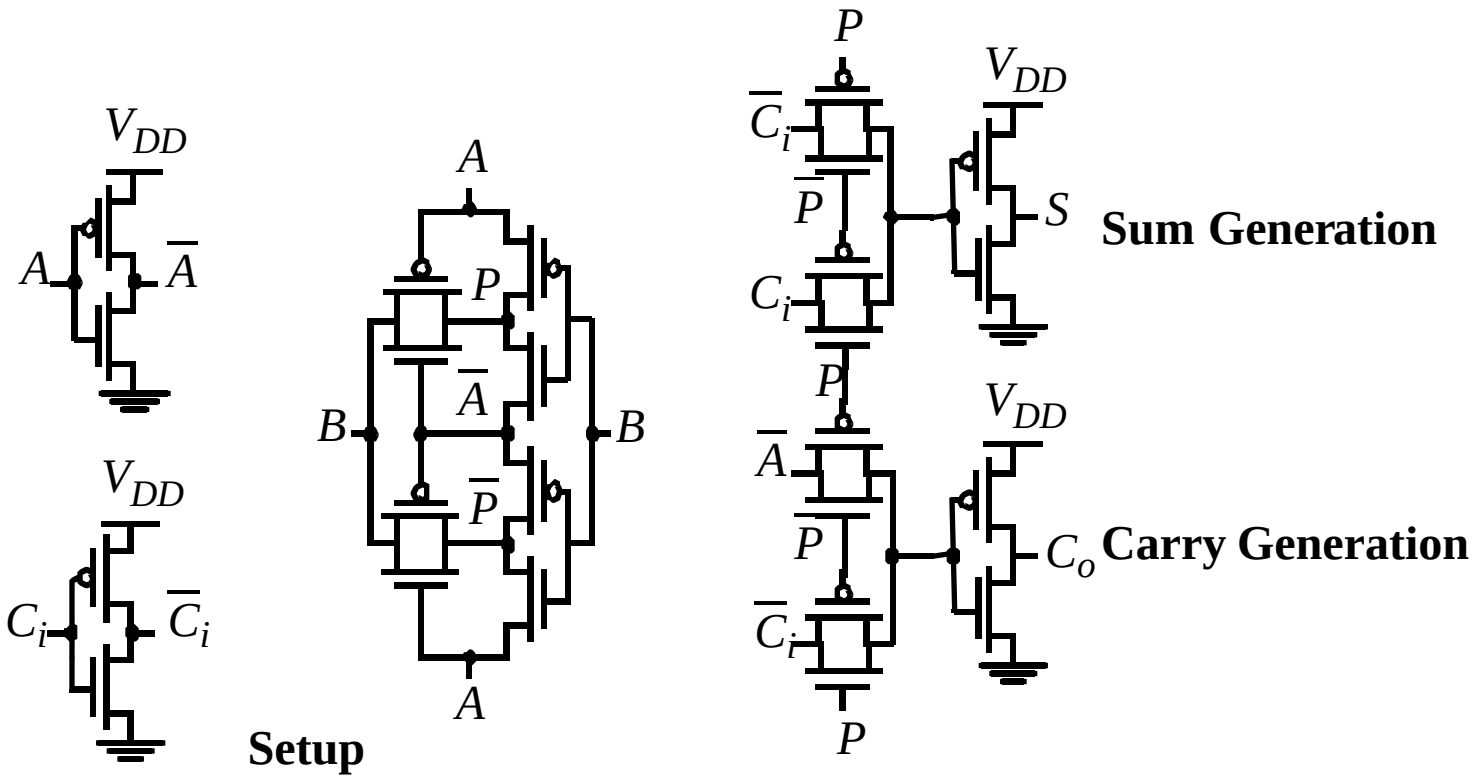
- The control signal S turns the transfer gates on and off depending on its value.
- When s=1, the upper transfer gate is on and that allows A to follow to the output

- Implement the Multiplexer with static CMOS and compare with this

Transmission Gate XOR



Transmission Gate Full Adder



Similar delays for sum and carry