EE 466/586
VLSI Design

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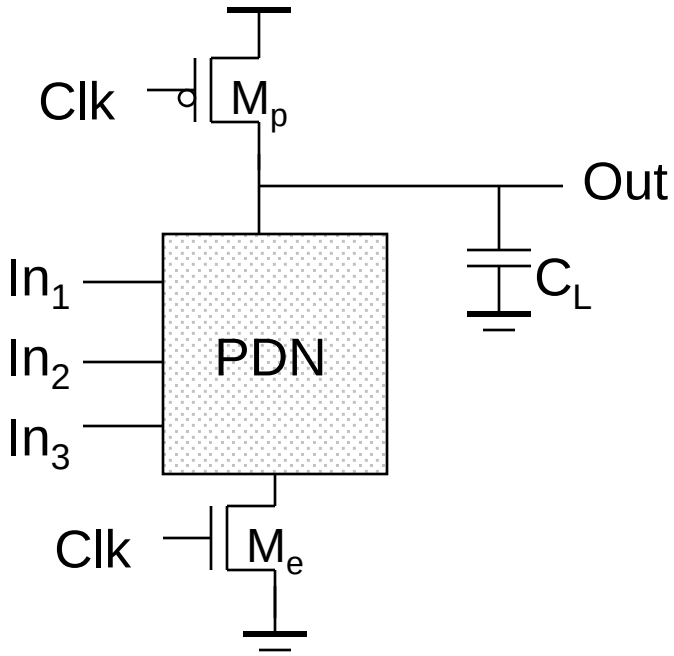
Lecture 15

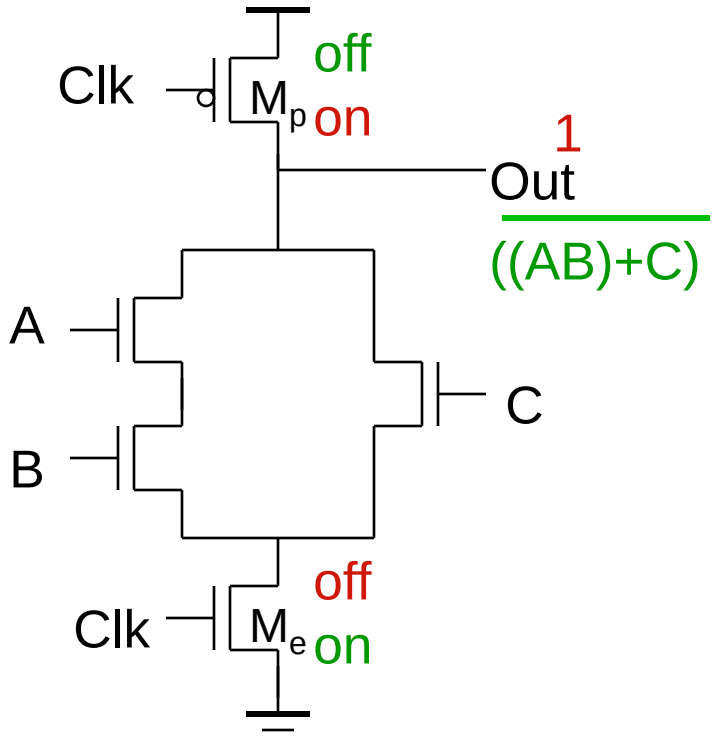
Dynamic Logic

Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on *n* + 2 (*n*+1 N-type + 1 P-type) transistors

Dynamic Gate





Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L
- This behavior is fundamentally different than the static counterpart that always has a low resistance path between the output and one of the power rails.

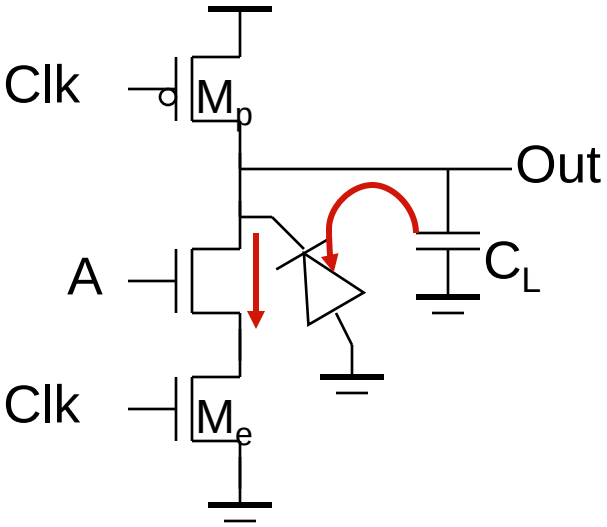
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (Cout)
  - no Isc, so all the current provided by PDN goes into discharging CL

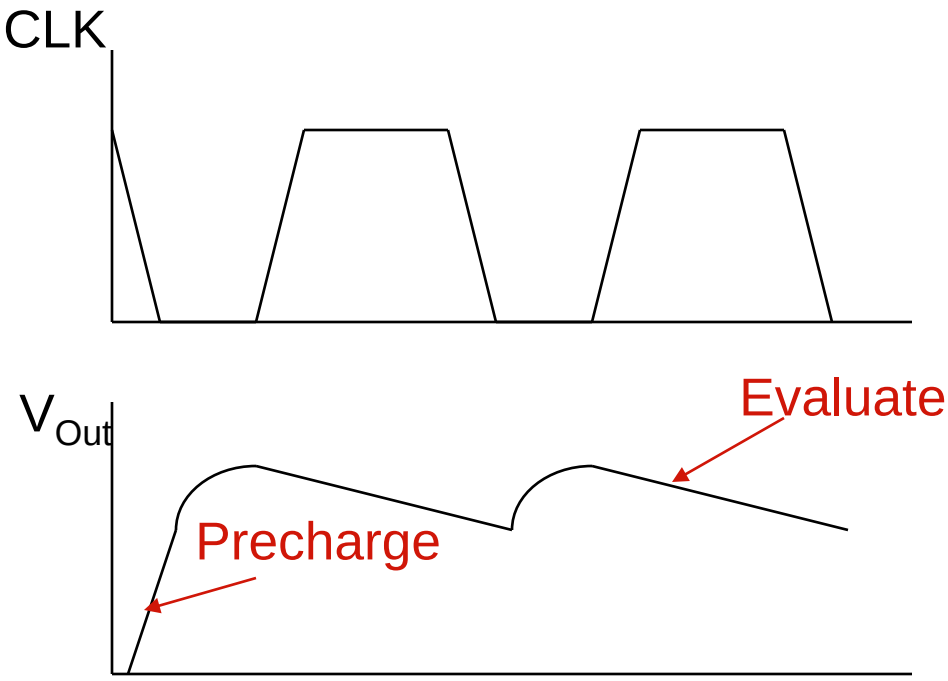
Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- Needs a precharge/evaluate clock

Issues in Dynamic Design 1: Charge Leakage

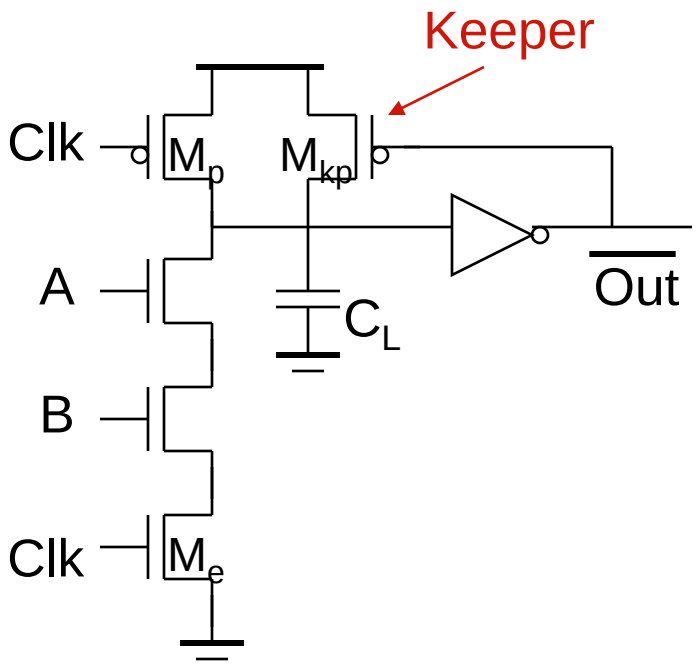


Leakage sources



leakage sources are reverse-biased diode and the sub-threshold leakage of the NMOS pull down device.

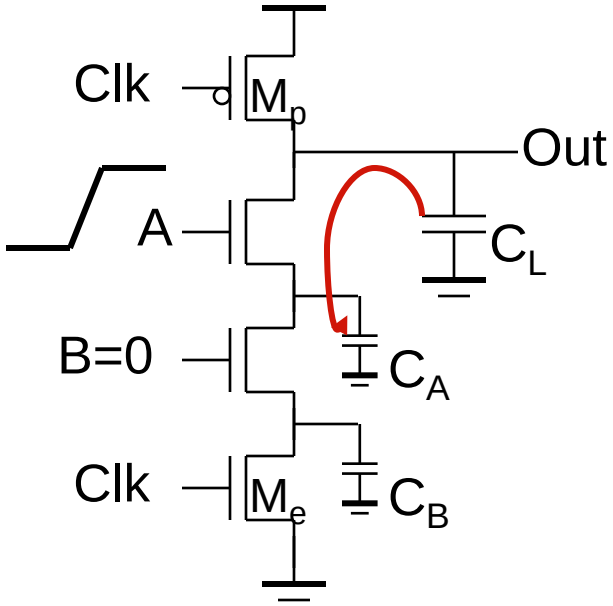
Solution to Charge Leakage



Same approach as level restorer for pass-transistor logic

During precharge, Out is VDD and inverter out is GND, so keeper is on

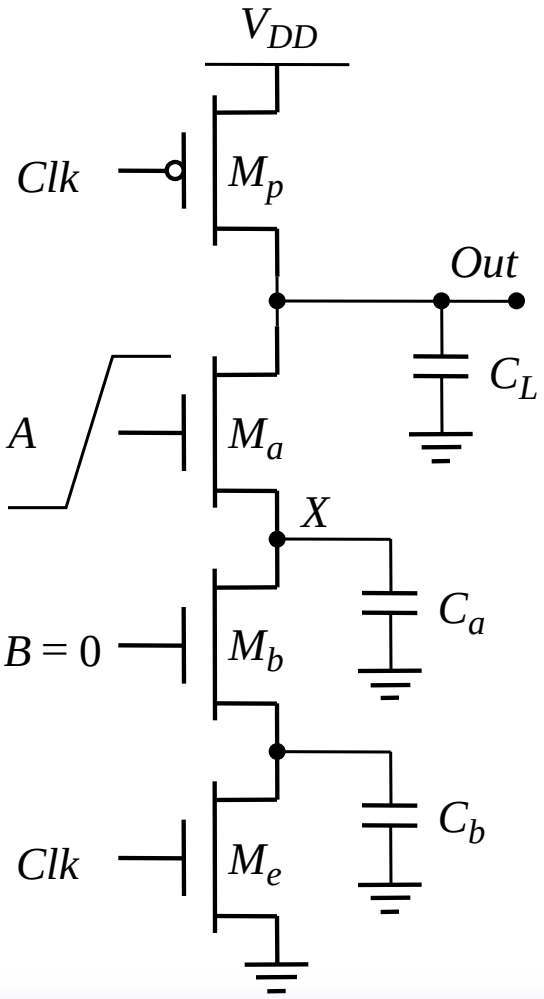
Issues in Dynamic Design 2: Charge Sharing



Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

CA initially discharged and CL fully charged

Charge Sharing



case 1) if $\Delta V_{out} < V_{Tn}$

$$C_L V_{DD} = C_L V_{out}(t) + C_a(V_{DD} - V_{Tn}(V_X))$$

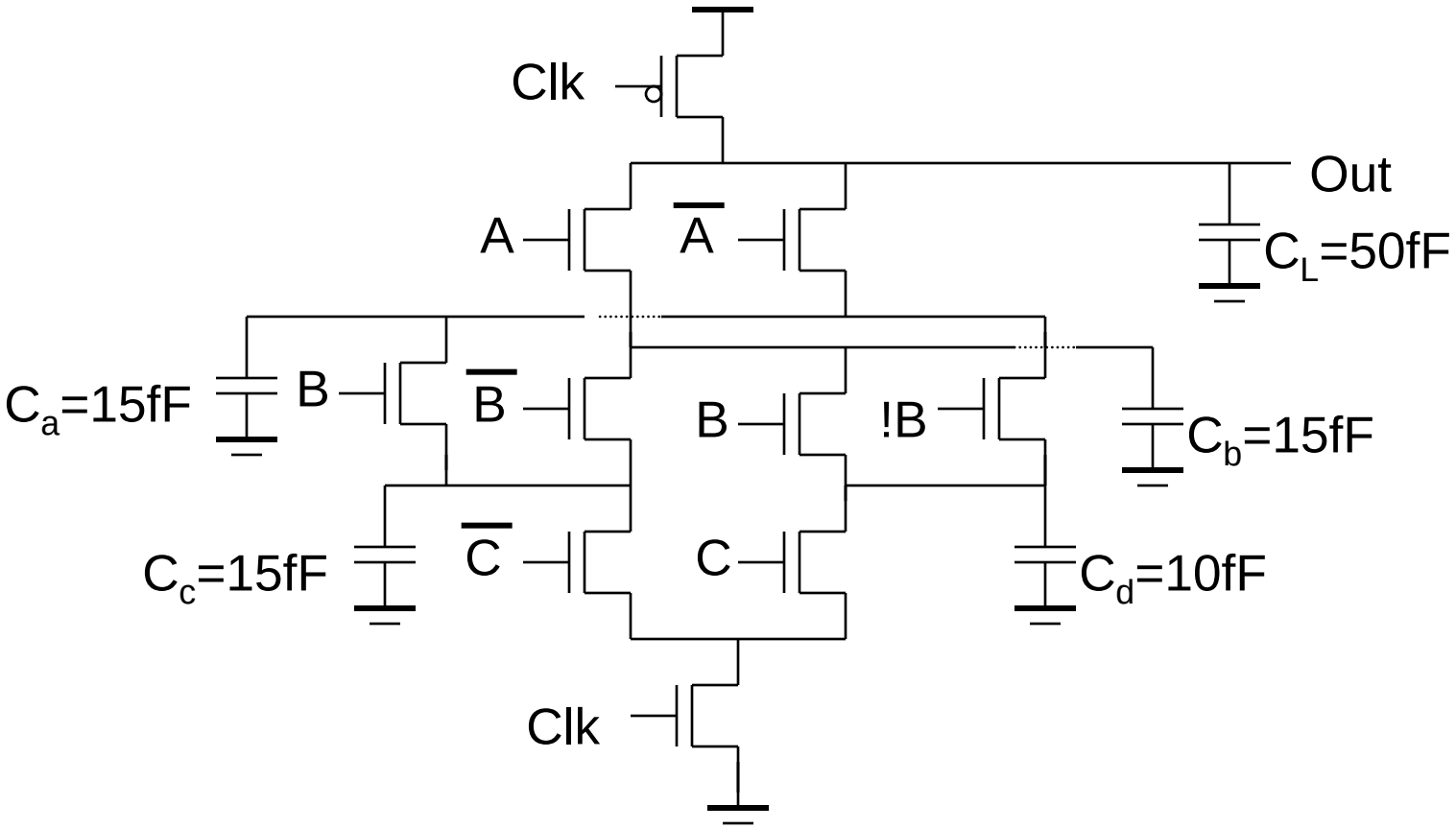
or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L}(V_{DD} - V_{Tn}(V_X))$$

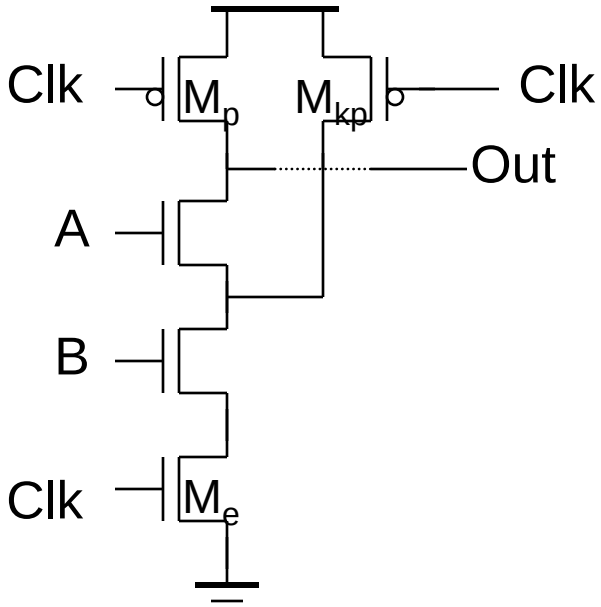
case 2) if $\Delta V_{out} > V_{Tn}$

$$\Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right)$$

Charge Sharing Example

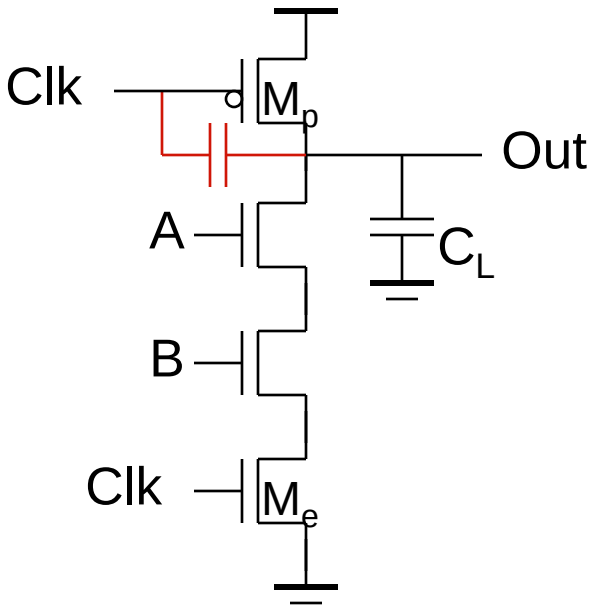


Solution to Charge Redistribution



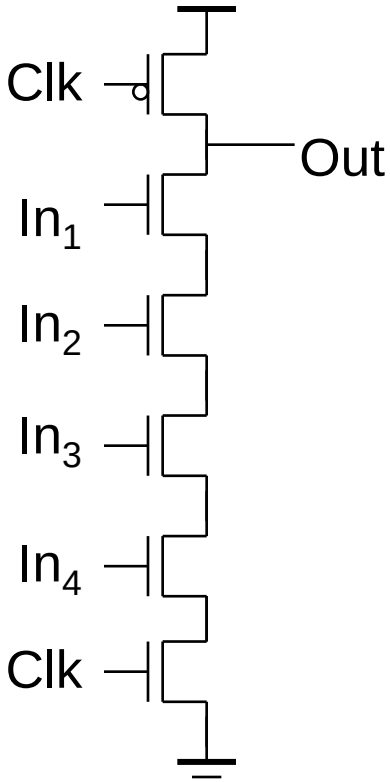
Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

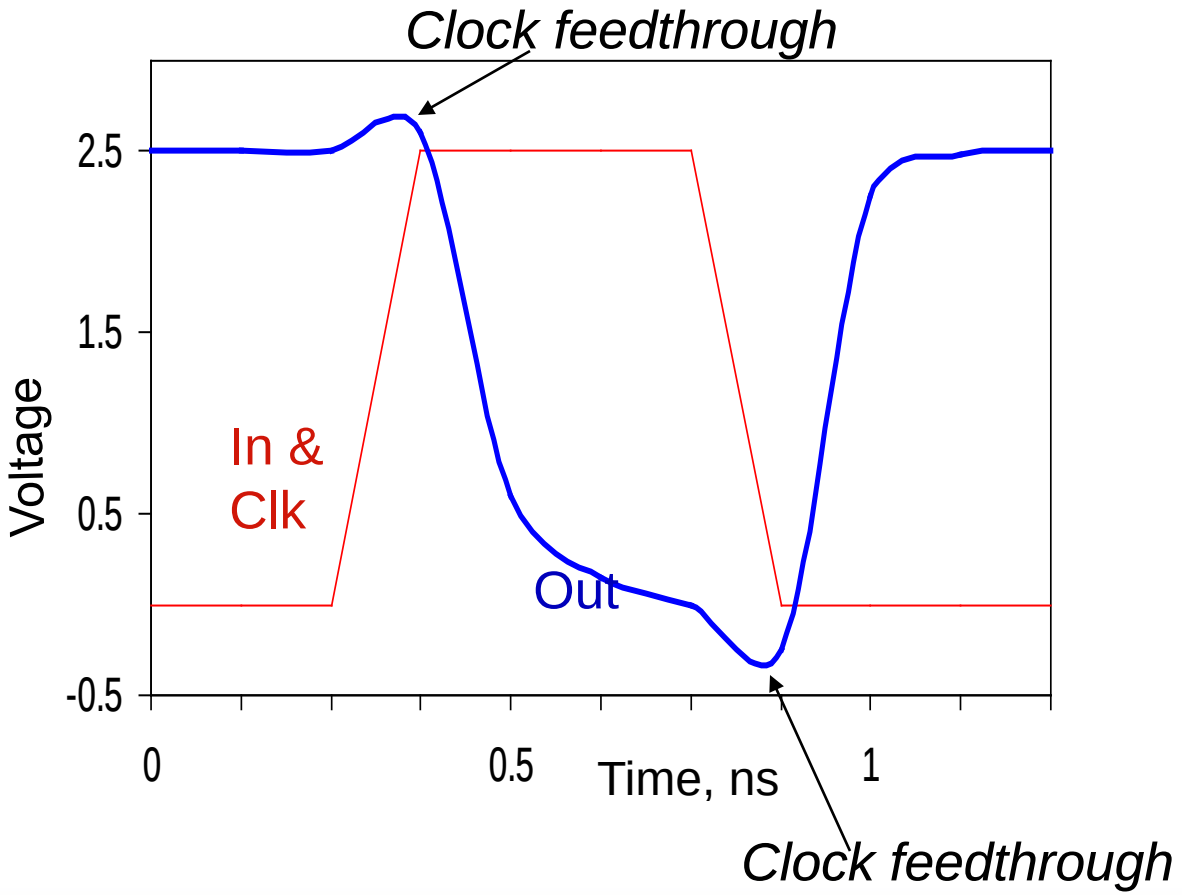
Issues in Dynamic Design 3: Clock Feedthrough



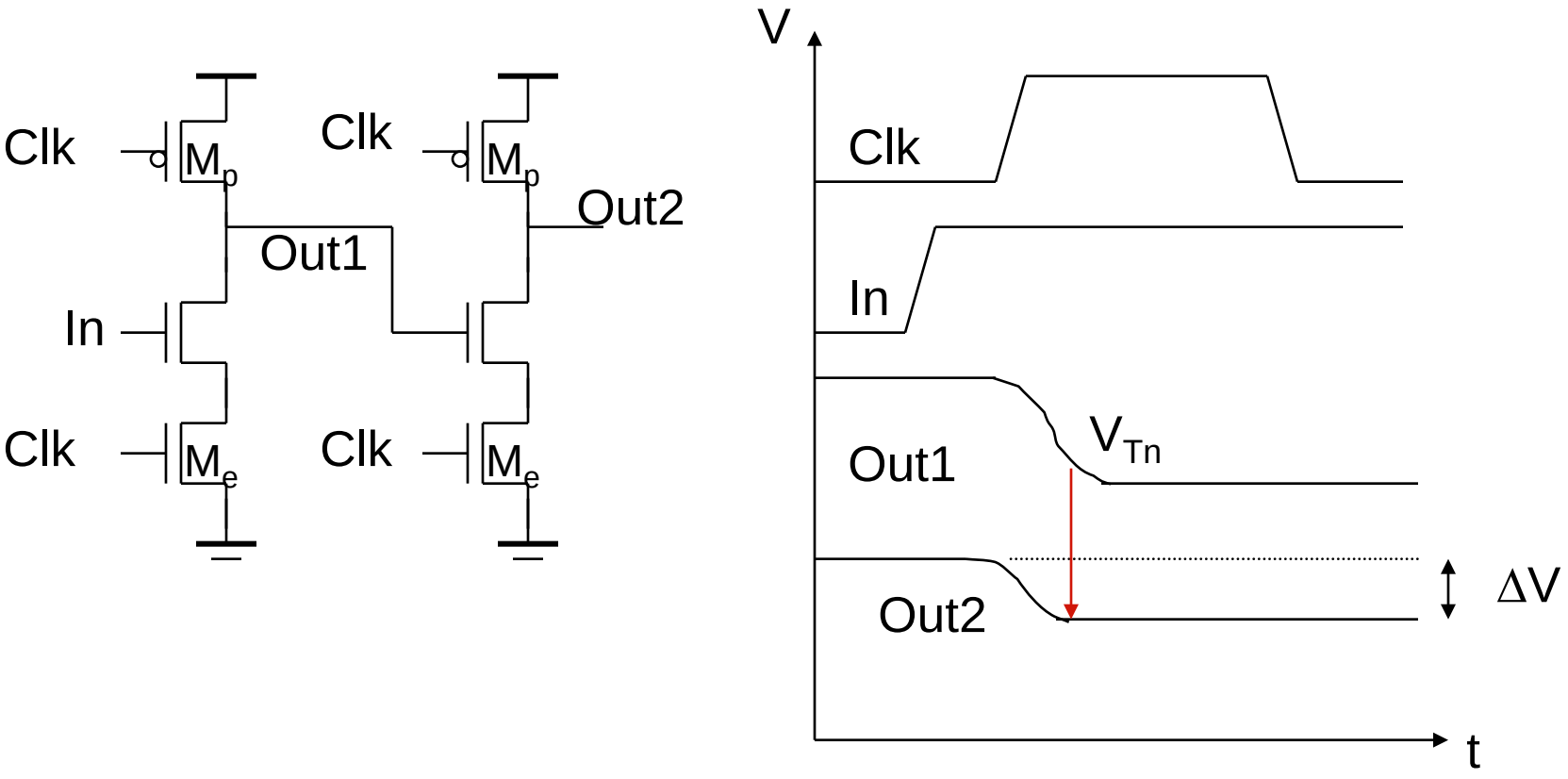
Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to Out.

Clock Feedthrough





Cascading Dynamic Gates

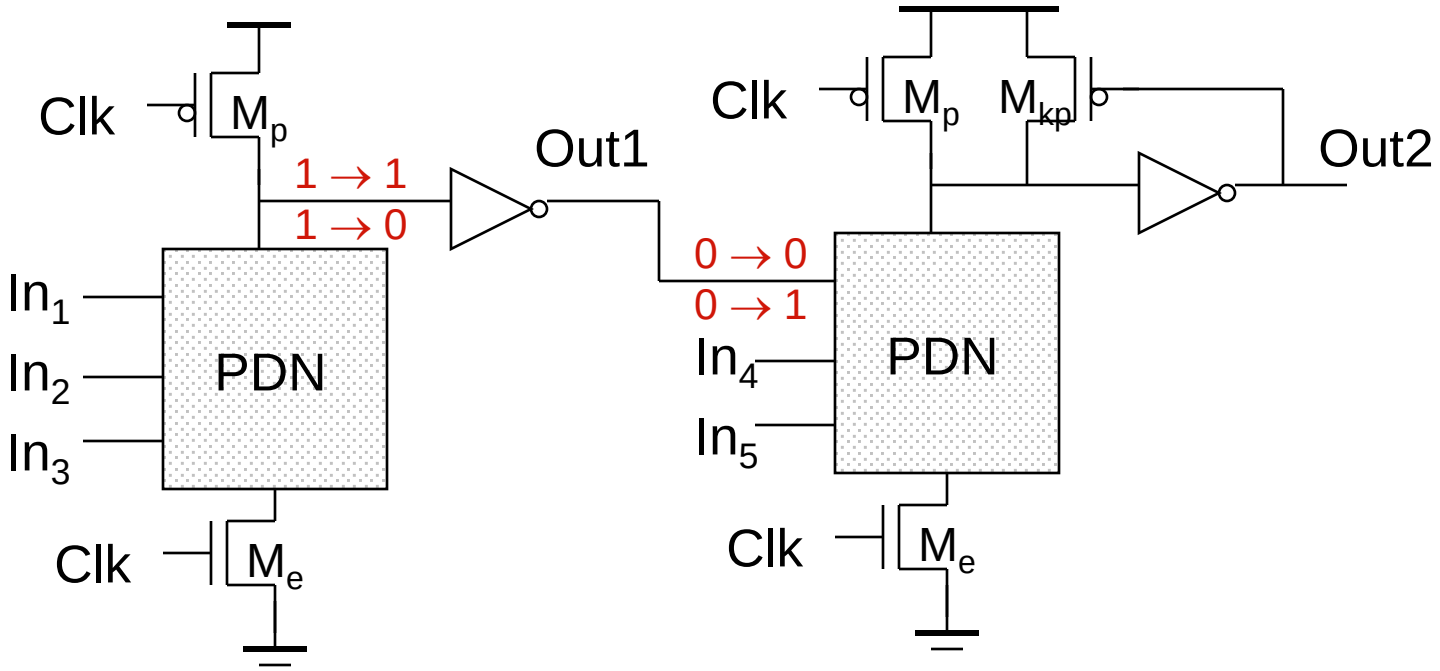


Only 0 → 1 transitions allowed at inputs!

Cascading Dynamic Gates

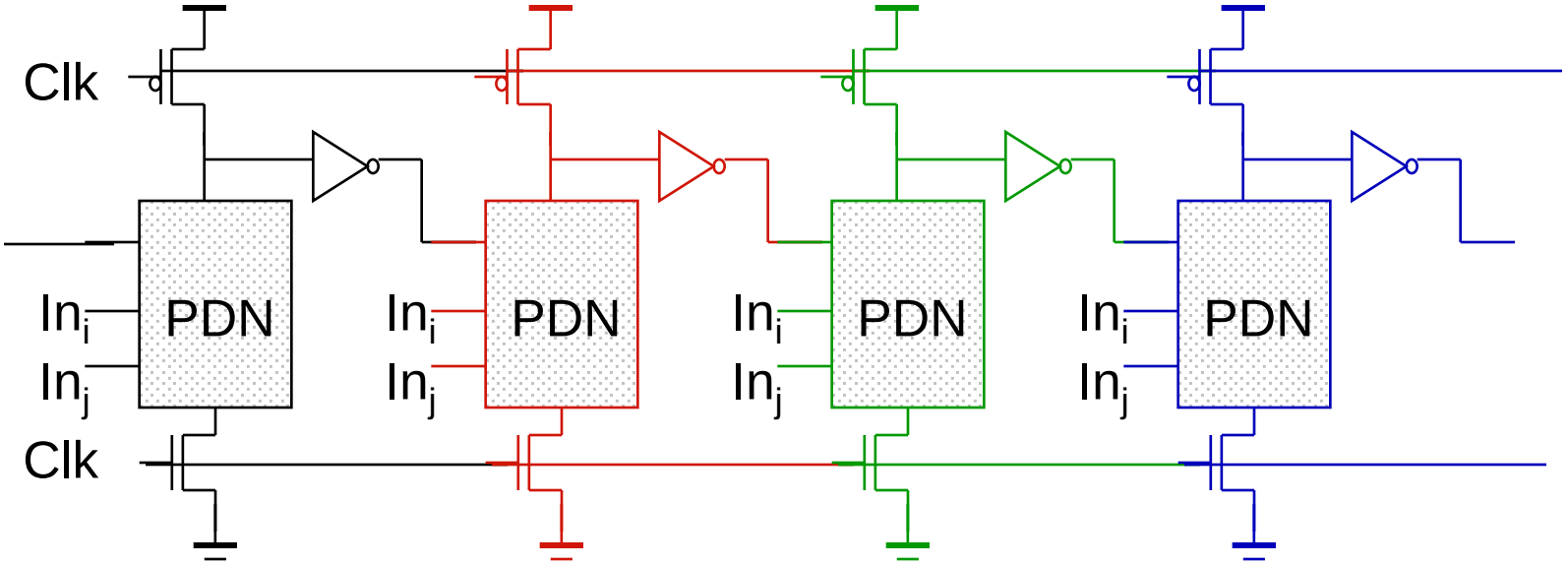
- Out2 should remain at V_{DD} since Out1 transitions to 0 during evaluation. However, since there is a finite propagation delay for the input to discharge Out1 to GND, the second output also starts to discharge.
- The second dynamic inverter turns off (PDN) when Out1 reaches V_{Tn}.
- Setting all inputs of the second gate to 0 during precharge will fix it.
- Correct operation is guaranteed (ignoring charge redistribution and leakage) as long as the inputs can only make a single 0 -> 1 transition during the evaluation period

Domino Logic



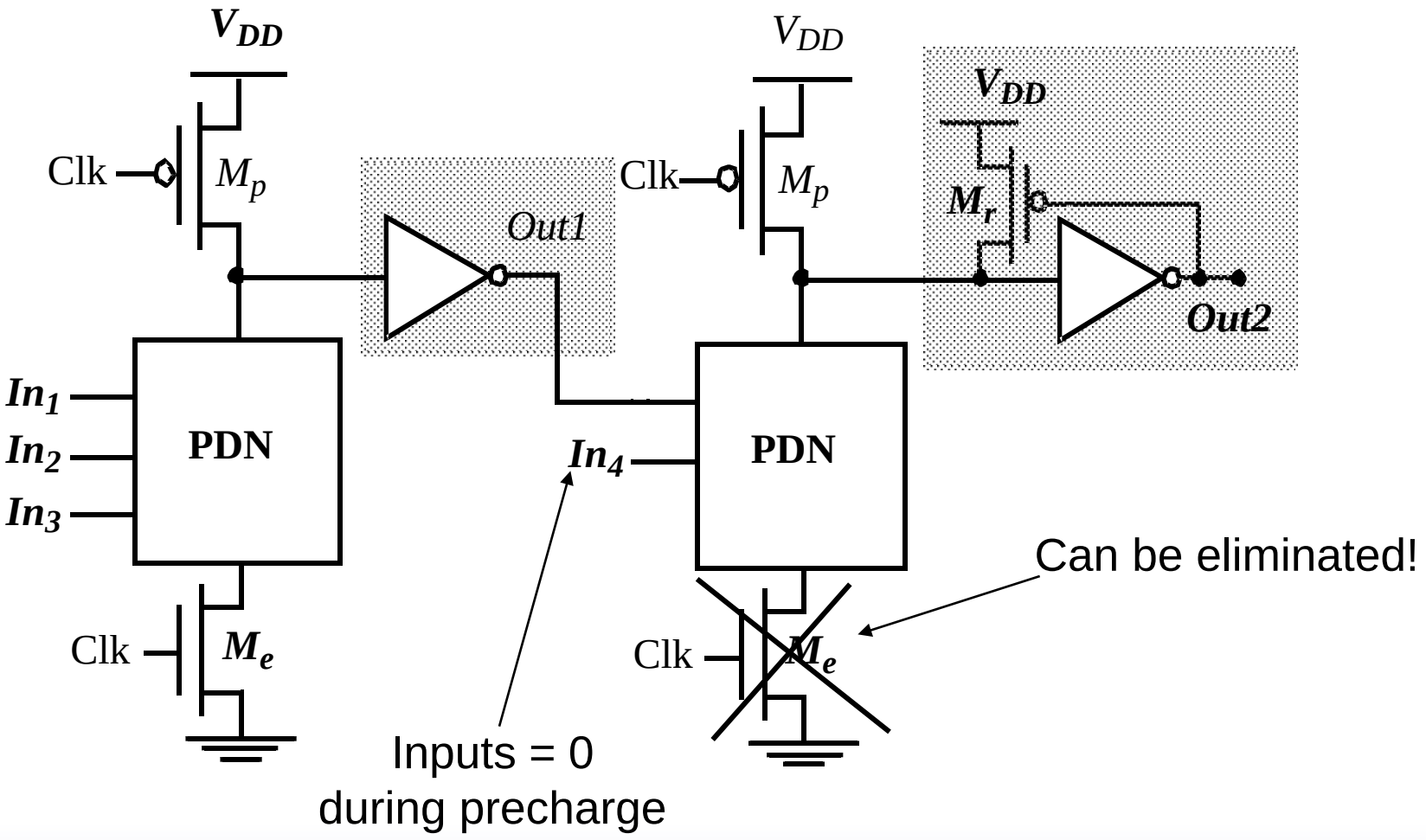
Ensures all inputs to the Domino gate are set to 0 at the end of the precharge period. Hence, the only possible transition during evaluation is 0 -> 1

Why Domino?

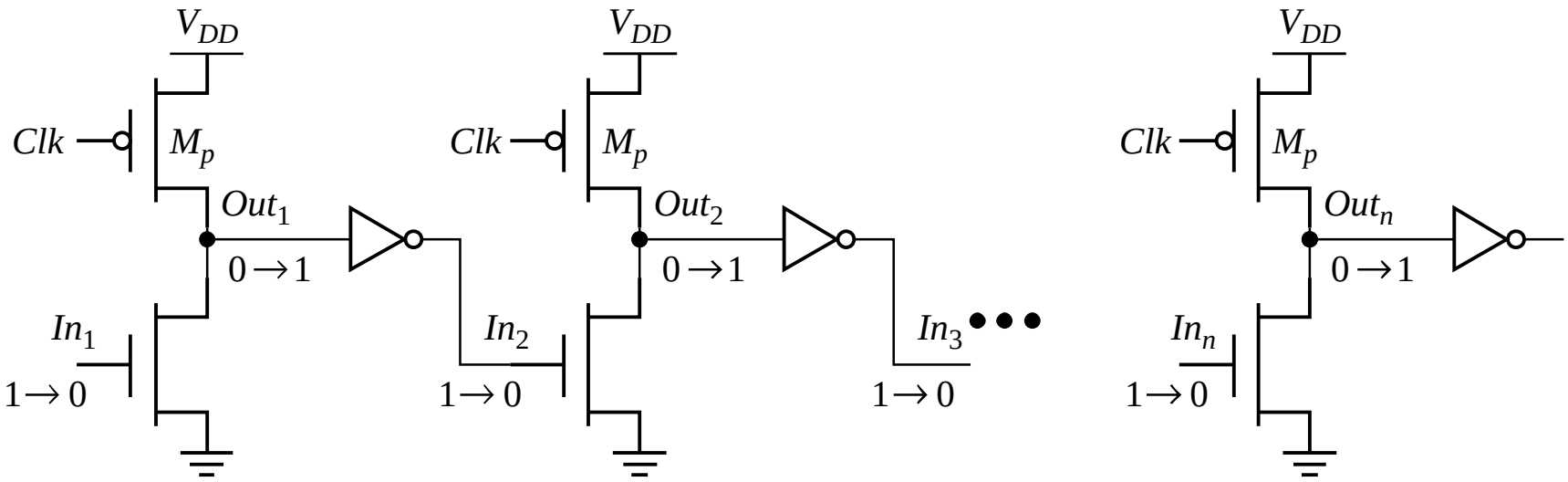


Like falling dominos!

Designing with Domino Logic

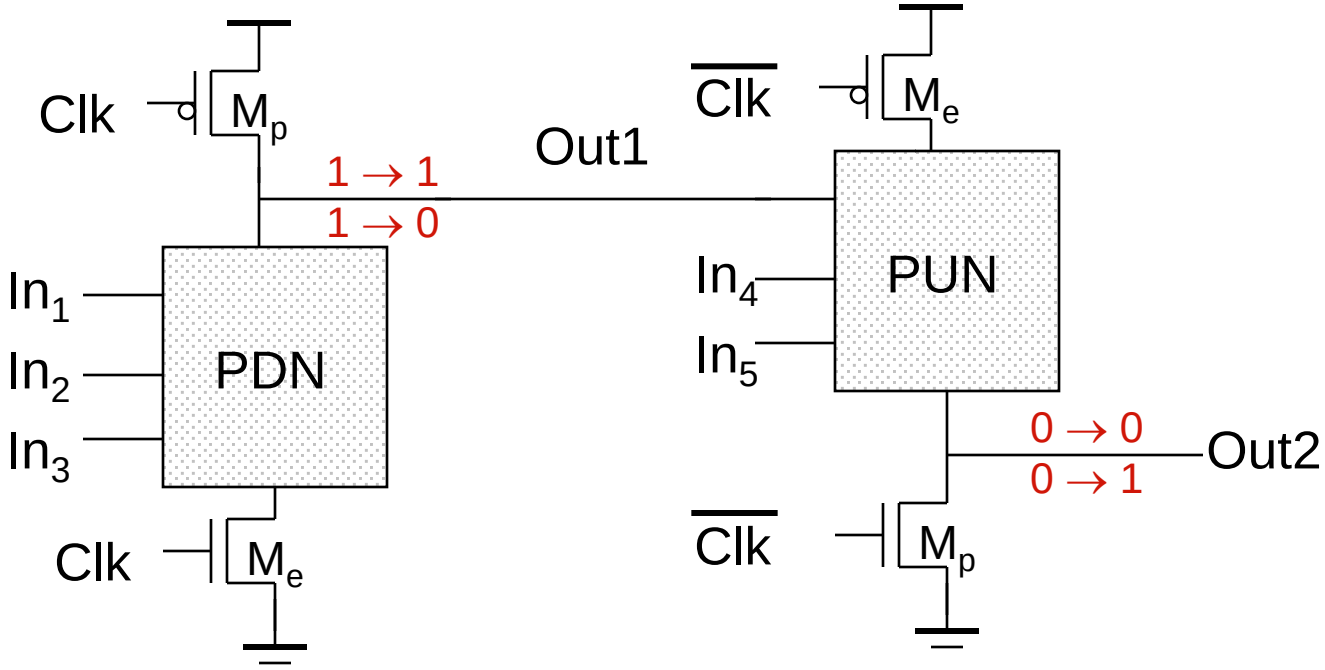


Footless Domino



The first gate in the chain needs a foot switch
Precharge is rippling – short-circuit current
A solution is to delay the clock for each stage

np-CMOS



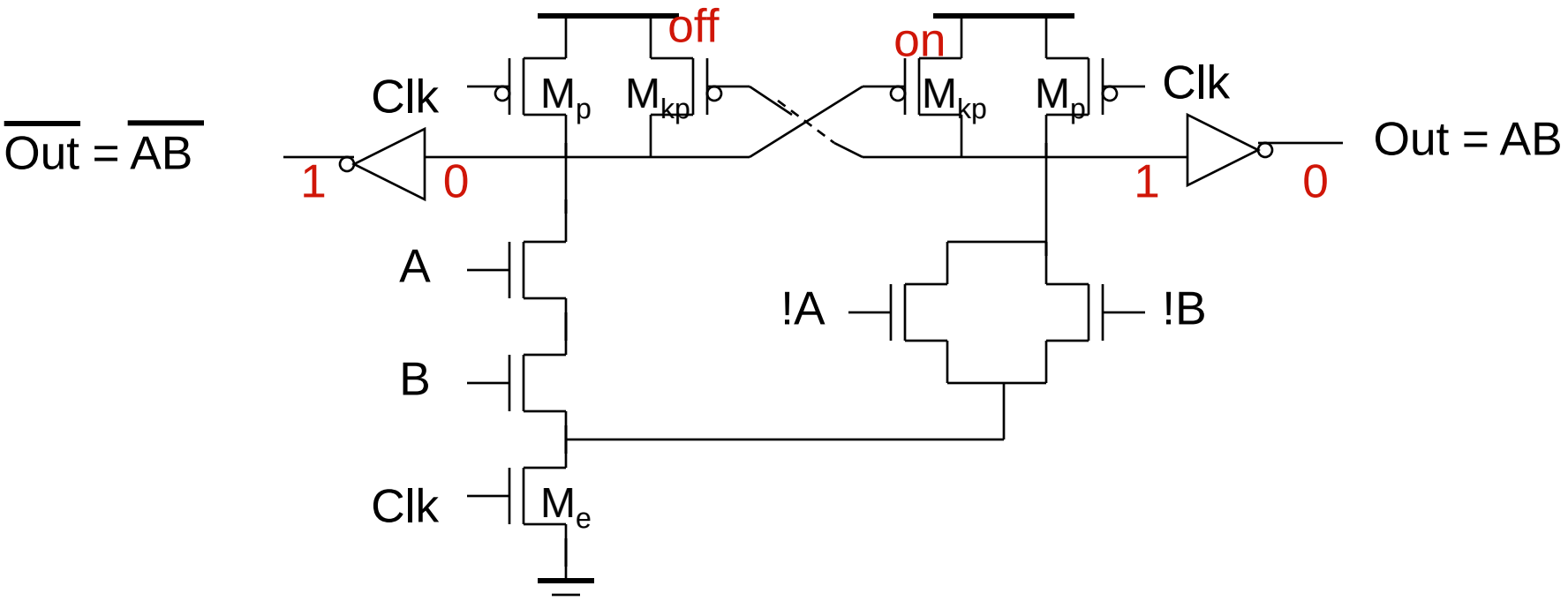
Only $0 \rightarrow 1$ transitions allowed at inputs of PDN

Only $1 \rightarrow 0$ transitions allowed at inputs of PUN

Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition
  - Input capacitance reduced

Differential (Dual Rail) Domino



Solves the problem of non-inverting logic

Take Home Exercise

- Design a dual-rail XOR/XNOR domino gate and share as many transistors as possible between the true and complement logic blocks