EE 466
Course Project

Project Report due on Dec. 15, 2017

Comparative performance evaluation of dynamic and static flip-flops

This design project consists of following specific goals.

(1) Performance evaluation of semi dynamic flip-flops: consider the following three types of semi dynamic flip-flops: (a) implicit-pulsed, data-close-to-output, semi dynamic hybrid flip-flop (ip-DCO) [1], (b) hybrid latch-flip-flop [2] and (c) semi dynamic edge-triggered flip-flop [3]. Then, obtain delay, power consumption, and the total device width for each flip-flop. Undertake this analysis in 65 nm or 45nm technology node.

(2) Implicit-pulsed static flip-flops: In the next step you are required to design a time-borrowing master-slave flip-flop (tb-SMS) [1]. Obtain delay, power consumption, and the total device width. Undertake the design and the analysis in the 65 nm or 45nm technology node.

(3) Explicit-pulsed flip-fops: In this step, you are required to design an explicit-pulsed, hybrid static flip-flop (ep-SFF) [1] and compare its performance with the tb-SMS and ip-DCO. Among these three which one has the shortest delay? Which one has the lowest power consumption? Which one has the smallest total device width? Undertake the design in the 65 nm or 45nm technology node.

(4) Dual edge-triggered flip-flops: In this step, you will be investigating characteristics of dual edge-triggered flip-flops. Modify the ep-SFF designed above to make it dual edge triggered. Design a dual edge-triggered, explicit-pulsed static hybrid flop (ep-DSFF) [1]. Obtain delay, power consumption, and the total device width. Undertake this design also in 65 nm or 45nm technology node.

(5) Among all the above flip-flops which one is the fastest? Is the fastest design most power efficient? Which one you should use in high-speed operation? Which one should be used for majority of the data paths?

(6) You need to submit a detailed report with all waveforms. You need to explain the operations of each circuit clearly and justify your claim with suitable experimental results. The questions asked in the point (5) above need to be answered in the paper. You are welcomed to add any new reference you want to add to enhance the quality of your work.

Please follow the following references for this project:

1. J. Tschanz et al., “Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High-Performance Microprocessors”, ISLPED’01, August 6-7, 2001, Huntington Beach, Califomia, USA.

2. H. Partovi et al., “Flow-Through Latch and Edge-Triggered Flip-flop Hybrid Elements” 1996 IEEE International Solid-state Circuits Conference (ISSCC).
3. Fabian Klass et al., “A New Family of Semi dynamic and Dynamic Flip-Flops with Embedded Logic for High-Performance Processors” IEEE Journal of Solid-State Circuits, vol. 34, no. 5, may 1999.