# EE434

# ASIC and Digital Systems

## Midterm Exam 2

## April 8, 2016. (5:10pm – 6pm)

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**Name:**

**WSU ID:**

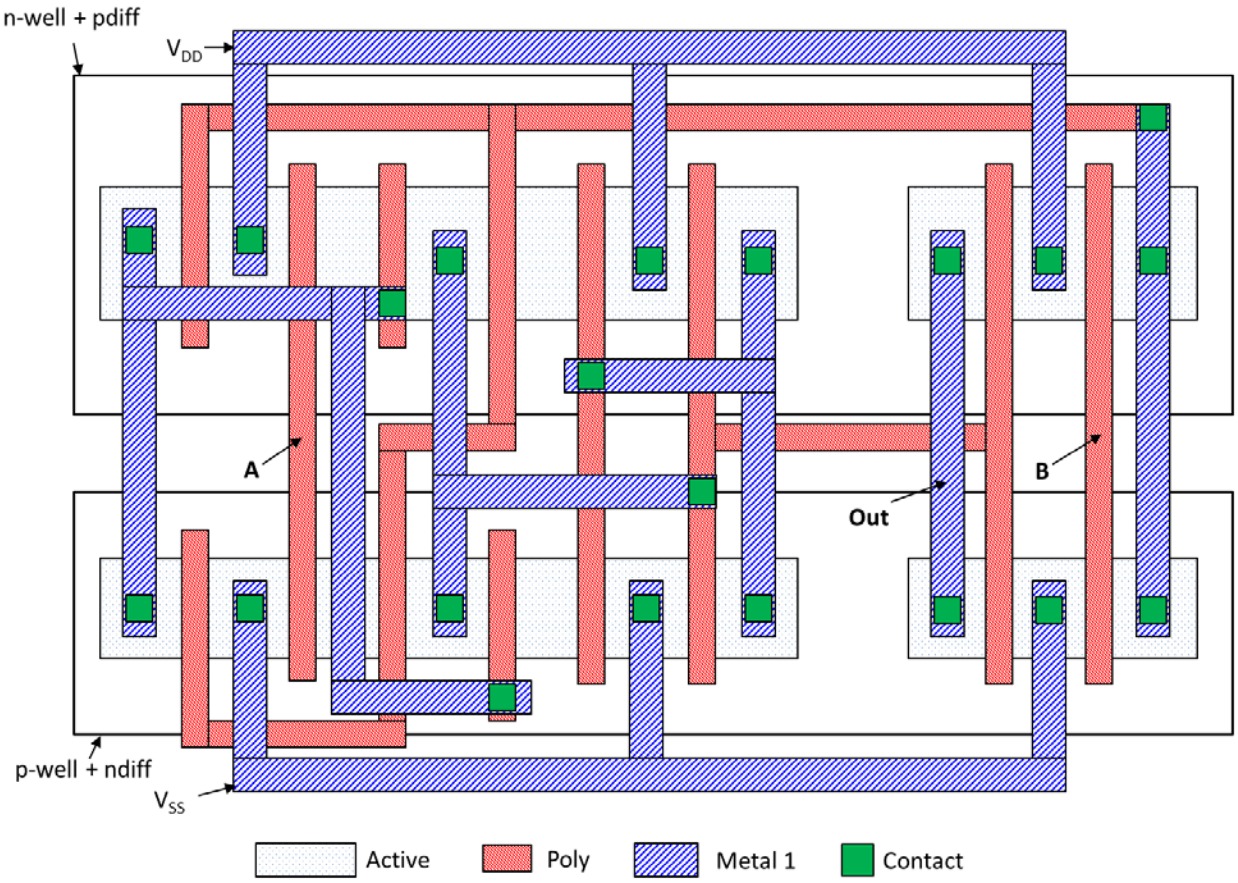
| Problem | Points | |
|---|---|---|
| 1 | 15 | |
| 2 | 15 | |
| 3 | 15 | |
| 4 | 10 | |
| 5 | 13 | |
| 6 | 12 | |
| Total | 80 | |

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

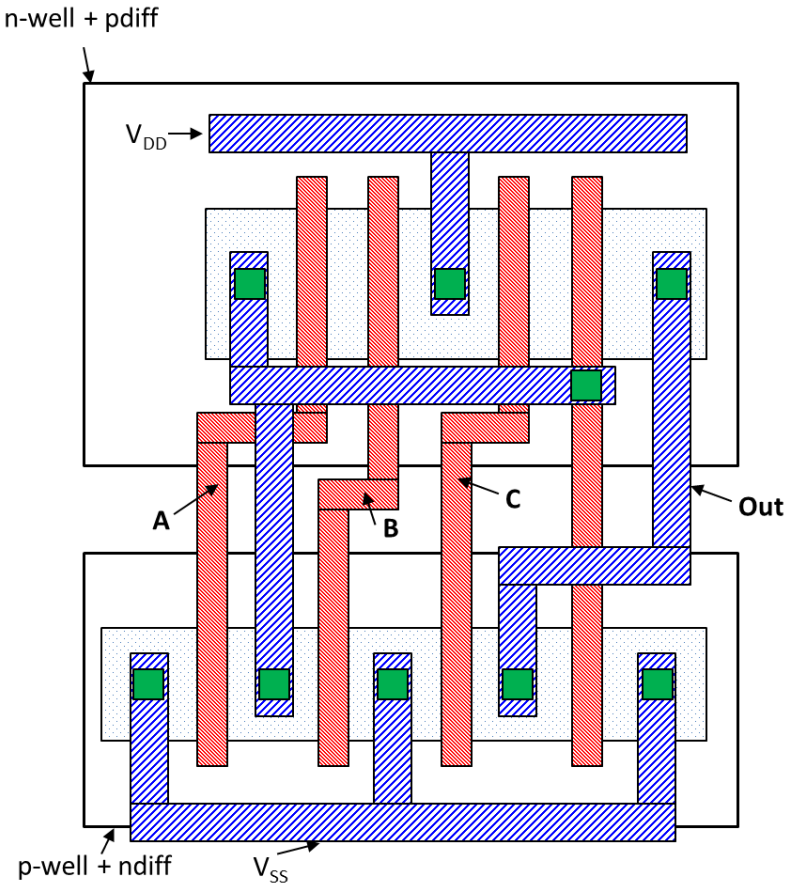
## Problem #1 (Layout, 15 points).

Represent $Out$ as a Boolean function of $A$ and $B$ or describe the function of the following layout in as much detail as possible (Primary inputs: A, B. Primary output: Out).

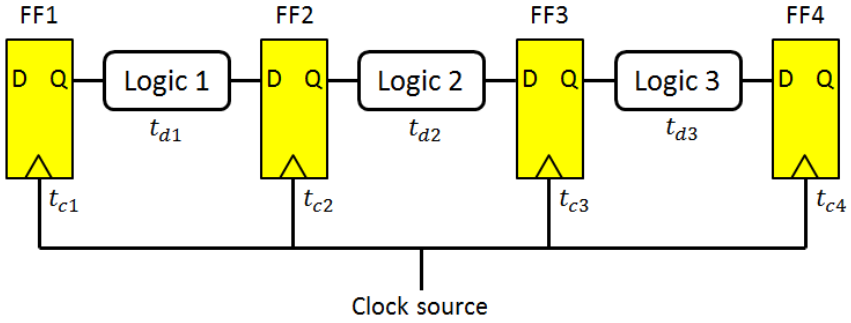


## Problem #2 (Layout, 15 points).

Represent $Out$ as a Boolean function of $A, B$ and $C$ or describe the function of the following layout in as much detail as possible (Primary inputs: A, B, C. Primary output: Out).



## Problem #3 (Timing Analysis, 15 points).




Four flip-flops are connected as shown above.

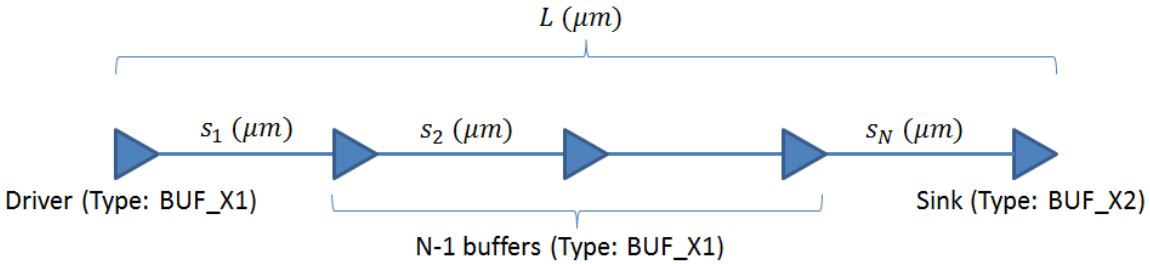
- F/F internal delay: $t_{CQ} = 50ps$
- Setup time of each F/F: $t_s = 50ps$
- Delay of Logic 1: $t_{d1} = 450ps$
- Delay of Logic 2: $t_{d2} = 480ps$
- Delay of Logic 3: $t_{d3} = 250ps$
- Delay of the clock from the clock source to FF1: $t_{c1} = 400ps$
- Delay of the clock from the clock source to FF#: $t_{c\#}$ (#=2, 3, 4)

Since the delays of Logic 1 and Logic 2 are too large, Logic 1 and Logic 2 will violate the setup time constraint if the clock skew is zero (i.e., $t_{c1} = t_{c2} = t_{c3} = t_{c4}$). To resolve this issue, we want to intentionally use the clock skew. However, we also want to minimize the total clock delay ($t_{c1} + t_{c2} + t_{c3} + t_{c4}$) to minimize the clock power consumption. Find $t_{c2}$, $t_{c3}$, and $t_{c4}$ that satisfies the setup time constraint and minimizes the total clock delay ($t_{c1} + t_{c2} + t_{c3} + t_{c4}$).

## Problem #4 (Timing Analysis, 10 points).

Can a path have both setup and hold time violations at the same time? Yes/No. Explain why.

## Problem #5 (Interconnect, 13 points).

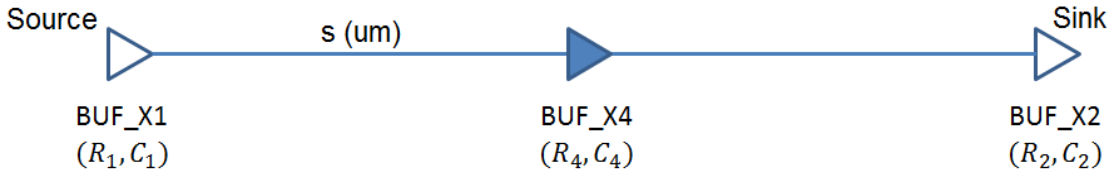



A source (type: BUF_X1) drives a sink (type: BUF_X2) through a net and you are supposed to ***optimally*** insert N-1 buffers (type: BUF_X1) between them. Find the number of buffers to insert (i.e., find N) and the optimal locations of the buffers (i.e., find $s_1, s_2, \ldots, s_N$) minimizing the total delay.

- Output resistance of BUF_X1: $R_1$
- Input capacitance of BUF_X1: $C_1$
- Input capacitance of BUF_X2: $C_2$
- Total length of the net: L (um)
- Unit wire resistance: $r_w$
- Unit wire capacitance: $c_w$

## Problem #6 (Interconnect, 12 points).

A source (type: BUF_X1) drives a sink (type: BUF_X2) through a net and we want to *optimally* insert a buffer (type: BUF_X4) between them to minimize the total signal delay as shown in the figure below. s is the distance between the source and the buffer. Answer the following questions.




- Output resistance of each cell: $R_{\#}$ $(R_1 > R_2 > R_4)$
- Input capacitance of each cell: $C_{\#}$ $(C_1 < C_2 < C_4)$
- Unit wire resistance and capacitance: $r_w$, $c_w$

1) If $R_4$ goes up, $s$ should go up. (True/False)

2) If $C_4$ goes up, $s$ should go up. (True/False)

3) If $R_1$ goes up, $s$ should go up. (True/False)

4) If $C_2$ goes up, $s$ should go up. (True/False)

5) If $r_w$ goes up, $s$ should go up. (True/False)

6) If $c_w$ goes up, $s$ should go up. (True/False)