EE434

ASIC and Digital Systems

Midterm Exam 2

Mar. 28, 2018. (4:10pm – 5pm)

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Name:

WSU ID:

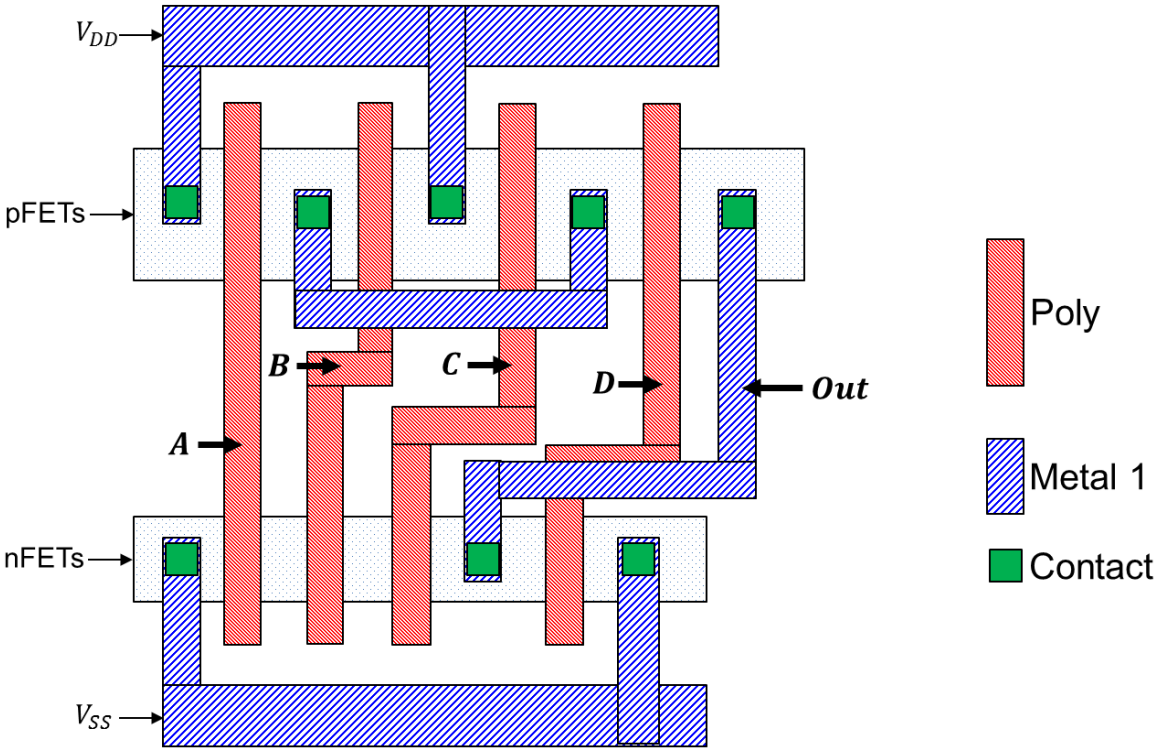
Problem	Points	
1	10	
2	10	
3	10	
4	20	
5	5	
6	15	
Total	70	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Layout, 10 points)

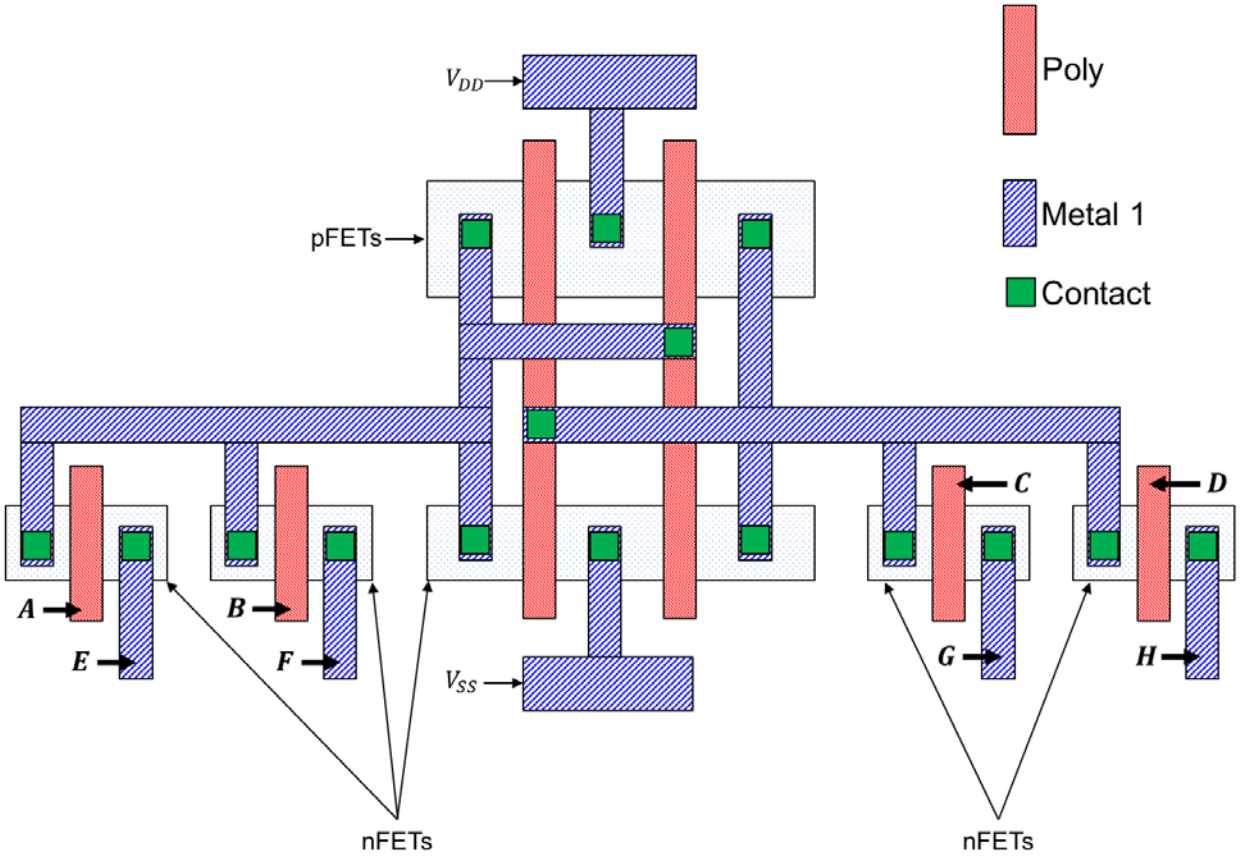
Represent Out as a Boolean function of A, B, C, D.

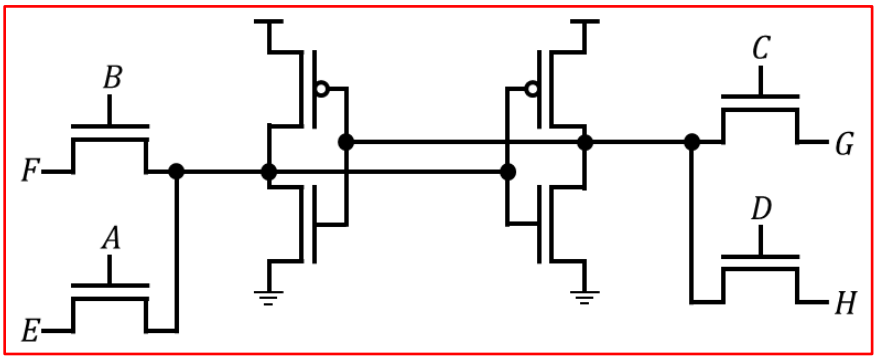


$$Out = \overline{ABC + D}$$

Problem #2 (Layout, 10 points)

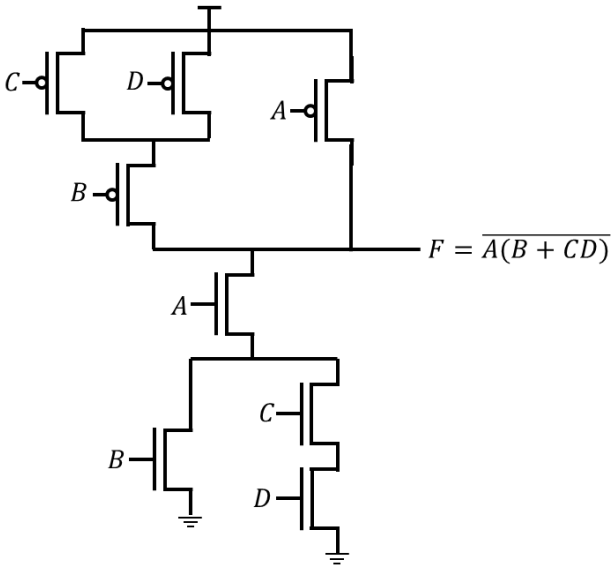
Draw a transistor-level schematic (netlist) for the following layout. Input ports: A, B, C, D. Inout (input/output) ports: E, F, G, H.



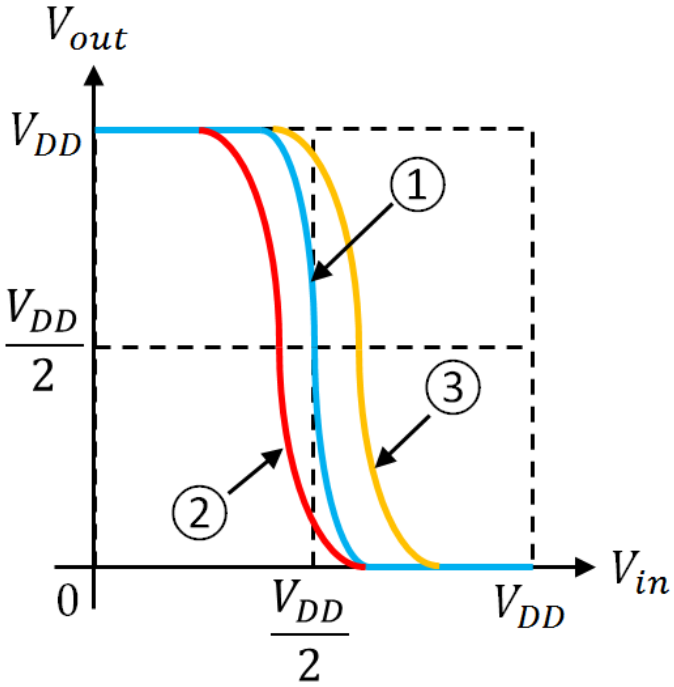


Problem #3 (DC Analysis, 10 points)

The following schematic implements $F = \overline{A(B + CD)}$.



The following shows a DC characteristic graph of the logic above. Currently, the DC characteristic of the above logic follows the curve ①.



1) If μ_n (the electron mobility) increases, the DC characteristic of the logic will move from ① to ②. (True/False)

2) If β_p of all the PFETs increases, the DC characteristic of the logic will move from ① to ③. (True/False)

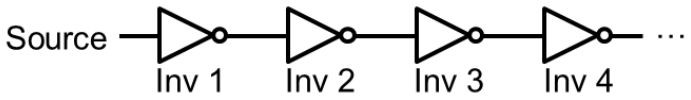
3) If β_n of the NFET connected to input C increases, the DC characteristic of the logic will move from ① to ③. (True/False)

4) If the threshold voltages of all the NFETs increase (due to the body-bias effect), the DC characteristic of the logic will move from ① to ②. (True/False)

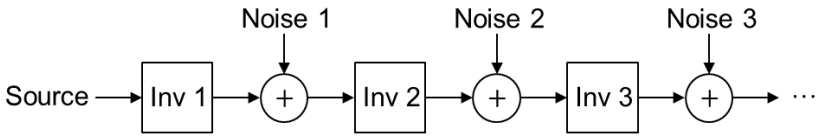
5) If the length of the PFET connected to input B increases, the DC characteristic of the logic will move from ① to ②. (True/False)

Problem #4 (DC Analysis, 20 points)

An infinite chain of inverters is defined as follows:

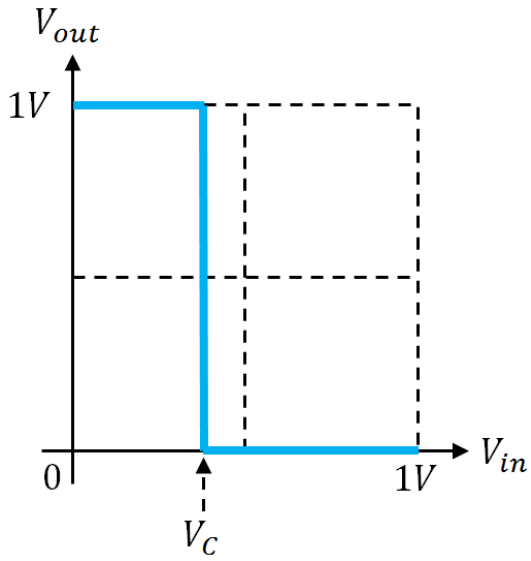


All the inverters are identical, i.e., have the same characteristics. The above chain is modeled as a block diagram as follows:



where $Noise\ k$ is the k-th noise and $Source$ is a signal generator and $V_{Source} = V_{DD} \cdot u(t)$ (i.e., 0 if $t < 0$ and V_{DD} if $t \geq 0$). $V_{DD} = 1V$. The signal source is either 0V (for logic 0) or 1V (for logic 1). All the noise sources are independent. For example, if the range of the value of each noise source is [-0.1V, 0.1V], the value of noise source 1 could be 0.05V while the value of noise source 2 is 0.07V and the value of noise source 3 is -0.03V.

1) The following shows the DC characteristics of the inverters. V_C is between 0V and 1V. If the range of the value of each noise source is $[0,0.3V]$ (i.e, $0V \leq noise \leq 0.3V$), <u>what is the minimum value of V_C that does not lead to signal inversion?</u> (5 points)



If the output of an inverter is t, it becomes $[t, t + 0.3]$ at the input of its next inverter. If the logical value of t is 1, $[t, t + 0.3]$ should be greater than V_C. If the logical value of t is 0, $[t, t + 0.3]$ should be less than V_C. Thus, $t > V_C$ and $t + 0.3 < V_C$ should be satisfied. If

t is 1V for the signal source, it is always greater than V_C. If t is 0V for the signal source, $t + 0.3V = 0.3V$ should always be less than V_C. Thus, the minimum value of V_C is 0.3V.

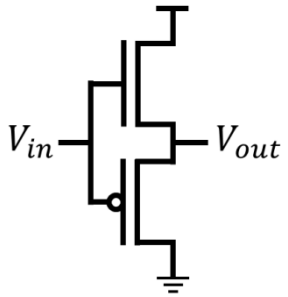
2) Assume that all the inverters follow the DC characteristic curve shown above. If the range of the value of each noise source is $[-0.1V, 0.2V]$ (i.e, $-0.1V \leq noise \leq 0.2V$), what is the minimum value of V_C that does not lead to signal inversion? (5 points) What is the maximum value of V_C that does not lead to signal inversion? (5 points)

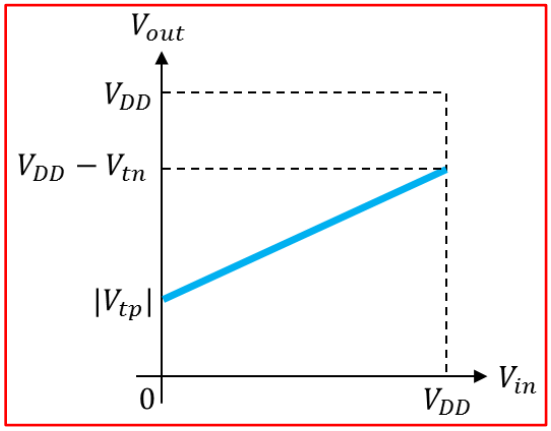
We apply the same analysis to find min. and max. of V_C. If the output of an inverter is t, it becomes $[t - 0.1, t + 0.2]$ at the input of its next inverter. If the logical value of t is 1, $[t - 0.1, t + 0.2] = [0.9V, 1.2V]$ should be greater than V_C. If the logical value of t is 0, $[t - 0.1, t + 0.2] = [-0.1V, 0.2V]$ should be less than V_C. Thus, V_C should be less than 0.9V and greater than 0.2V.

Min: 0.2V

Max: 0.9V

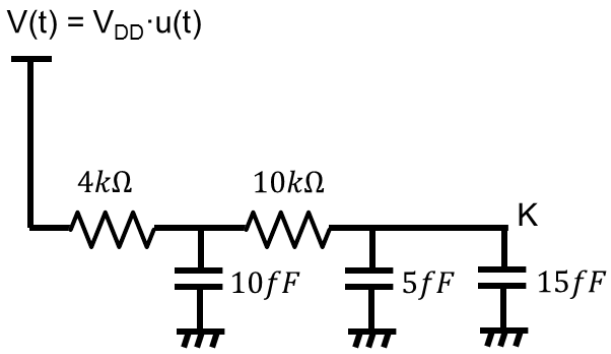
3) Draw a DC characteristic curve for the following buffer circuit. (5 points)
   - V_{tn}: Threshold voltage of the NFET.
   - V_{tp}: Threshold voltage of the PFET.
   - You don't need to derive equations or formulas to draw it. Just a rough sketch will be accepted.
   - However, you should show the output values for $V_{in} = 0$ and $V_{in} = V_{DD}$.





Problem #5 (Elmore Delay, 5 points)

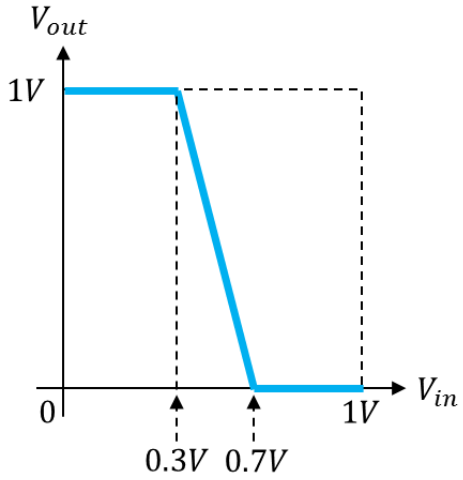
Compute the Elmore delay at node K.



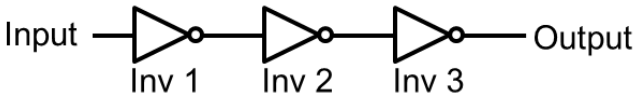
$$\tau = 10k * 20f + 4k * 30f = 200p + 120p = 320ps$$

Problem #6 (DC Analysis, 15 points)

The following shows the DC characteristic curve of an inverter.



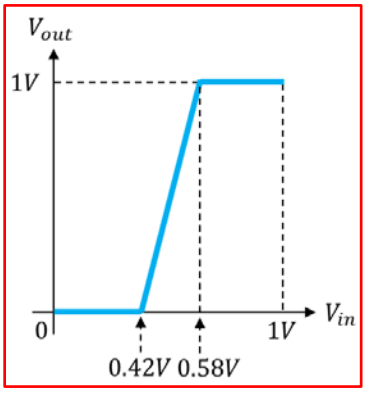
Draw a DC characteristic curve between the input and the output of the following inverter chain composed of three inverters whose DC characteristics follow the graph shown above. Note: The DC curve you draw should be very accurate, i.e., show all the important values such as x-intercepts, y-intercepts, etc.



The equation of the straight line in the middle is as follows:

$$y = -2.5x + 1.75$$

Thus, the output is 0.7V when the input is 0.42V. Similarly, the output is 0.3V when the input is 0.58V. Thus, the combined DC characteristic of the first two inverters is as follows:



The equation of the straight line in the middle is as follows:

$$y = 6.25x - 2.625$$

Thus, the output is 0.7V when the input is 0.532V. Similarly, the output is 0.3V when the input is 0.468V. Thus, the DC characteristic of the whole circuit is as follows: