EE434

ASIC and Digital Systems

Midterm Exam 2

Mar. 28, 2018. (4:10pm – 5pm)

Instructor: Dae Hyun Kim (daehyun@eecs.wsu.edu)
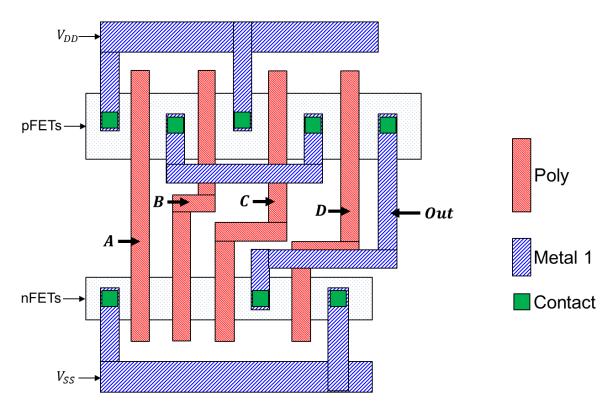
Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	20	
5	5	
6	15	
Total	70	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches
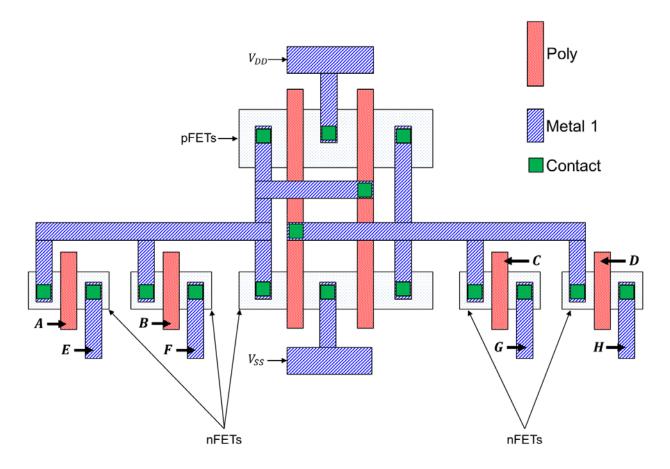
Problem #1 (Layout, 10 points)

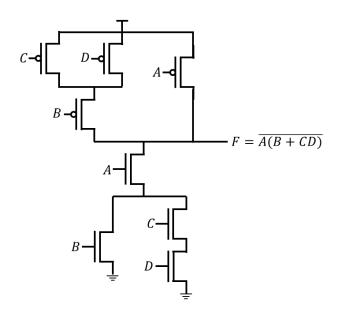Represent Out as a Boolean function of A, B, C, D.

Problem #2 (Layout, 10 points)

Draw a transistor-level schematic (netlist) for the following layout. Input ports: A, B, C, D. Inout (input/output) ports: E, F, G, H.
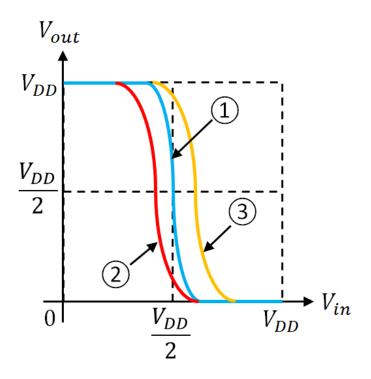
Problem #3 (DC Analysis, 10 points)

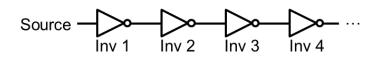The following schematic implements $F = \overline{A(B + CD)}$.

The following shows a DC characteristic graph of the logic above. Currently, the DC characteristic of the above logic follows the curve ①.
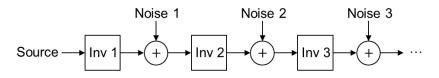
1) If μ_n (the electron mobility) increases, the DC characteristic of the logic will move from ① to ②. (True/False)

2) If β_p of all the PFETs increases, the DC characteristic of the logic will move from ① to ③. (True/False)

3) If β_n of the NFET connected to input C increases, the DC characteristic of the logic will move from ① to ③. (True/False)

4) If the threshold voltages of all the NFETs increase (due to the body-bias effect), the DC characteristic of the logic will move from ① to ②. (True/False)

5) If the length of the PFET connected to input B increases, the DC characteristic of the logic will move from ① to ②. (True/False)

Problem #4 (DC Analysis, 20 points)

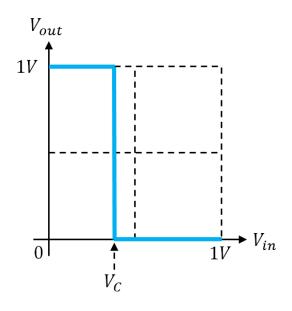An infinite chain of inverters is defined as follows:

All the inverters are identical, i.e., have the same characteristics. The above chain is modeled as a block diagram as follows:
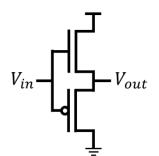

where $Noise\ k$ is the k-th noise and $Source$ is a signal generator and $V_{Source} = V_{DD} \cdot u(t)$ (i.e., 0 if $t < 0$ and V_{DD} if $t \geq 0$). $V_{DD} = 1V$. The signal source is either 0V (for logic 0) or 1V (for logic 1). All the noise sources are independent. For example, if the range of the value of each noise source is [-0.1V, 0.1V], the value of noise source 1 could be 0.05V while the value of noise source 2 is 0.07V and the value of noise source 3 is -0.03V.

1) The following shows the DC characteristics of the inverters. V_C is between 0V and 1V. If the range of the value of each noise source is $[0,0.3V]$ (i.e, $0V \leq noise \leq 0.3V$), <u>what is the minimum value of V_C that does not lead to signal inversion?</u> (5 points)
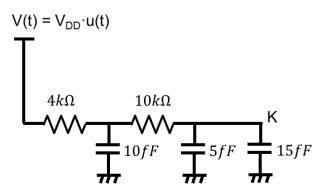
2) Assume that all the inverters follow the DC characteristic curve shown above. If the range of the value of each noise source is $[-0.1V, 0.2V]$ (i.e, $-0.1V \leq noise \leq 0.2V$), <u>what is the minimum value of V_C that does not lead to signal inversion?</u> (5 points) <u>What is the maximum value of V_C that does not lead to signal inversion?</u> (5 points)

3) Draw a DC characteristic curve for the following buffer circuit. (5 points)
- V_{tn}: Threshold voltage of the NFET.
- V_{tp}: Threshold voltage of the PFET.
- You don't need to derive equations or formulas to draw it. Just a rough sketch will be accepted.
- However, you should show the output values for $V_{in} = 0$ and $V_{in} = V_{DD}$.
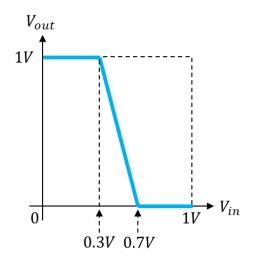
Problem #5 (Elmore Delay, 5 points)

Compute the Elmore delay at node K.

$$V(t) = V_{DD} \cdot u(t)$$

Node A (after $4k\Omega$) has $10fF$. Node K (after $10k\Omega$) has $5fF + 15fF = 20fF$.

Shared resistances to node K:
- $10fF$ cap: $R = 4k\Omega$
- $20fF$ cap: $R = 4k\Omega + 10k\Omega = 14k\Omega$

$$\tau_K = (10fF)(4k\Omega) + (20fF)(14k\Omega) = 40\,ps + 280\,ps = 320\,ps$$

Problem #5 (Elmore Delay, 5 points)

Compute the Elmore delay at node K.

$$V(t) = V_{DD} \cdot u(t)$$

$4k\Omega \qquad 10k\Omega$

K

$10fF \qquad 5fF \qquad 15fF$

Problem #6 (DC Analysis, 15 points)

The following shows the DC characteristic curve of an inverter.

Draw a DC characteristic curve between the input and the output of the following inverter chain composed of three inverters whose DC characteristics follow the graph shown above. Note: The DC curve you draw should be very accurate, i.e., show all the important values such as x-intercepts, y-intercepts, etc.