Advanced Techniques in CMOS Logic Circuits

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References

- John P. Uyemura, “Introduction to VLSI Circuits and Systems,” 2002.
  - Chapter 9

Goal

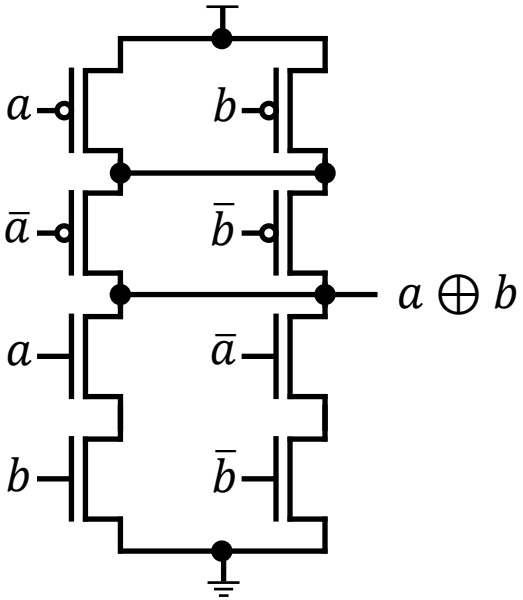
- Understand various advanced logic design techniques
  - Mirror circuits
  - Pseudo-nMOS
  - Tri-state circuits
  - Clocked CMOS
  - Dynamic CMOS
  - Dual-rail logic

Mirror Circuits

- Uses the same transistor topology for the nFET and pFET networks.
- When there are equal numbers of input combinations producing 0s and 1s.
  - XOR
  - XNOR
  - …
- Advantages
  - More symmetric layouts
  - Shorter rise and fall times

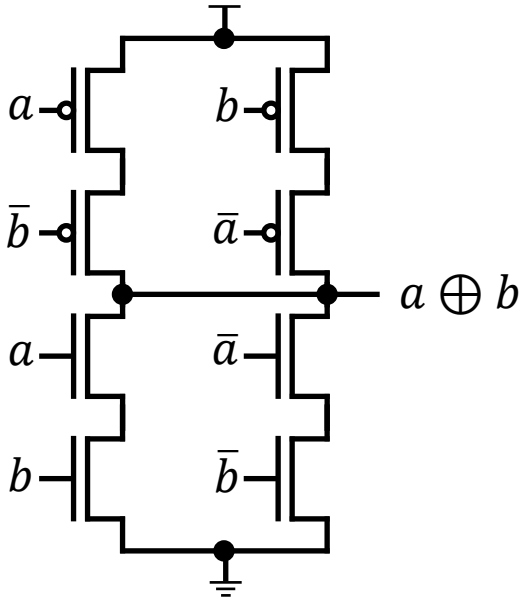
Mirror Circuits

- XOR



Traditional static CMOS

$$\tau_n = 2R_nC_{out} + R_nC_x$$
$$\tau_p = 2R_pC_{out} + R_p(2C_x)$$

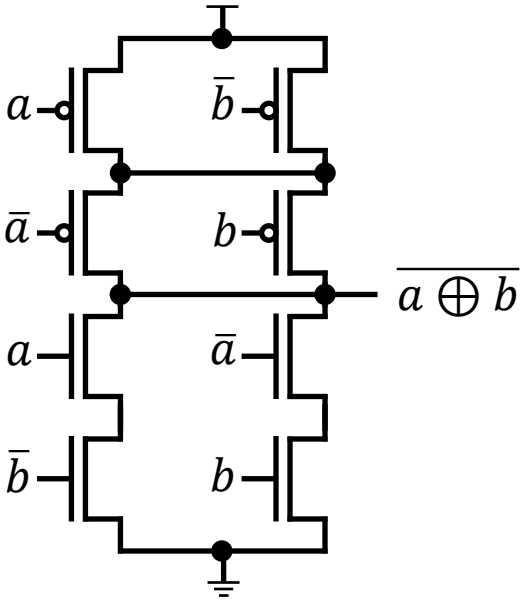


Mirror circuit

$$\tau_n = 2R_nC_{out} + R_nC_x$$
$$\tau_p = 2R_pC_{out} + R_pC_x$$

Mirror Circuits

- XNOR



Traditional static CMOS

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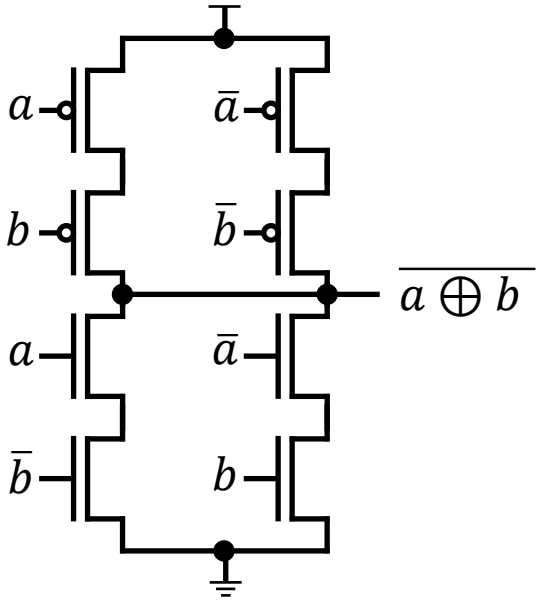
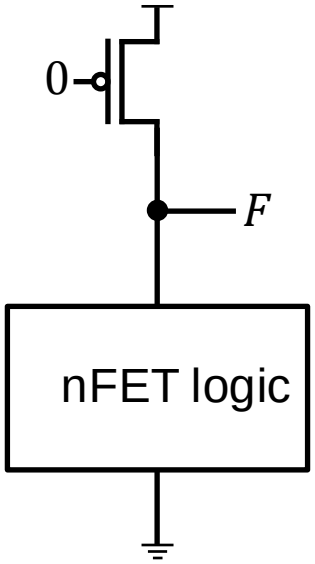


Mirror circuit

$$\tau_n = 2R_nC_{out} + R_nC_x$$
$$\tau_p = 2R_pC_{out} + R_pC_x$$

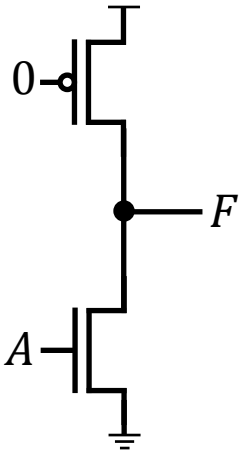
Pseudo-NMOS

- Ratioed logic
- If the nFET logic is turned off, $F = 1$.
- If the nFET logic is turned on, $F = 0$ (ideally).
- V_{OL} is determined by the resistance ratio between the pFET and the nFETs.
- Smaller, but $V_{OL} > 0$.
- Static power consumption.



Pseudo-NMOS

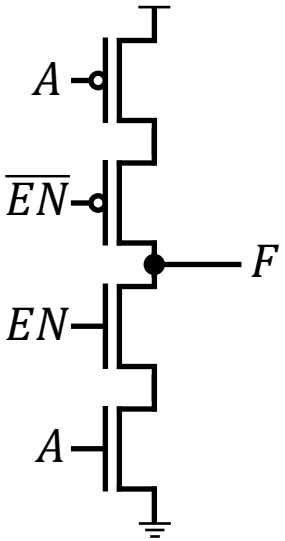
- Pseudo-NMOS inverter



- If $A = 0$: $F = V_{DD}$.
- If $A = 1$
  - nFET: $V_{GS} - V_{Tn} = V_{DD} - V_{Tn} > V_{DS} = V_{out}$
  - pFET: $V_{SG} - |V_{Tp}| = V_{DD} - |V_{Tp}| < V_{SD} = V_{DD} - V_{out}$
  - Linear region.
  - $I_{DSn} = \beta_n \left[(V_{DD} - V_{Tn}) V_{out} - \frac{1}{2} {V_{out}}^2 \right] = I_{SDp} = \frac{1}{2} \beta_p (V_{DD} - |V_{Tp}|)^2$
  - $V_{OL} = (V_{DD} - V_{Tn}) - \sqrt{(V_{DD} - V_{Tn})^2 - \frac{\beta_p}{\beta_n} (V_{DD} - |V_{Tp}|)^2}$

Tri-State Circuits

- Tri-state inverter
  - $EN = 1: F = \bar{A}$
  - $EN = 0: F = Z$



Clocked CMOS

- C^2MOS