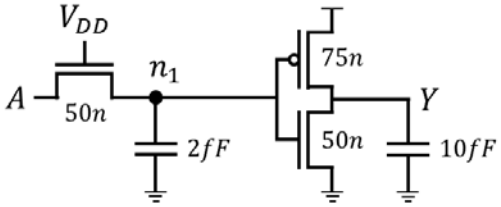
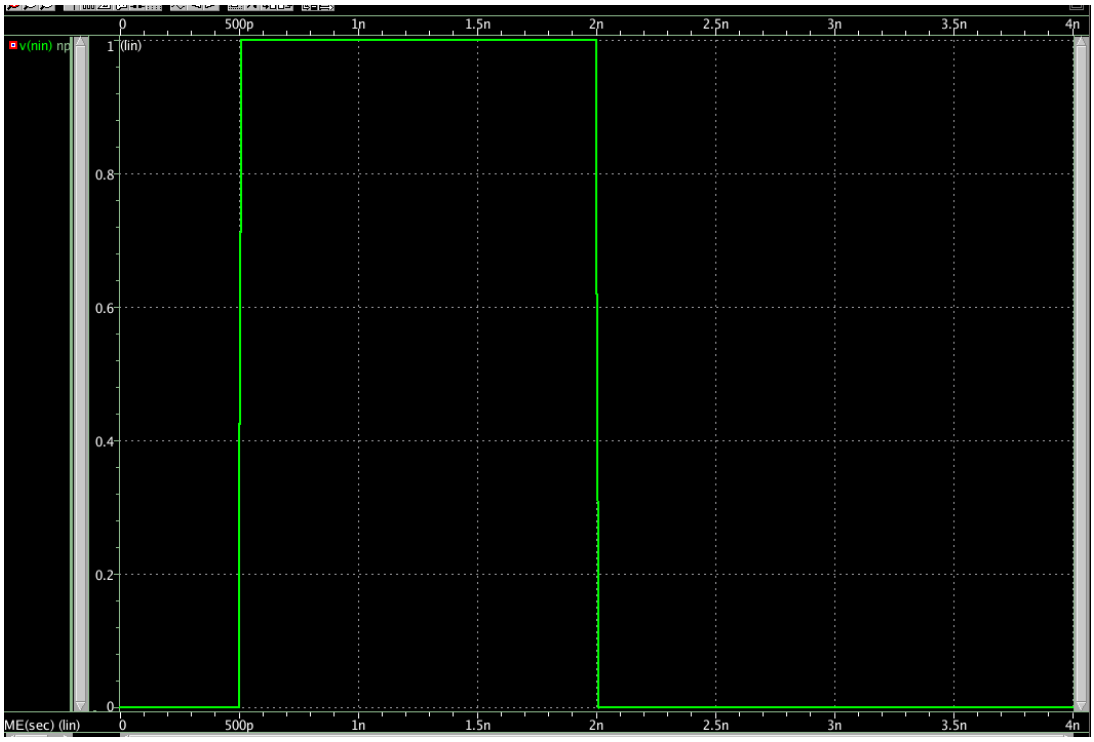
Homework Assignment 6
(Due 5pm, Feb. 5, email to daehyun@eecs.wsu.edu)

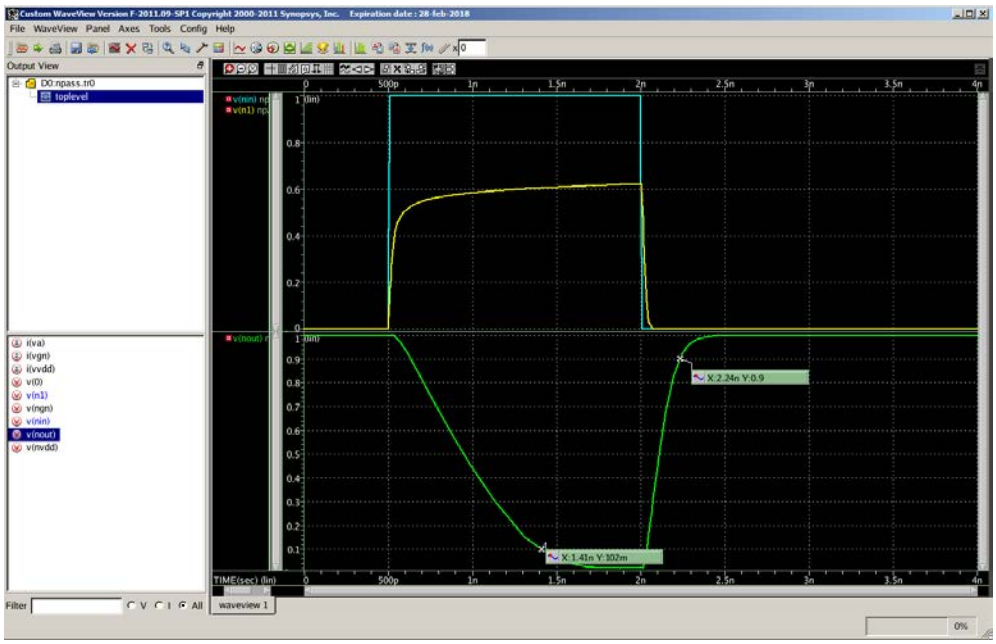
(1) **[Pass Transistor – NFET, 15 points]** The following shows a schematic for testing an NFET pass transistor. All the transistors have the minimum length (45nm) and the width of each transistor is shown in the figure.



Generate the following input signal and apply it to node A. The transition time is 10ps.

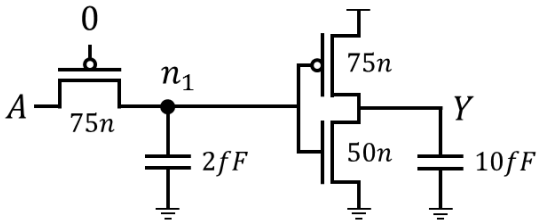


[**Submit**] Find the rise delay and the fall delay at the output node (Y). Notice that the rise delay is measured by $b - a$ where b is the time when the output reaches 0.9V and a is the time when the input starts switching. The fall time is defined in a similar way (b is the time when the output reaches 0.1V). Show (screen-capture) the waveforms at node A (input), node n_1, and node Y (output).

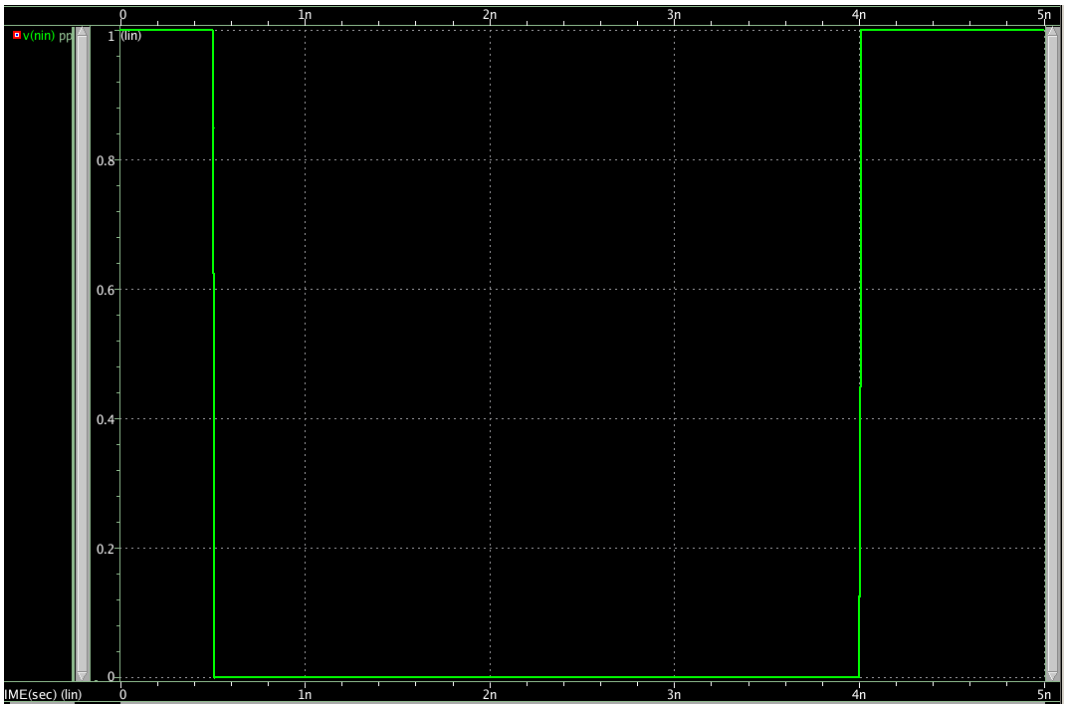


Rise delay: 240ps, Fall delay: 910ps

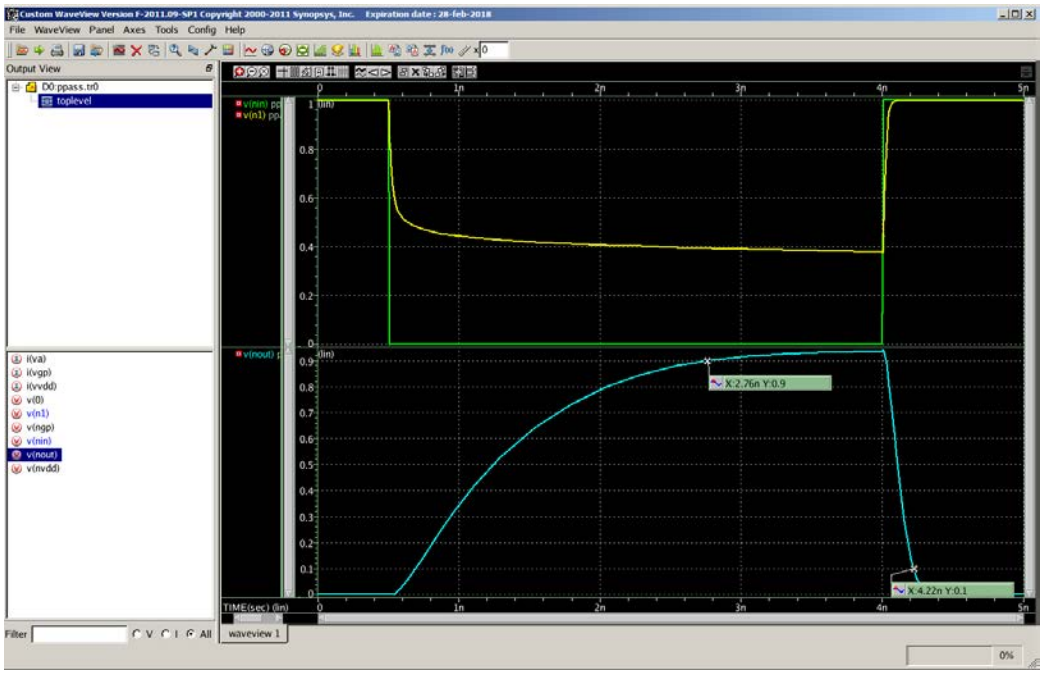
(2) **[Pass Transistor – PFET, 15 points]** The following shows a schematic for testing a PFET pass transistor. All the transistors have the minimum length (45nm) and the width of each transistor is shown in the figure. Notice that the bodies of the PFETs should be connected to VDD.



Generate the following input signal and apply it to node A. The transition time is 10ps.

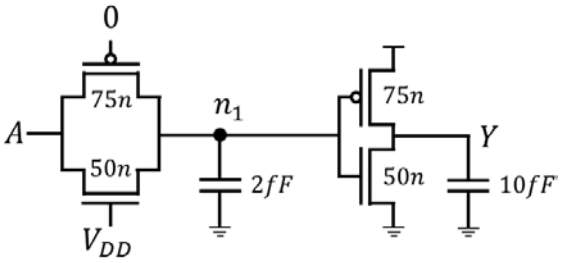


[**Submit**] Find the rise delay and the fall delay at the output node (Y). Notice that the rise delay is measured by $b - a$ where b is the time when the output reaches 0.9V and a is the time when the input starts switching. The fall time is defined in a similar way (b is the time when the output reaches 0.1V). Show (screen-capture) the waveforms at node A (input), node n_1, and node Y (output).

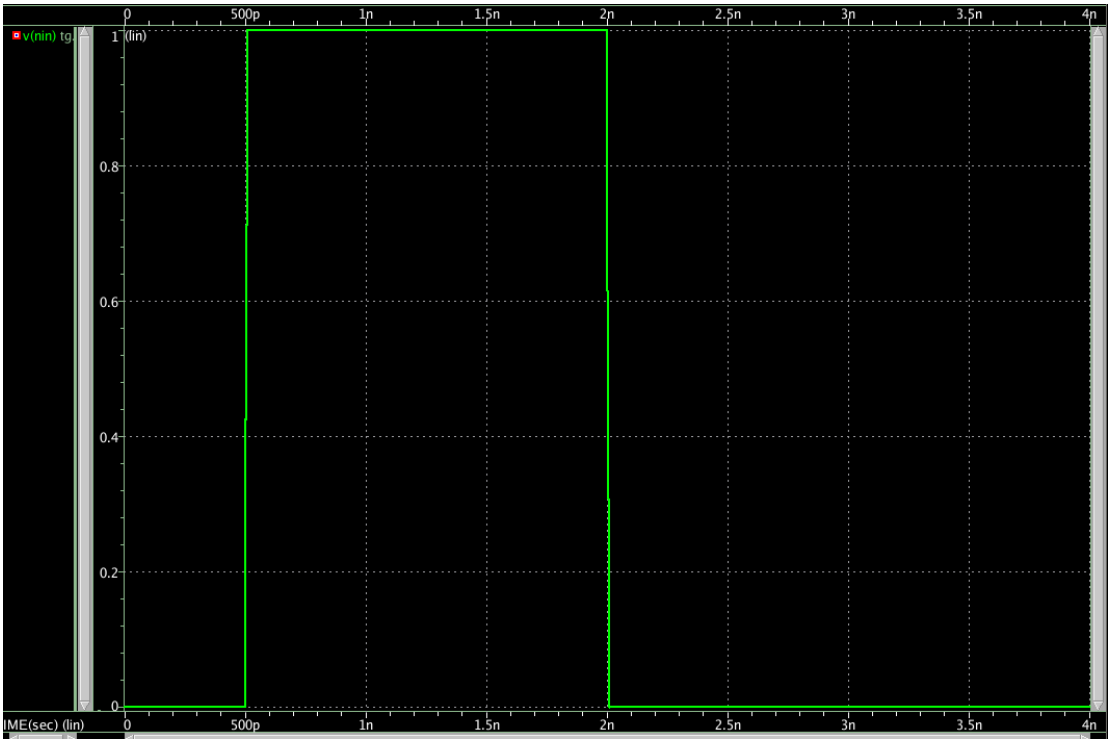


Rise delay: 2.26ns, Fall delay: 220ps

(3) **[Transmission Gate, 20 points]** The following shows a schematic for testing a transmission gate. All the transistors have the minimum length (45nm) and the width of each transistor is shown in the figure. Notice that the bodies of the PFETs should be connected to VDD and those of the NFETs should be connected to the ground.

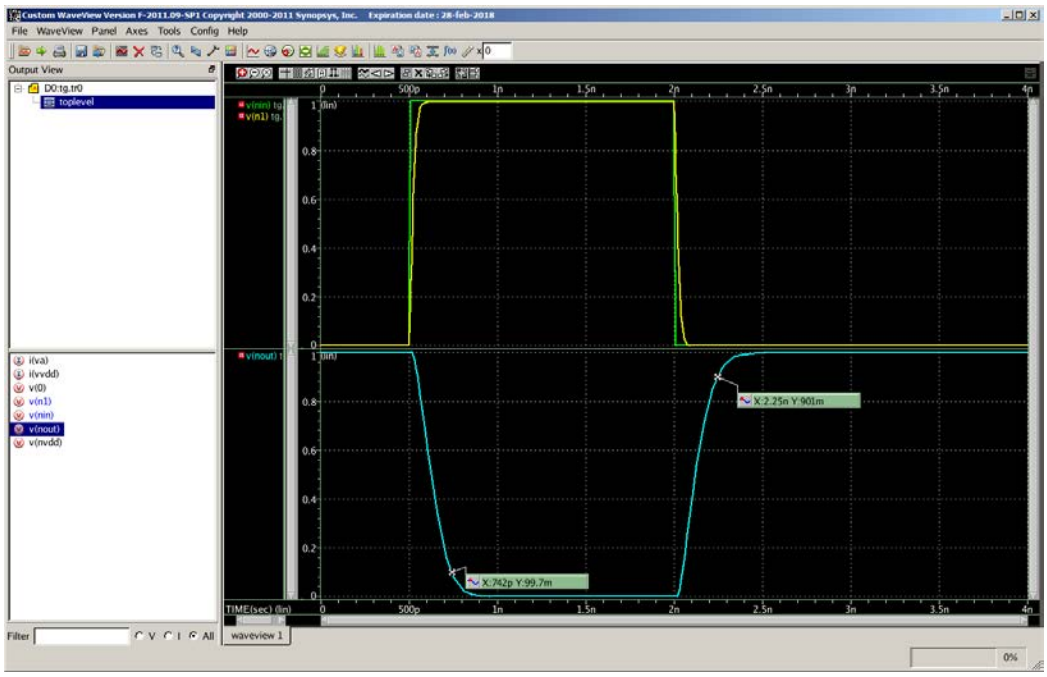


Generate the following input signal and apply it to node A. The transition time is 10ps.



[**Submit**] Find the rise delay and the fall delay at the output node (Y). Notice that the rise delay is measured by $b - a$ where b is the time when the output reaches 0.9V and a is the time when the input starts switching. The fall time is defined in

a similar way (b is the time when the output reaches 0.1V). Show (screen-capture) the waveforms at node A (input), node n_1, and node Y (output).



Rise delay: 250ps, Fall delay: 242ps