

**Homework Assignment 7**  
(Due 4:10pm, Feb. 9, email to [daehyun@eecs.wsu.edu](mailto:daehyun@eecs.wsu.edu))

- (1) [Process Variation, 20 points] A fabrication process has several uncontrollable process variation sources, so the length or the width of a transistor has some variations. To simulate the variation, we will assume that each variation follows the Gaussian (normal) distribution function. First, download “hw07.zip” from the class website. Unzip it and you will see inv.sp and dly.pl. inv.sp is an HSpice netlist simulating an inverter with some variations. dly.pl is a Perl script to compute some statistics of the simulation result. “sweep monte = N” in the netlist tells HSpice to perform the Monte Carlo simulation N times. The width of each transistor is not a constant, rather it is defined by the “agauss” function, which is `agauss(default value, variation value, sigma)`. Run “`hspice inv.sp > inv.out`” to perform the Monte Carlo simulation (N=100) and dump the output messages into the file “inv.out”. Once the simulation is done, you will see “\*\*\*\*\* hspice job concluded”.

Once the HSpice simulation is done, run “`perl dly.pl inv.out`” to parse the output file and obtain the statistics of the simulation. It will print out something like this.

# fall delay values: # (# simulations)

Min. fall delay

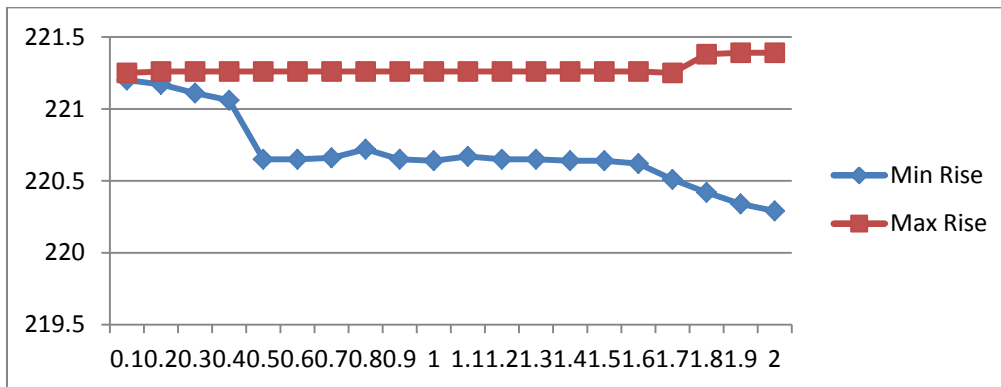
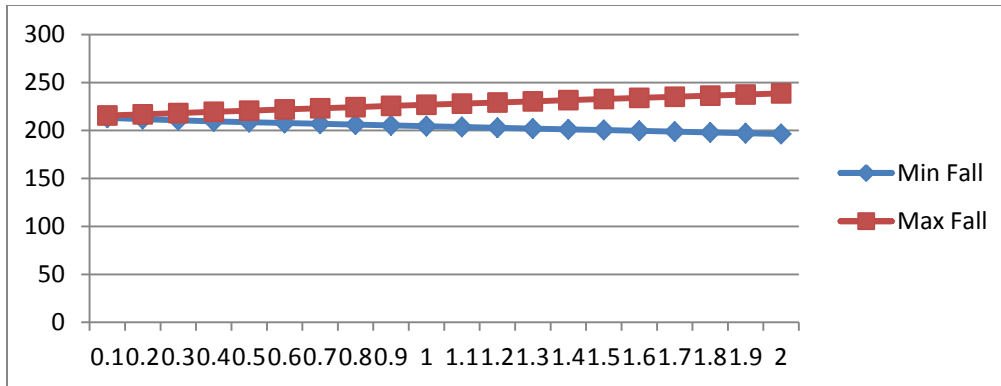
Max. fall delay

Avg. fall delay (average)

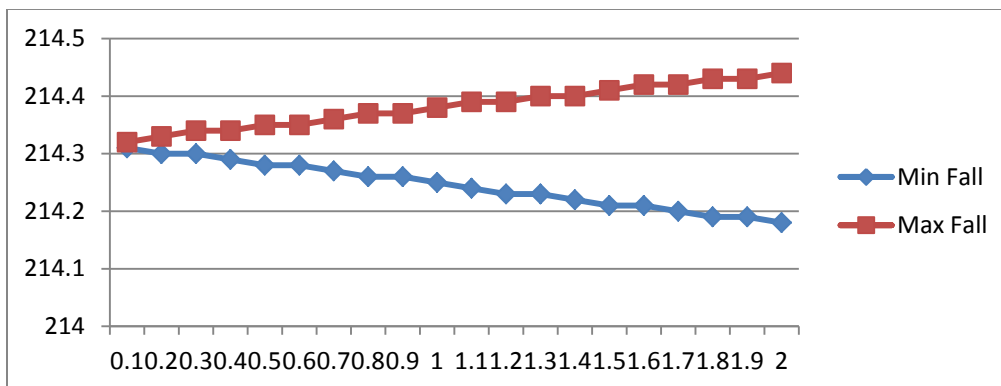
Sigma (Standard deviation)

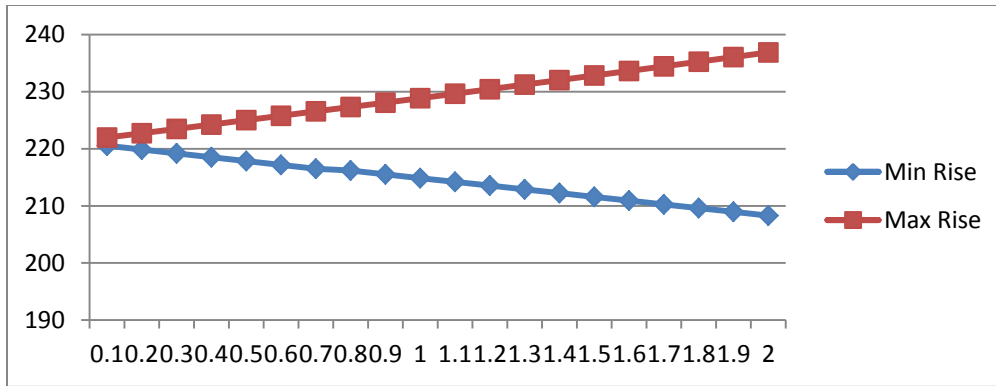
Set the width of the PFET to 75nm (no variation) and that of the NFET to `agauss(50n, Xn, 1)` where X is (0.1, 0.2, ..., 2.0). Simulate inv.sp for each X and find the min. fall delay and the max. fall delay for each X.

[Submit] Plot X vs. min. fall delay. Plot X vs. max. fall delay. Plot X vs. min. rise delay. Plot X vs max. rise delay.



(2) [Process Variation, 20 points] Set the width of the NFET to 50nm (no variation) and that of the PFET to agauss (75n, Xn, 1) where X is (0.1, 0.2, ..., 2.0). Simulate inv.sp for each X and find the min. fall delay and the max. fall delay for each X. [Submit] Plot X vs. min. fall delay. Plot X vs. max. fall delay. Plot X vs. min. rise delay. Plot X vs max. rise delay.





(3) [Process Variation, 20 points] Set the width of the NFET to agauss (50n, 1n, 1) and that of the PFET to 75n, run the MC simulation 10,000 times, and obtain the min fall delay (fn\_min), max fall delay (fn\_max), min rise delay (rn\_min), and max rise delay (rn\_max). Then, set the width of the NFET to 50n and that of the PFET to agauss (75n, 1n, 1), run the MC simulation 10,000 times, and obtain the min fall delay (fp\_min), max fall delay (fp\_max), min rise delay (rp\_min), and max rise delay (rp\_max). Then, set the width of the NFET to agauss (50n, 1n, 1) and that of the PFET to agauss (75n, 1n, 1), run the MC simulation 10,000 times, and obtain the min fall delay (fnp\_min), max fall delay (fnp\_max), min rise delay (rnp\_min), and max rise delay (rnp\_max). [Submit] Submit the 12 min/max fall/rise delay values.

fn_min	197.47
fn_max	233.4
rn_min	220.48
rn_max	221.26
fp_min	214.21
fp_max	214.45
rp_min	207.55
rp_max	233.22
fnp_min	197.52
fnp_max	233.4
rnp_min	207.75

rnp_max	233.07
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Compare the following values (use < and > symbols. for example, fn\_min<fp\_min<fnp\_min).

- (a) fn\_min, fp\_min, fnp\_min: **fn\_min<fnp\_min<fp\_min**
- (b) fn\_max, fp\_max, fnp\_max: **fp\_max<fn\_max=fnp\_max**
- (c) rn\_min, rp\_min, rnp\_min: **rnp\_min<rp\_min<rn\_min**
- (d) rn\_max, rp\_max, rnp\_max: **rn\_max<rnp\_max<rp\_max**