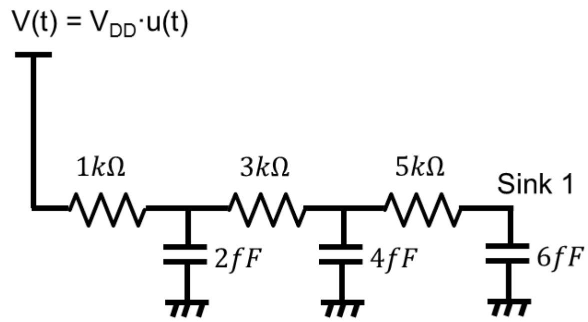
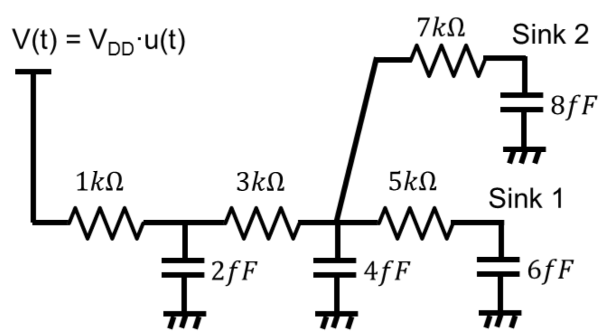
Homework Assignment 13
(Due 4:10pm, Mar. 23, email to daehyun@eecs.wsu.edu)

(1) **[Elmore Delay, 10 points]** Compute the Elmore delay from the source to Sink 1.



$\tau = 5k * 6f + 3k * 10f + 1k * 12f = 30p + 30p + 12p = 72ps$

(2) **[Elmore Delay, 10 points]** Compute the Elmore delays from the source to Sink 1 and Sink 2.

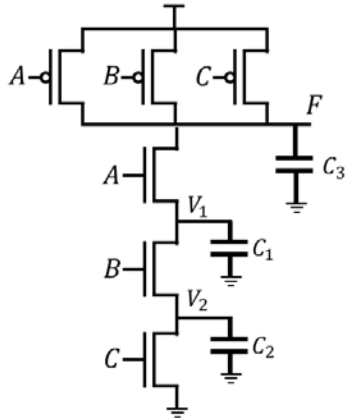


Sink 1: $\tau = 5k * 6f + 3k * 18f + 1k * 20f = 30p + 54p + 20p = 104ps$

Sink 2: $\tau = 7k * 8f + 3k * 18f + 1k * 20f = 56p + 54p + 20p = 130ps$

(3) **[AC Analysis, 10 points]** The following figure implements a three-input NAND gate. C_1 and C_2 are small parasitic capacitances. C_3 is an output capacitance. Use $R_{n,A}, R_{n,B}, R_{n,C}$ for the equivalent resistance values for the NFETs connected to A, B, C, respectively, and $R_{p,A}, R_{p,B}, R_{p,C}$ for the equivalent resistance values for the PFETs connected to A, B, C, respectively. Assume that $V_1(t)$ and $V_2(t)$ are V_{DD} before the inputs switch. Compute the Elmore delay (i.e., express the delay as

a function of the resistance and capacitance variables shown above) to estimate the fall delay at the output node when the input ABC switches from 000 to 111.



$$\tau = R_{n,A}C_3 + R_{n,B}(C_1 + C_3) + R_{n,C}(C_1 + C_2 + C_3)$$

(4) **[AC Analysis, 10 points, use the 3-input NAND gate schematic in Problem 3]** Assume that $V_1(t)$ and $V_2(t)$ are 0V before the inputs switch. Compute the Elmore delay to estimate the rise delay at the output node when the input ABC switches from 111 to 010.

$$\tau = \frac{R_{p,A}R_{p,C}}{R_{p,A} + R_{p,C}} C_3$$