Homework Assignment 19
(Due 4:10pm, Apr. 25, email to daehyun@eecs.wsu.edu)

1. [VHDL, **20 points**] Make a VHDL code for a 4:1 mux and test it with the following spec.
   - Input ports: i0, i1, i2, i3 (four data inputs), s1, s0 (two selection inputs)
   - Output port: z
   - Function: z=i0 (when s1s0=00), z=i1 (when s1s0=01), z=i2 (when s1s0=10), z=i3 (when s1s0=11)
   - Test input vectors (i3i2i1i0s1s0): All the 64 values from 000000 to 111111
     - 000000 → 000001 → 000010 → 000011 → 000100 → 000101 → …
   - [**Submit**] Source code + waveform (inputs + output)

2. [VHDL, **20 points**] Make a VHDL code for a positive-edge-triggered D-F/F with an active-high asynchronous set and an active-high synchronous reset. Use the following spec.
   - Input ports: D (data input), CK (clock), S (set), R (reset)
   - Output ports: Q
   - Function
     - If S=1, Q=1 (asynchronously).
     - If S=0 and R=1, Q=0 at the next rising clock edge (synchronous).
     - If S=0 and R=0, it is just a normal positive-edge-triggered D-F/F.
   - Test input vectors (D, S, R, CK)
     - 0000 → 0001 → 0000 → 1000 → 1001 → 1000 → 0000 → 0001 → 0000 → 0100 → 0101 → 0100 → 0010 → 0001 → 0000 → 0110 → 0111 → 0110
   - [**Submit**] Source code + waveform (inputs + output)