Lab 1
(Due 23:59:59, Apr. 29th)

Draw a layout for a positive-edge-triggered D-F/F (primary inputs: D, CK, $\overline{CK}$ primary outputs: Q, $\bar{Q}$). Do not use Metal 2 to Metal 10 layers. Run DRC, LVS, and PEX. Once you get a netlist with parasitic RC, run HSpice to obtain rise and fall delay values. You need to create proper input waveforms to test the rise and fall delays at Q. The following shows some specifications you should satisfy:

- Load capacitance: 10fF
- T_{CQ} delay for the given load cap: 50ps
- Total transistor width $\leq$ 4,000nm (4um)

Tips

- Draw a schematic first and properly size the transistors.
- Run HSpice simulation.
- Draw a layout and run DRC, LVS, PEX.
- Refer to the D-F/F schematic shown in the lecture notes.

Submit

- Layout snapshot
- Transistor-level schematic (with the size of each transistor)
- DRC, LVS, PEX reports
    - Do not print them out. You can just zip the report files and send it to me by email).
- Input and output waveforms (use WaveView).
- The worst-case rise and fall delays at Q.