#### EE434 ASIC & Digital Systems

# Automatic Layout Generation (Encounter)

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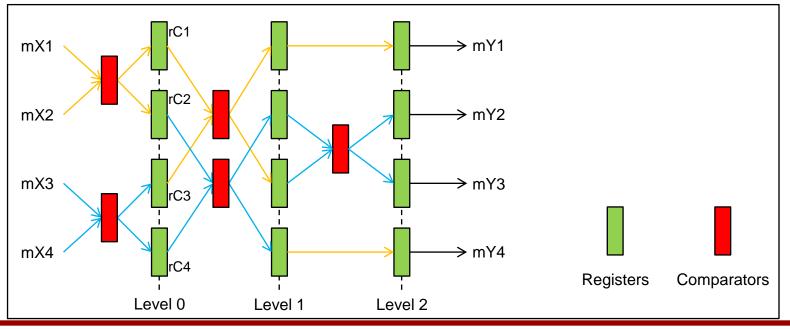
#### **Preparation for Lab3**

- Download the following file into your working directory.
   wget http://eecs.wsu.edu/~ee434/Labs/lab3.tar.gz
- Unzip it.
  - tar xvfz lab3.tar.gz

# What We Are Going To Do

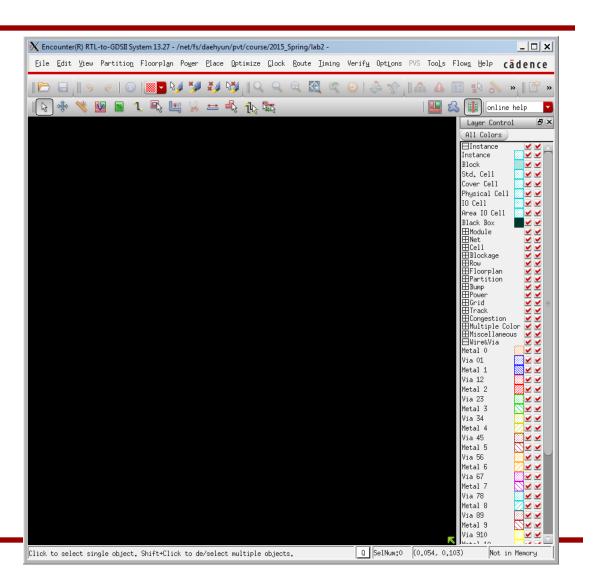
- 1. Chip outlining
- 2. P/G network design
- 3. Placement
- 4. Pre-CTS optimization
- 5. CTS
- 6. Post-CTS optimization
- 7. Routing
- 8. Post-routing optimization
- 9. Fill insertion

- Benchmark
  - VQS64\_4 (four-input 64-bit pipelined quick sort)
    - input [63:0] mX1, mX2, mX3, mX4
    - input mCLK
    - output [63:0] mY1, mY2, mY3, mY4



- VQS64\_4\_fm.globals
  - init\_pwr\_net: Power nets.
  - init\_gnd\_net: Ground nets.
  - init\_lef\_file: Physical library files.
  - init\_mmmc\_file: Analysis view files.
    - mmmc: Multi-mode multi-corner
  - init\_verilog: Verilog netlists.
- VQS64\_4\_fm.view
  - create\_rc\_corner: Capacitance table + RC analysis corner
  - create\_library\_set: Library files
  - create\_constraint\_mode: Constraint files
  - create\_delay\_corner: Library + RC corner
  - create\_analysis\_view: Analysis view
  - set\_analysis\_view: Setup and hold analysis view

- Source "edi.sh".
  - % source edi.sh
- Run Encounter.
  - % encounter



- Click "File"  $\rightarrow$  "Import Design...".
- In the "Design Import" window, click "Load..." and choose "VQS64\_4\_m.globals". This will automatically fill up the settings. Then, click "OK".

Wetlist:   • Verilog   Files:   • De   • Library:   • Cali:   • Cali:   • Cali:   • Verilog   • Cali:   • Cali:   • Cali:   • Cali:   • Verilog   • Cali:	🗙 Design Import	X Design Import
OR   Library:   Cell:   Visu:   Visu:   Visu:   Poer   Poer <t< td=""><td>● Verilog Files:</td><td> • Verilog Files: VQS64_4_m.v</td></t<>	● Verilog Files:	 • Verilog Files: VQS64_4_m.v
OR Reference Libraries: Abstract View Names: Layout View Names: Layout View Names: Lef Files Our Power Power Power Power Nets: Coround Nets: CPF File: Power Nets: WHYC View Definition File: WHYC View Definition File: WHYC View Definition File: OB OB Reference Libraries: Analysis Configuration WHYC View Definition File: WHYC View Definition File: OB Reference Libraries: Analysis Configuration WHYC View Definition File: WHYC View Definition File: OB OB Reference Libraries: Analysis Configuration WHYC View Definition File: WHYC View Definition File: OB O	OA	Cell:
Floorplan   IO Assignment File:   Power   Power Nets:   Ground Nets:   CPF File:   Philos   Analysis Configuration   WMC View Definition File:	OR     Reference Libraries:     Abstract View Names:     Layout View Names:	OR     Reference Libraries:     Abstract View Names:     Layout View Names:
Power Nets:       Power Nets:       VDD         Ground Nets:       Ground Nets:       VSS         CPF File:       CPF File:       CPF File:         Analysis Configuration       MHMC View Definition File:       MHMC View Definition File:	Floorplan IO Assignment File:	Floorplan IO Assignment File:
MMMC View Definition File: VQS64_4_m.view 🖻	Power Nets: Ground Nets: CPF File:	Power Nets: VDD Ground Nets: VSS CPF File:
OK Save (Load) (Lance) Help OK Save (Load) (Lance) Help	MMMC View Definition File: Create Analysis Configuration	MMMC View Definition File: VQS64_4_m.view Create Analysis Configuration

- See the terminal for Encounter messages. There might be some Error or Warning messages.
- In the Encounter main window, press "f" to see the outline of the layout.
- Encounter automatically computes and prepares the layout area.
- In the main window, click "Floorplan"  $\rightarrow$  "Specify Floorplan...".
- Set the core utilization to 0.6.
- Set the core-to-left, core-to-top, core-to-right, and core-to-bottom to 5.0.
- Then, click OK.

Specify Floorplan			,
Basic Advanced			
🦟 Design Dimensions —			
	Die /10 /Come Coondin		
Specify By: 🖲 Size 🥥	Die/IU/Core Coordin	ates	
🥑 Core Size by:	🥑 Aspect Ratio:	Ratio (H/W):	345392877
		◉ Core Utilization:	0.6
		◯ Cell Utilization:	0,699971
	🔾 Dimension:	Width:	88.45
		Height:	86.8
🔾 Die Size by:		Width:	88.45
		Height:	86.8
Core Margins by:🥑	Core to IO Boundary		
0	Core to Die Boundary	1	
	Core to Left:	5 Core to Top:	5
	Core to Right:	5 Core to Bottom:	5
Die Size Calculatio	n Use: 🔾 Max IO Hei	ight 🥑 Min IO Height	
Floorplan Origin at	: 💽 Lower Left Co	orner 🔾 Center	
			Unit: Micron
<u>OK</u>	Apply	Cancel	Help

• Now, you will see the following window.

X Encounter(R) RTL-to-GDSII System 13.27 - /net/fs/daehyun/pvt/course/2015_Spring/lab2 - VQ	QS64_4	_ 🗆 X
Eile Edit View Partition Floorplan Power Place Optimize Clock Route Timing	g Verify Opt <u>i</u> ons PVS Too <u>l</u> s Flow <u>s H</u> elp	cādence
। 🎦 🔚 🛛 🔅 🚺 🔛 😼 🎾 🧩 🖓 🔍 🔍 🔍 🖏	😧   🕭 🎲   🗛 🛕 💷 😵 እ	» 📔 🚰 »
I 🕞 🚸 帐 😐 🗉 🤇 🖳 🔛 🥉 🖴 🔩 🔃 🖏		ne help 🔽
Click to select single object. Shift+Click to de/select multiple objects.	Layer Cont All Colors:	Color Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y

#### Save

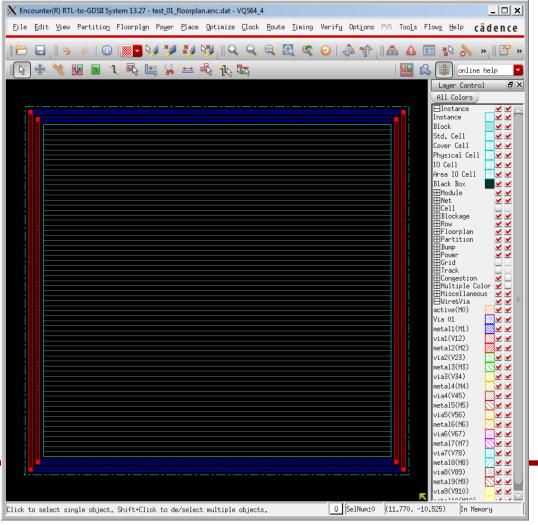
- Let's save the current design.
- In the terminal, run the following command to save the current design into "test\_01\_floorplan.enc".
   encounter #> saveDesign test\_01\_floorplan.enc
- Later on, you can load the design as follows.
  - When you launch Encounter, add the following option to load the specified design.
    - encounter –init test\_01\_floorplan.enc
  - or, after you launch Encounter, run the following command.
    - source test\_01\_floorplan.enc

• Click "Power"  $\rightarrow$  "Power Planning"  $\rightarrow$  "Add Rings...".

Add Rings					_ 🗆
asic Advanced	Via Genera	tion			
Net(s):VDD VSS					
Ring Type					
● Core ring(s) c ● Around core	-	◯ Along I/	0 boundary		
📃 Exclude sel	· ·	ts			
Block ring(s)	around				
Each block					
Each reef Selected point	uon domain/l	fancas/naafa			
-		tences/reets d/or group of cor	e rous		
		locks and/or grou		IS	
	ared ring ec				
◯ User defined c	oordinates:			TouseClick	2
🖲 Core ring	🔘 Bloc	sk ring			-
Ring Configurati	on				
Top:	Bottom				
		11 H 🕨 🔪 metal2 \			
Width: 1	1	1	1		
Spacing: 1	1	1	1	Update	
Offset: Offset:	~	· · · · · · · · · · · · · · · · · · ·			
0.095	0.095	0.095 0.0	35		
Option Set					
Edit Add Ring	Option )				
COIC HOD KING					
Euro Hou King			Jefaults		

• Fill in the input boxes as shown in the previous page and click

OK.



13

• Click "Route" → "Special Route...".

Basic Advanced Via Generation	
Net(s): VDD VSS	
SRoute	
🗹 Block Pins 🗹 Pad Pins 🗹 Pad Rings 🗹 Follow Pins 🗹 Floating Stripes 📃 Secondary Power Pins	
Routing Control	HI.
Layer Change Control	hl I
Top Layer: metal10 > Bottom Layer: metal1 >	
✓ Allow Jogging ✓ Allow Layer Change	
Area Power Domain Selection	
X2: View Area	
Connect to Target Inside The Area Only  I Delete Existing Routes	
Generate Progress Messages	
Mode Setup	
Target Editing Option	s
QK Apply Lefaults Cancel Help	

• P/G network

Eile Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options PVS Tools Flows Help Cadence
Image: Second secon
Instance       Instance         Insta
Image: Second

• saveDesign test\_02\_pg.enc

#### 3. Placement

- Let's place the instances (cells).
- In the main window, click "Place"  $\rightarrow$  "Place Standard Cell".
- In the following window, turn off "Include Pre-Place Optimization".

N Place
💿 Run Full Placement 🔾 Run Incremental Placement 🔾 Run Placement In Floorplan Mode
Optimization Options
Include Pre-Place Optimization Include In-Place Optimization
Number of Local CPU(s): 1 Set Multiple CPU
OK Apply Mode Lefaults Cancel Help

• Then, click "OK" to run Placement.

#### 3. Placement

- It shows placement and trialRoute results.
- See the terminal. It shows some more information.
  - Total wire length: 46,920um
- Save it.
  - saveDesign test\_03\_pl.enc

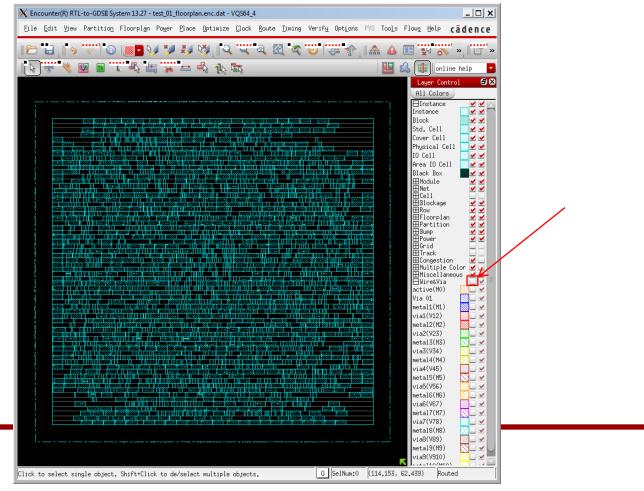
Total length:					
M1(H) length:	1.187e+03um,	number	of	vias:	9371
M2(V) length:	2.059e+04um,	number	of	vias:	6881
M3(H) length:	1.976e+04um,	number	of	vias:	506
M4(V) length:					
M5(H) length:	1.261e+03um,	number	of	vias:	68
M6(V) length:	7.066e+02um,	number	of	vias:	25
M7(H) length:	9.350e+00um,	number	of	vias:	8
M8(V) length:	6.480e+00um,	number	of	vias:	6
M9(H) length:	4.140e+00um,	number	of	vias:	0
M10(V) length	: 0.000e+00um				

K Encounter(R) RTL-to-GDSII System 13.27 - test_01_floorplan.enc.dat - VQS64_4	_ <b>_ X</b>
Eile Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options PVS Tools	Flows Help cādence
┃┣ ▃    ᠀ ╭   ᠐   <b>◎● <sup>い</sup>/ */ */ ѷ</b> /  ♀ ♀ ♀ ⊠ ९ ♀   ♣ ☆   & ▲     ┣ ♣ ♥ ≌ ≘ Ղ 록 ╚ % ⋍ 록 1∖ ┺	🔲 🕵 🚴 » 🛛 🕾 » A 🗊 online help 🔽
	Layer Control Layer Control R11 Colors H1stance H1stance Std, Cell Std, Cell

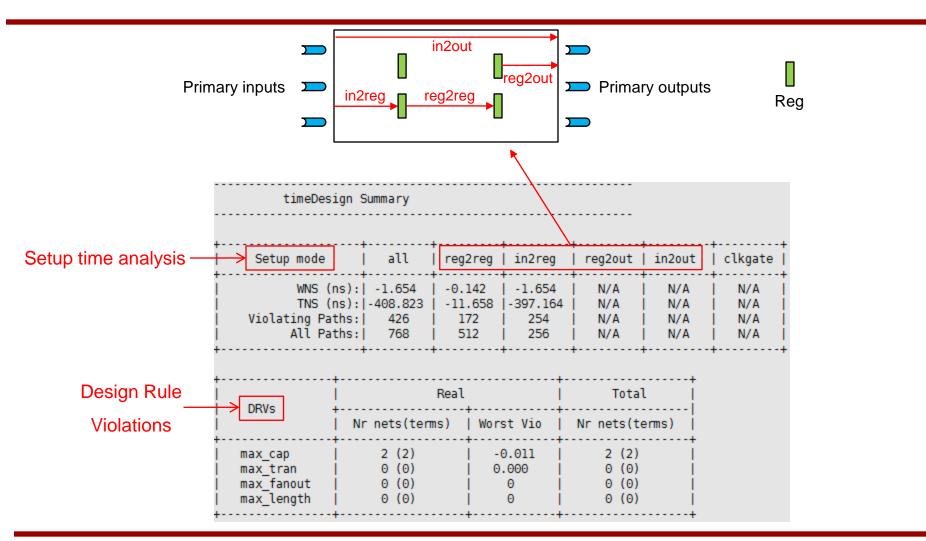
# Visibility

- Let's see the placement result only.
- Turn off the following check-box to turn off the visibility of the

wires.



- Run the following command to turn off SI-awareness.
   encounter #> setDelayCalMode –siAware false
- Then, run the following command to analyze setup time.
   encounter #> timeDesign –preCTS
- It will show the following summary:



#### • Run the following command to check the longest path.

#### – encounter #> report\_timing

Path 1: VIOLATED Set	tup Check with F	Pin rCl_reg[5	52]/CK		
	[52]/D (v) check				.K'
Beginpoint: mX2[1]	(^) trigg	gered by lea	ading edg	ge of '@'	
Analysis View: NG_vi	iew_typ				
Other End Arrival Ti	ime 0.0	900			
- Setup	0.0	947			
+ Phase Shift	1.0	900			
= Required Time	0.9	953			
- Arrival Time	2.6	506			
= Slack Time	-1.6	554			
Clock Rise Edge	e	0.000	9		
+ Input Delay		0.000	Ð		
= Beginpoint A	rrival Time	0.000	9		
+					+
Instance	Arc	Cell	Delay	•	Required
				Time	Time
				+	
111100	mX2[1] ^	TNU 1/7	0.010	0.000	-1.654
04103	A ^ -> ZN v	INV_X1	0.010	0.011	-1.643
U3853	C2 v -> ZN ^	0AI211_X1	0.034	0.045	-1.609
U3852	A ^ -> ZN v	0AI221_X1	0.034	•	-1.575
U3861	A v -> ZN ^	0AI221_X1	•	•	-1.549
U3860	A ^ -> ZN v	0AI221_X1	0.041	•	-1.508
U3859	A v -> ZN ^	0AI221_X1	0.028	•	-1.480
U3858	A ^ -> ZN v	0AI221_X1	0.040	0.214	-1.440
U3869	A v -> ZN ^	0AI221_X1	0.027	0.241	-1.413
U3868	A ^ -> ZN v	0AI221_X1	0.040	0.281	-1.372
U3867	A v -> ZN ^	0AI221_X1	0.029	0.311	-1.343
U3866	A ^ -> ZN v	0AI221_X1	0.041	0.352	-1.302
U3877	A v -> ZN ^	0AI221_X1	0.028	0.380	-1.274
U3876	A ^ -> ZN v	0AI221_X1	0.041	0.421	-1.233
U3875	A v -> ZN ^	0AI221_X1	0.028	0.449	-1.205
U3874	A ^ -> ZN v	0AI221_X1	0.041	0.490	-1.164
U3885	A v -> ZN ^	0AI221_X1	0.027	0.517	-1.137
U3884	A ^ -> ZN v	0AI221_X1	0.040	0.556	-1.097
U3883	A v -> ZN ^	0AI221_X1	0.027	0.584	-1.070
U3882	A ^ -> ZN v	0AI221_X1	0.040	0.624	-1.030
U3893	Av->ZN^	0AI221_X1	0.027	0.651	-1.003

U3946	A ^ -> ZN v	OAI221_X1	0.039	1.707	0.053
U3957	A v -> ZN ^	0AI221_X1	0.027	1.734	0.080
U3956	A ^ -> ZN v	0AI221 X1	0.040	1.774	0.120
U3955	A v -> ZN ^	0AI221 X1	0.029	1.803	0.149
U3954	A^-> ZN v	0AI221 X1	0.041	1.843	0.190
U3965	A v -> ZN ^	0AI221 X1	0.028	1.872	0.218
U3964	A ^ -> ZN ∨	0AI221_X1	0.042	1.914	0.260 İ
U3963	A v -> ZN ^	0AI221 X1	0.029	1.943	0.289 İ
U3962	A ^ -> ZN v	0AT221 X1	0.042	1.985	0.331
U3973	A v -> ZN ^	0AI221 X1	0.027	2.011	0.358
U3972	A^-> 7N v	0AI221 X1	0.040	2.051	0.397
U3971	A v -> ZN ^	0AI221 X1	0.026	2.077	0.424
U3970	A^-> ZN v	0AI21 X1	0.024	2,102	0.448
U4233	$A v \rightarrow ZN^{1}$	0AI21_X1	0.021	2.123	0.469
U4232	$ A^{-} \rightarrow ZN v $	0AI221 X1	0.034	2.157	0.503
U4231	A V -> ZN ^	0AI21 X1	0.113	2.270	0.616
U3648	A ^ -> ZN V	I INV XI	0.025	2.295	0.642
		_			
U3330	A v -> Z v	BUF_X1	0.050	2.346	0.692
U3273	A v -> Z v	BUF_X1	0.055	2.401	0.747
U3255	A v -> ZN ^	INV_X1	0.157	2.557	0.903
U3513	B2 ^ -> ZN v	0AI22_X1	0.049	2.606	0.953
rC1_reg[52]	Dv	DFF XI	0.000	2.606	0.953
+					

# 4. Pre-CTS Optimization

- Run the following command to optimize the design before CTS.
   encounter #> optDesign –preCTS
- (This will take some time, up to 20~30 minutes depending on the machine you are working in).
- After Pre-CTS optimization is done, you will see the following result:

### 4. Pre-CTS Optimization

• Pre-CTS optimization

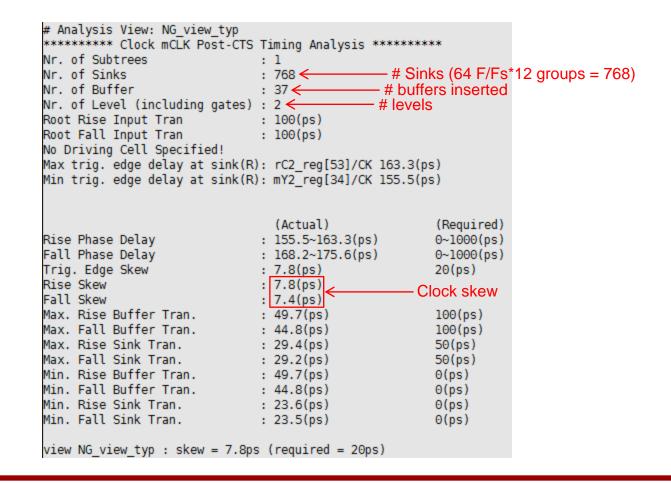
į	Setup mode	Ì	all	reg2r	eg	in2reg	reg2out	in2out	clkgate
Positive WNS -	WNS (r TNS (r Violating Pat All Pat	ns):  ths:	0.066 0.000 0 768	0.07 0.00 0 512	0   	0.066 0.000 0 256	N/A   N/A   N/A   N/A	N/A N/A N/A N/A	N/A   N/A   N/A   N/A
Ť	DRVs -	Nr	nets(tem	Real +- ns)	Wors	+	Total Nr nets(te	·····i	
+-	max_cap max_tran max_fanout max_length		0 (0) 0 (0) 0 (0) 0 (0) 0 (0)	+-     	0.	000   000   0   0	0 (0) 0 (0) 0 (0) 0 (0)		

### 4. Pre-CTS Optimization

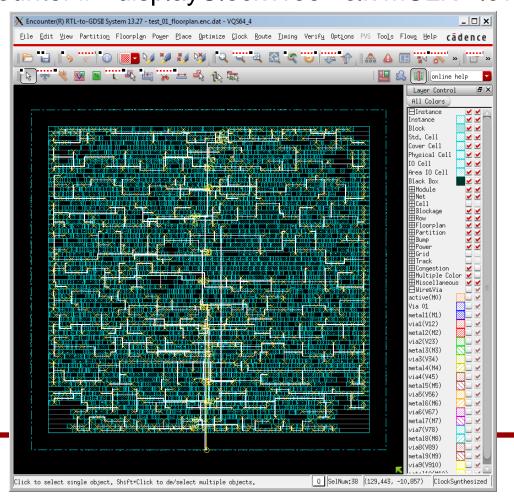
• saveDesign test\_04\_prectsopt.enc

- Open "VQS64\_4\_fm.ctstch" in a text editor and see the spec.
- Run the following command to run CTS.
  - encounter #> clockDesign -specFile VQS64\_4\_fm.ctstch outDir clk\_report

#### • CTS



You can see the clock tree by the following command:
 – encounter #> displayClockTree –clk mCLK –level 1



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• saveDesign test\_05\_cts.enc

- Run the following command to check timing.
  - timeDesign –postCTS

timeDes	ign S	ummary						
Setup mode WNS (ns): TNS (ns): Violating Paths: All Paths:		all	+   reg2	reg?	+   in2reg	reg2out	in2out	+
		0.000 0.0		071   0.207 000   0.000 0   0 12   256		N/A   N/A   N/A   N/A	N/A N/A N/A N/A	N/A   N/A   N/A   N/A
DRVs	+   +		Real			Tota	+ L	
	Nr	Nr nets(terms)			st Vio	Nr nets(terms)		
max_cap max_tran max_fanout max_length		0 (0) 0 (0) 0 (0) 0 (0) 0 (0)		0.000   0.000   0   0		0 (0)   0 (0)   0 (0)   0 (0)		

Density: 75.449%

#### 6. Post-CTS Optimization

- Although we already satisfied the timing without any further optimization after CTS, we will run post-CTS optimization.
  - encounter #> optDesign –postCTS

					+		+
Setup mode	Setup mode   all		reg2reg	in2reg	reg2out	in2out	clkgat
TNS Violating Pa	WNS (ns):  0.101   TNS (ns):  0.000   /iolating Paths:  0   All Paths:  768		0.121 0.000 0 512	0.101 0.000 0 256	N/A   N/A   N/A   N/A	N/A N/A N/A N/A	N/A   N/A   N/A   N/A
	+	F	Real	· · · · · · · · · · · · · · · · · · ·	Total	<b>+</b>	
DRVs	1						
DRVs	Nr net		+	st Vio	Nr nets(te	erms)	

Density: 65.532%

#### 6. Post-CTS Optimization

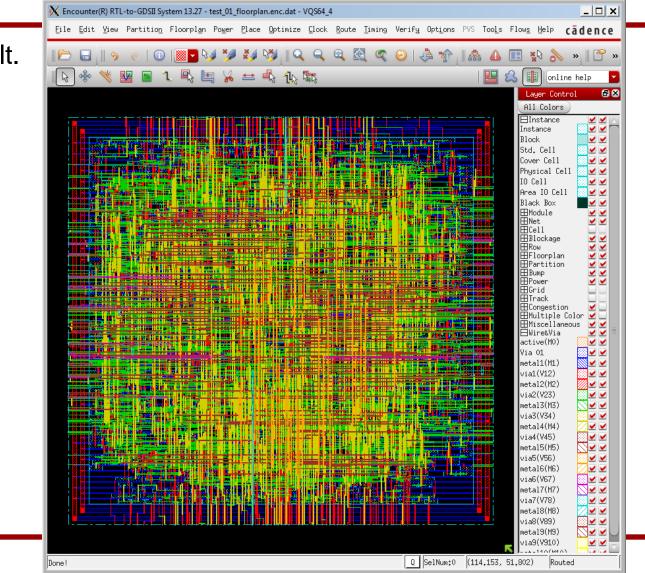
• saveDesign test\_06\_postctsopt.enc

- Run the following command to check timing.
  - timeDesign –postCTS

Setup mode	- i -	all	reg2	2reg	in2reg	reg2out	in2out	clkgate
WNS ( TNS ( Violating Pa All Pa	ns):  0 ths:	.101 .000 0 768			0.101 0.000 0 256	N/A   N/A   N/A   N/A	N/A   N/A   N/A   N/A	N/A   N/A   N/A   N/A
DRVs	+		Real		1	Tota	+ l	
DRVS	Nr ne	ts(tem	ns)	Worst Vio		Nr nets(t	erms)	
nax_cap nax_tran nax_fanout nax_length	0   0	(0) (0) (0) (0)			.000   .000   0   0	0 (0) 0 (0) 0 (0) 0 (0)		

- Click "Route"  $\rightarrow$  "NanoRoute"  $\rightarrow$  "Route...".
- Turn off "Fix Antenna" and click OK to run routing.

✓ NanoRoute
Routing Phase
✓ Global Route
✓ Detail Route Start Iteration 0 End Iteration default
Post Route Optimization 📃 Optimize Via 🛄 Optimize Wire
Concurrent Routing Features
Fix Antenna
Timing Driven     Effort 5     Congestion     Timing     S.M.A.R.T.
SI Driven
🗌 Post Route SI 🛛 SI Victim File 📄
Litho Driven
🔄 Post Route Litho Repair
Routing Control
Selected Nets Only Bottom Layer default Top Layer default ECO Route
Area Route Area Select Area and Route
Job Control
🗹 Auto Stop
Number of Local CPU(s): 1
Number of CPU(s) per Remote Machine: 1
Number of Remote Machine(s): 0 Set Multiple CPU
See Interface of 0***
OK Apply tribut Mode Save Load Cancel Help



• Routing result.

- Routing result.
- Wirelength: 52,077um
- No DRC violations.

#Complete Detail Routing. #Total number of nets with non-default rule or having extra spacing = 38 #Total wire length = 52077 um #Total half perimeter of net bounding box = 48628 um. #Total wire length on LAYER metall = 1604 um. #Total wire length on LAYER metal2 = 15448 um. #Total wire length on LAYER metal3 = 19261 um. #Total wire length on LAYER metal4 = 9446 um. #Total wire length on LAYER metal5 = 4644 um. #Total wire length on LAYER metal6 = 1314 um. #Total wire length on LAYER metal7 = 236 um. #Total wire length on LAYER metal8 = 68 um. #Total wire length on LAYER metal9 = 56 um. #Total wire length on LAYER metall0 = 0 um. #Total number of vias = 24082 #Up-Via Summary (total 24082): Metal 1 10605 Metal 2 10028 Metal 3 2748 Metal 4 515 Metal 5 147 Metal 6 25 Metal 7 8 Metal 8 6 24082 #Total number of DRC violations = 0

• saveDesign test\_07\_route.enc

- Run the following command to check timing.
  - timeDesign -postRoute

timeDes:	ign Summary						
					±		+
Setup mode	etup mode   all		reg2reg   in2reg		reg2out	in2out	clkgat
WNS (ns):  0.102 TNS (ns):  0.000 Violating Paths:  0 All Paths:  768		0.0	0.139   0.102 0.000   0.000 0   0 512   256		N/A   N/A   N/A   N/A	N/A   N/A   N/A   N/A	N/A   N/A   N/A   N/A
	+ 	Real			Tota	+ L [	
DRVs	Nr nets(te	ermis)	Worst Vio		Nr nets(terms)		
<pre>max_cap max_tran max_fanout max_length</pre>	0 (0)   0 (0)   0 (0)   0 (0)		Θ.	000   000   0   0	0 (0) 0 (0) 0 (0) 0 (0)		

### 8. Post-Routing Optimization

- Although we already satisfied the timing without any further optimization after routing, we will run post-routing optimization.
  - encounter #> optDesign –postRoute

	+				L		+	+
Setup mode	- į	all	reg2	reg	in2reg	reg2out	in2out	clkgat
TNS (ns):  ( Violating Paths:		0.102 0.000 0 768	0.000   0.000 0   0		0.102 0.000 0 256	N/A   N/A   N/A   N/A	N/A N/A N/A N/A	N/A N/A N/A N/A
			Real			' Tota	+ l	
DRVs	Nr	nets(term	ns)	Worst Vio		Nr nets(terms)		
max_cap max_tran max_fanout max_length		0 (0) 0 (0) 0 (0) 0 (0)			.000   .000   0   0	0 (0) 0 (0) 0 (0) 0 (0)		

#### 8. Post-Routing Optimization

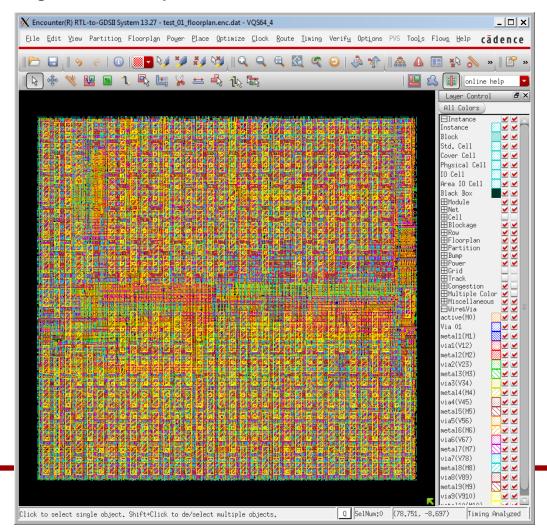
• saveDesign test\_08\_postrouteopt.enc

#### 9. Fill Insertion

- Click "Route" → "Metal Fill" → "Setup...".
- Click "Load" and choose "metalfill.cmd" to load the setting I made.
- Click OK.
- Click "Route"  $\rightarrow$  "Metal Fill"  $\rightarrow$  "Add".
- Click OK to insert metal fills.

#### 9. Fill Insertion

• The following shows my fill insertion result.



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- Run the following command to analyze timing.
  - encounter #> timeDesign –postRoute

timeDes	ign Summa	ry					
Setup mode	a	ii į	reg2reg	in2reg	reg2out	in2out	+   clkga
		0.000 0.0		0.102 0.000 0 256	N/A   N/A   N/A   N/A	N/A N/A N/A N/A	N/A N/A N/A N/A
DRVe			Real		Total	<b>+</b>	
DRVs	Nr nets	(terms	s)   Wors	st Vio	Nr nets(terms)		
max_cap max_tran max_fanout max_length	0   0	0 (0) 0 (0) 0 (0) 0 (0)		.000   .000   0   0	0 (0)   0 (0)   0 (0)   0 (0)		

Density: 65.532%

#### 9. Fill Insertion

• saveDesign test\_09\_fill.enc