EE 466/586
VLSI Design

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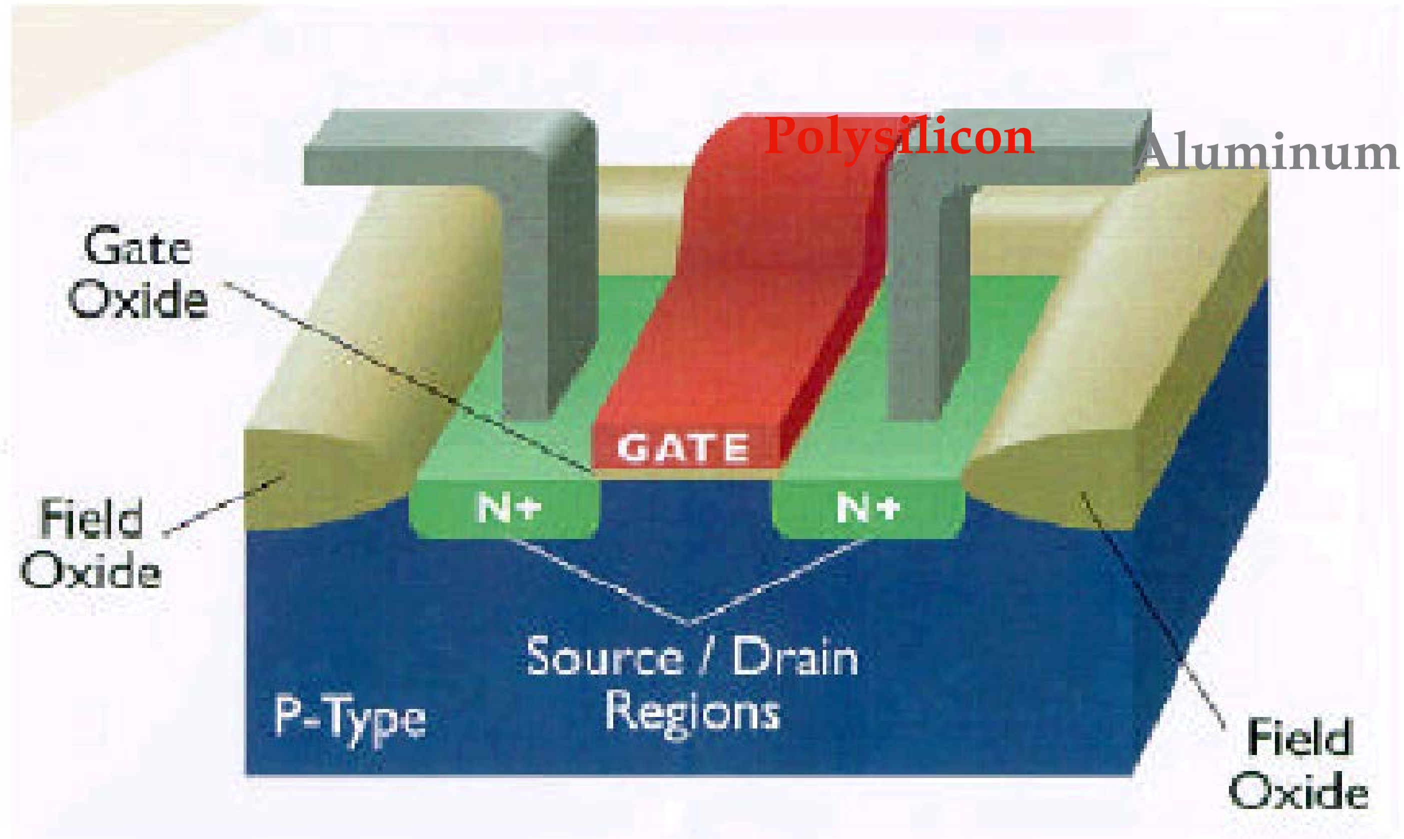
Lecture 2

The MOS Transistor

(Reference: Chapter 2 of Weste and Harris or Chapter 2 of HJS)

The MOS Transistor



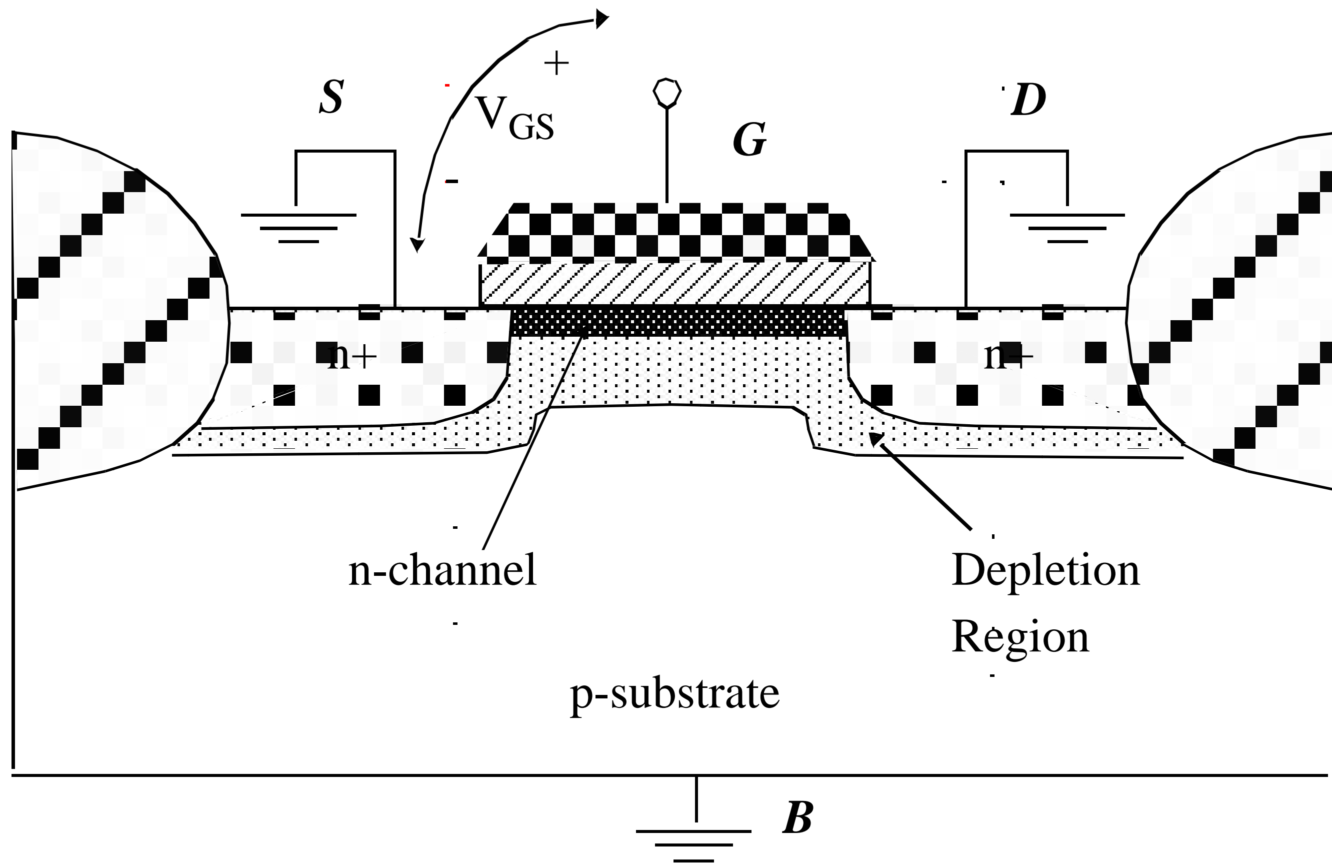
Structural Details

- Channel length L
  - Typical values of L today vary from 90nm to 32 nm
  - The dimension will continue to scale according to Moore's law
- Perpendicular to the plane of the figure is the channel width W
  - Much larger than the minimum length
- Gate oxide thickness t_{ox}
  - Around 25 Å

Operational Mechanism

- We consider a NMOS transistor
- N+ source and N+ drain regions separated by p-type material
- The body or substrate, is a single-crystal silicon wafer
- Suppose, source, drain and body are all tied to ground and a positive voltage applied to the gate
  - A positive gate voltage will tend to draw electrons from the substrate into the channel region
  - A conducting path is created between drain and source
  - Current will flow from drain to source in presence of a voltage difference between the source and the drain
  - The gate voltage needed to initiate formation of a conducting channel is termed as the threshold voltage Vt

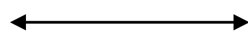
Threshold Voltage: Concept

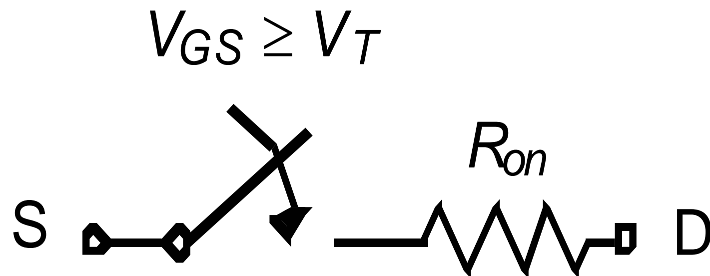


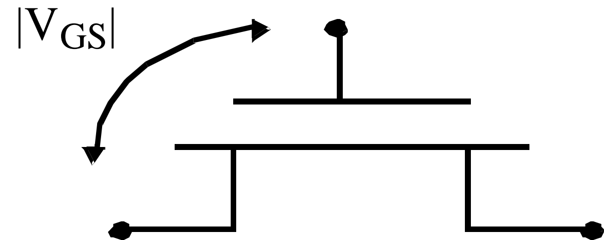
The Threshold Voltage

Follow board notes

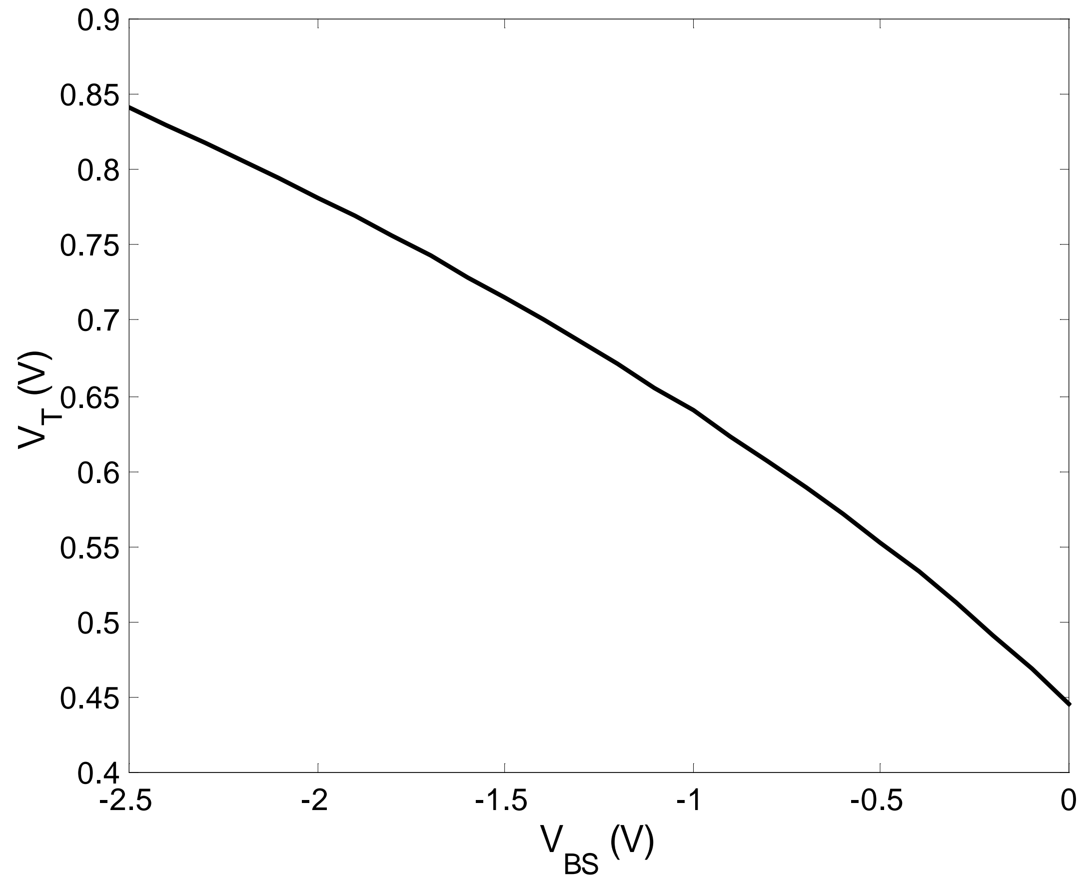
What is a Transistor?

A Switch!  An MOS Transistor





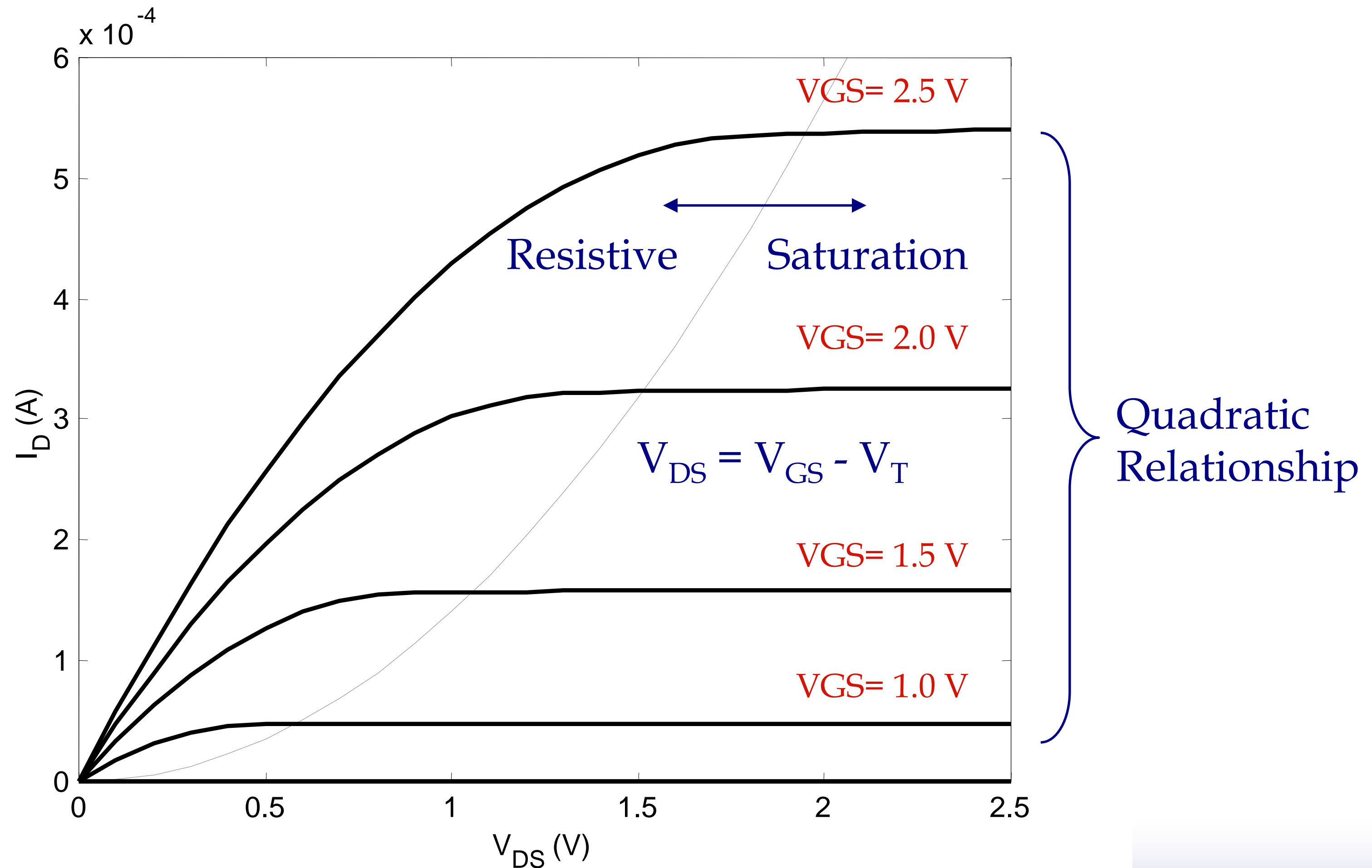
The Body Effect



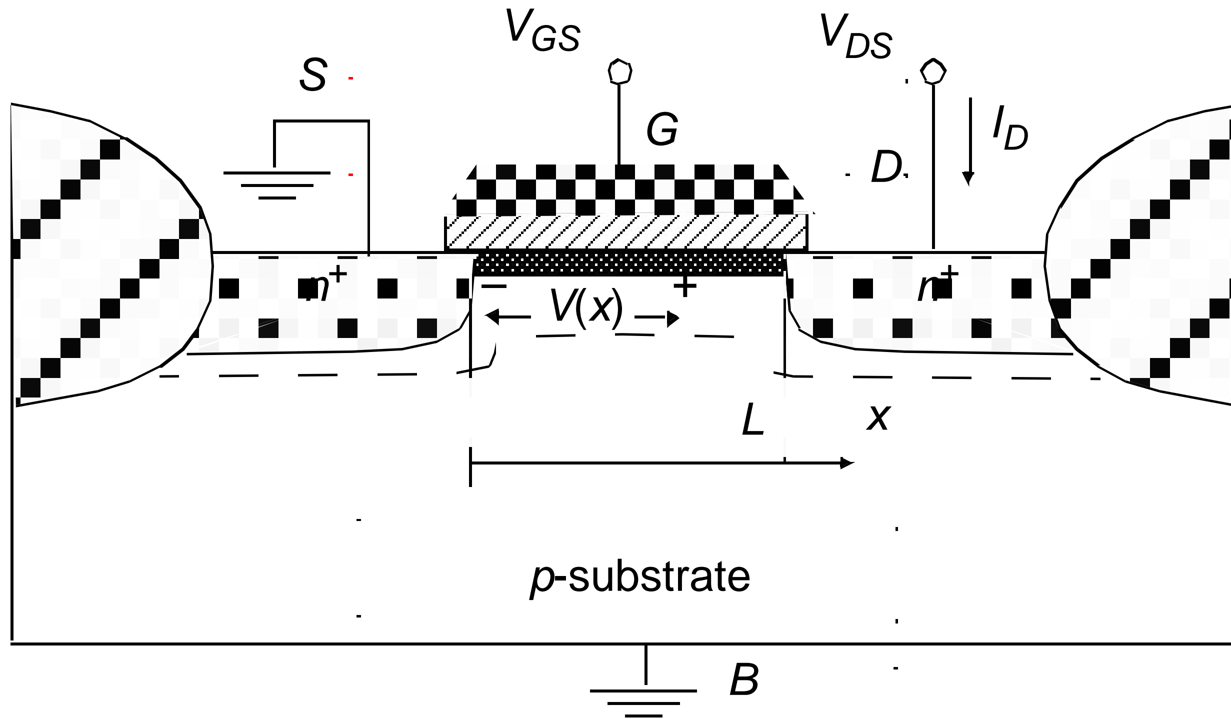
Current-Voltage Relations

- Follow board notes

Current-Voltage Relations

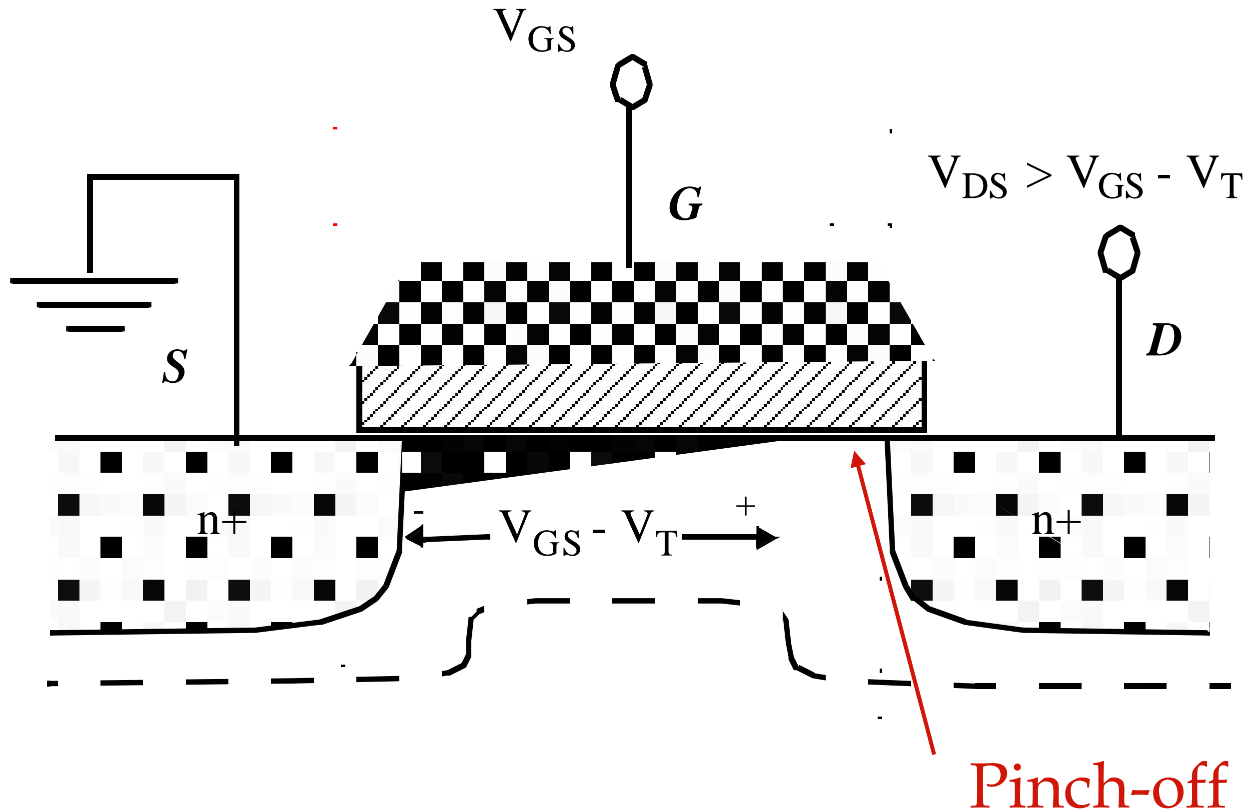


Transistor in Linear



MOS transistor and its bias conditions

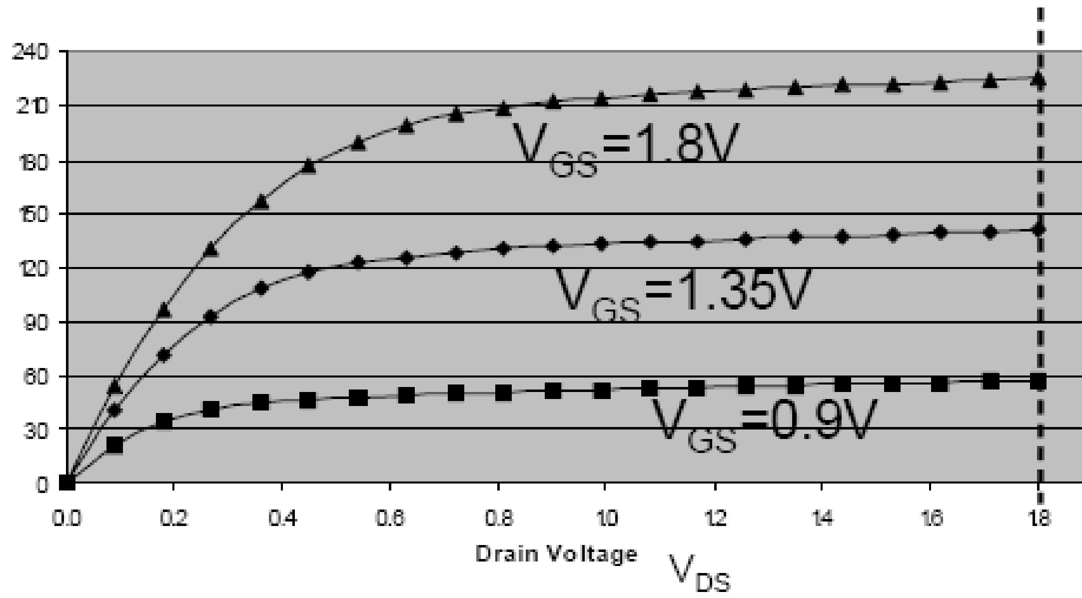
Transistor in Saturation

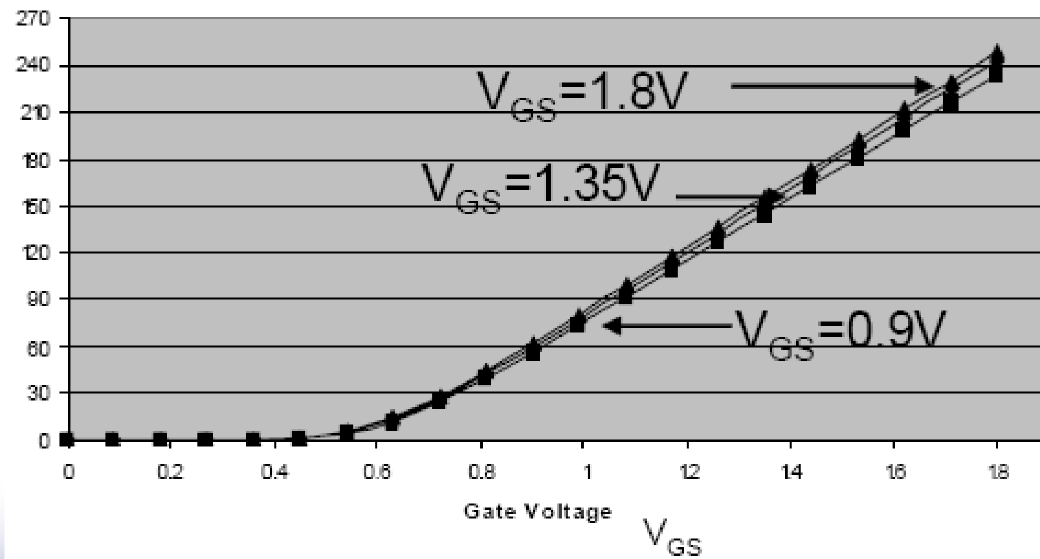


Current-Voltage Relations
The Deep-Submicron Era

- The quadratic model is valid for long channel devices
- In DSM, channel length is scaled
  - Vertical and horizontal electric fields are large and they interact with each other
  - Saturation in DSM devices occur when the carriers reach velocity saturation

I_{DS} vs. V_{DS} for NMOS





Effect of high fields

1980:	1995:	2001:
$E_y = \frac{5V}{5\mu m} = 10^4 \, V/cm$	$E_y = \frac{3.3V}{0.35\mu m} = 9.4\times10^4 \, V/cm$	$E_y = \frac{1.2V}{0.1\mu m} = 1.2\times10^5 \, V/cm$

Horizontal Field

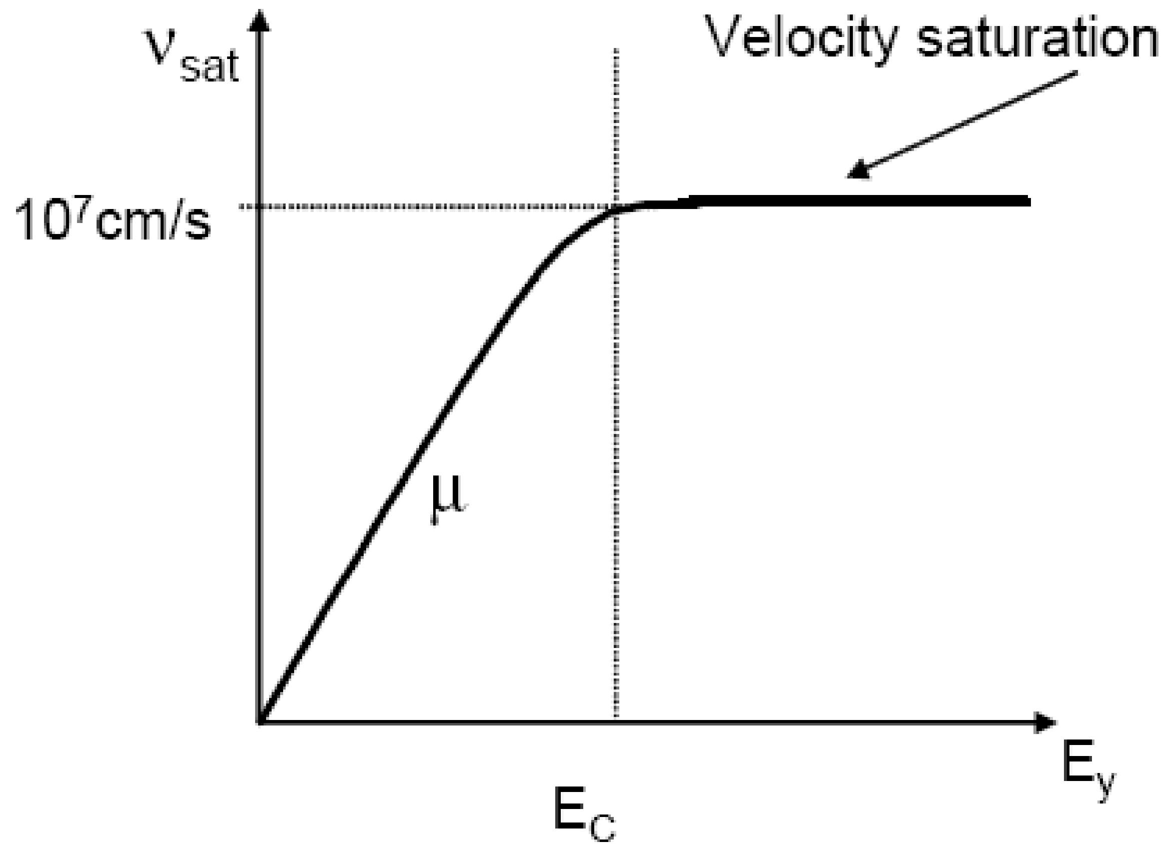
1980:	1995:	2001:
$E_x = \frac{5V}{1000Å} = 50\times10^4 \, V/cm$	$E_x = \frac{3.3V}{100Å} = 4.4\times10^6 \, V/cm$	$E_x = \frac{1.2V}{22Å} = 5.5\times10^6 \, V/cm$

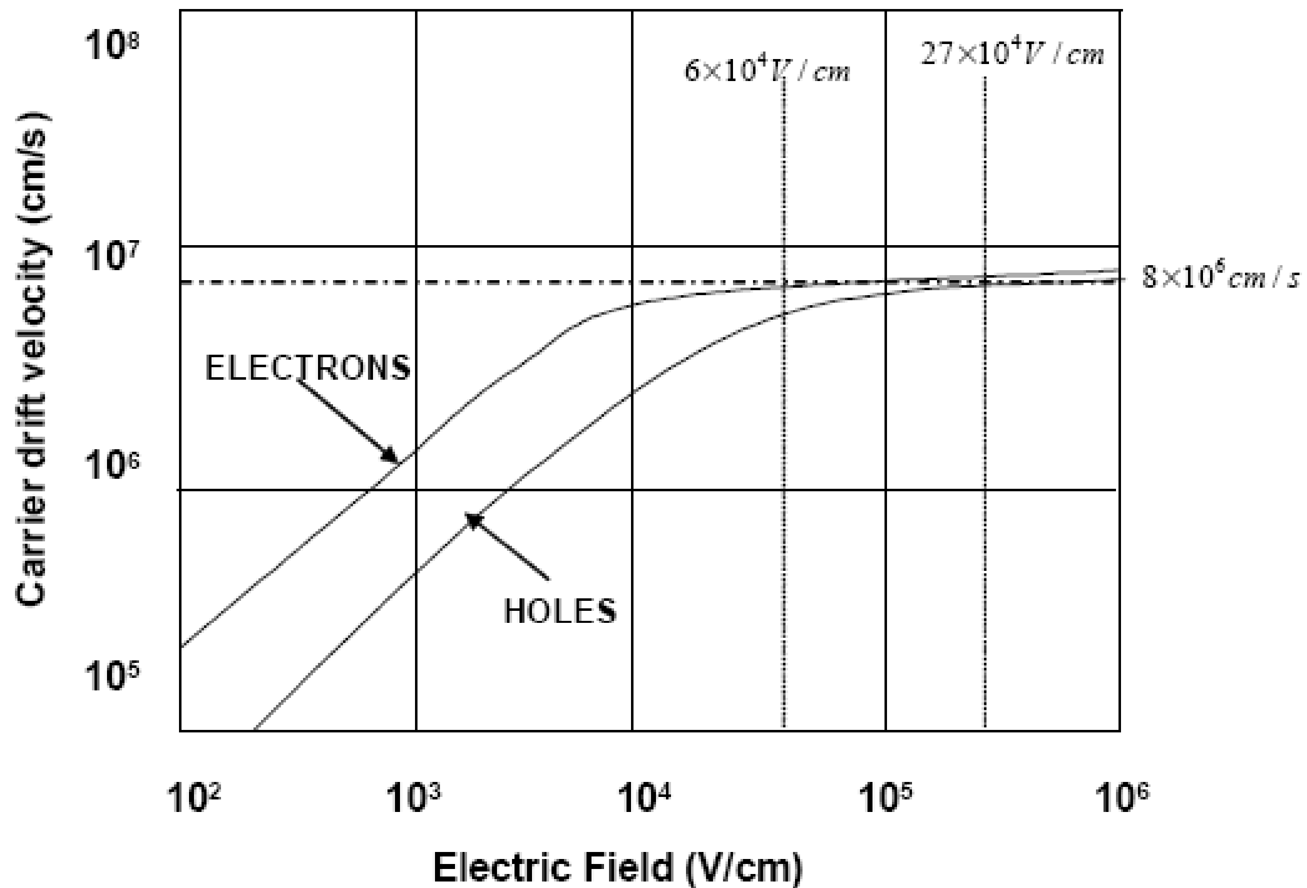
Vertical Field

Effect of high fields (Cont'd)

- Effect of the vertical field on the mobility
  - The vertical field increases the electron scattering at the surface of the channel
- Follow board notes
- The horizontal field acts to reduce the mobility even further

Velocity Saturation





$$E_{cn} = 6\times10^4 \ \frac{\mathrm{V}}{\mathrm{cm}} \ \text{for electrons}$$

$$E_{cp} = 27\times10^4 \ \frac{\mathrm{V}}{\mathrm{cm}} \ \text{for hole.}$$

Velocity Saturation (Cont'd)

$$v = \mu_e \frac{E}{\left(1+\frac{E}{E_c}\right)} \qquad E_y < E_c$$

$$v = v_{sat} \qquad E_y \geq E_c$$

$$v = \mu_e \frac{E}{\left(1+\frac{E}{E_c}\right)} = \frac{\mu_e E_c}{2}$$

$$\therefore E_c = \frac{2 v_{sat}}{\mu_e}$$

Current Equations

$$I_{DS} = W \times Q_n \times v$$

$$I_{DS} = W \; C_{ox}(V_{GS} - V_T - V(y)) \left(\frac{\mu_e E}{1 + \frac{E}{Ec}} \right)$$

$$I_{DS} = \frac{W}{1 + \frac{E}{E_c}} \; C_{ox}(V_{GS} - V_T - V(y)) \; \mu_e E$$

$$where \;\; E = -\frac{dV(y)}{dy}$$

Current Equation (Cont'd)

$$I_{DS} = W\mu_e \left[C_{ox}(V_{GS} - V_T - V(y)) + \frac{I_{DS}}{W/\mu_e E} \right] \frac{dV(y)}{dy}$$

$$I_{DS} = \frac{W}{L} \cdot \frac{\mu_e C_{ox}}{(1 + \frac{V_{DS}}{E_c L})} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}$$

Current Equation (Saturation)

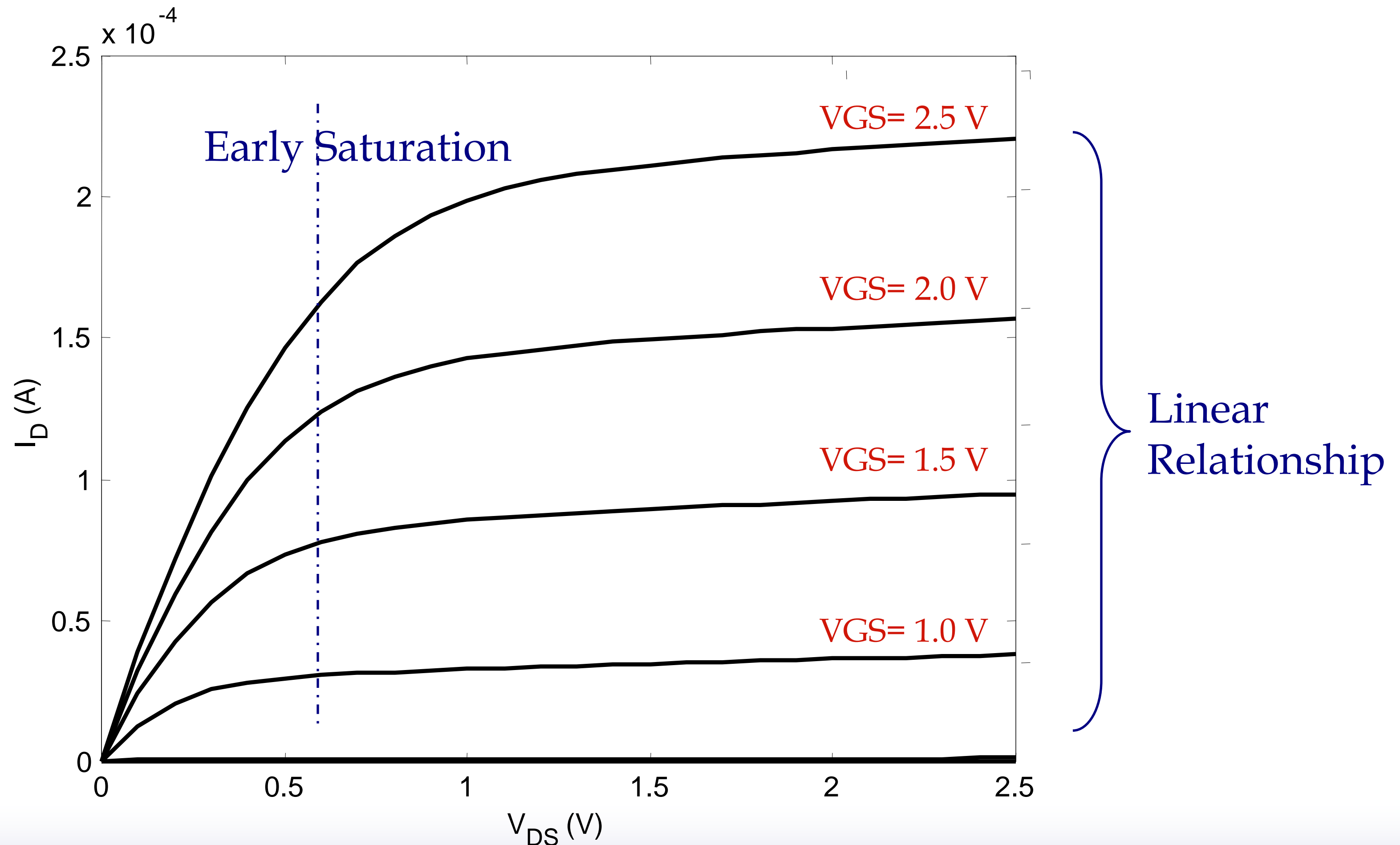
$$I_{DS} = W \times Q_n \times v_{sat}$$

$$I_{DS} = W \times C_{ox}\left(V_{GS} - V_T - V_{DS}\right)v_{sat}$$

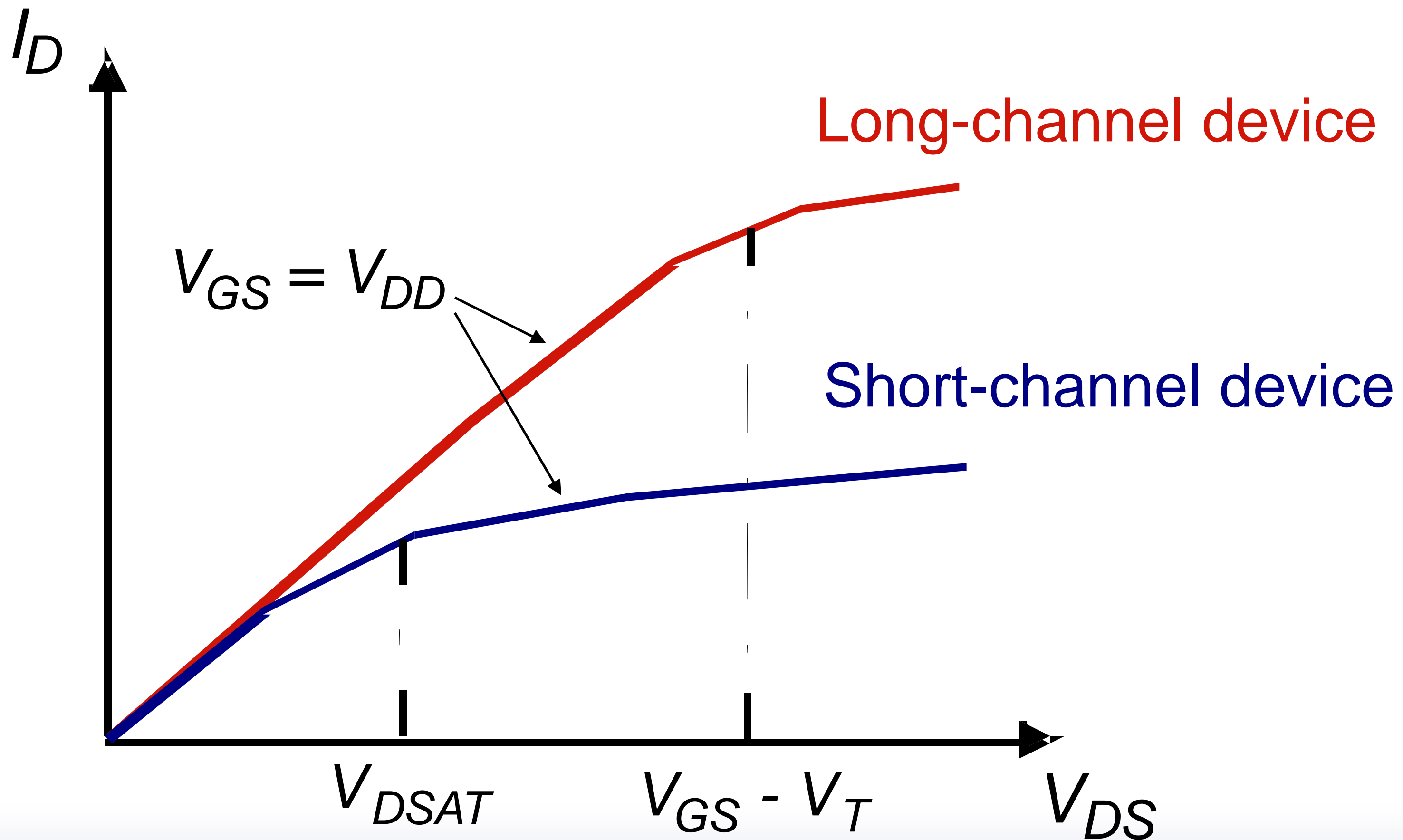
$$V_{Dsat} = \frac{(V_{GS} - V_T)E_c L}{(V_{GS} - V_T) + E_c L}$$

$$I_{DS} = W v_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_c L}$$

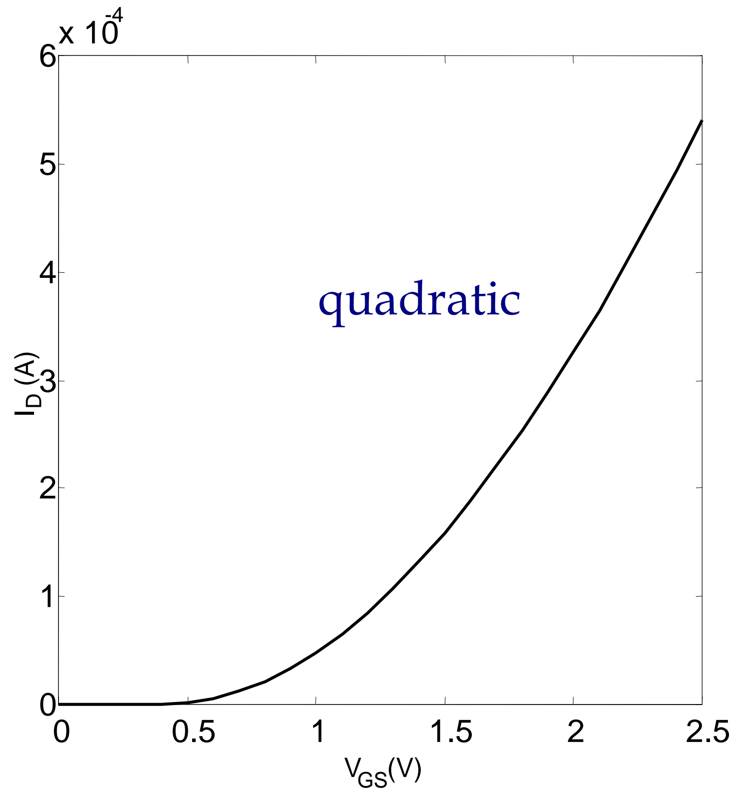
Current-Voltage Relations
The Deep-Submicron Era



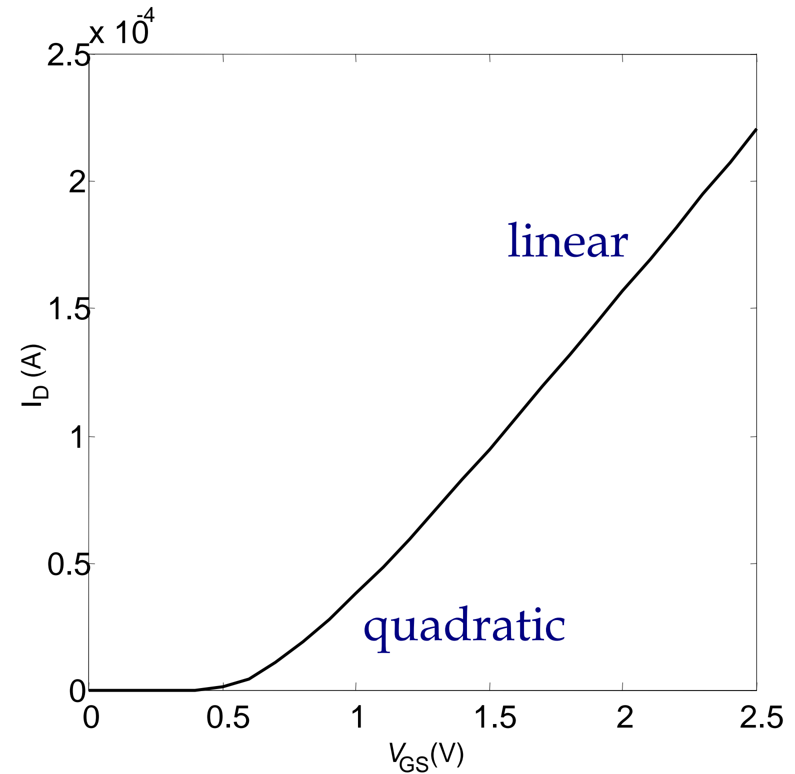
Perspective



I_D versus V_{GS}

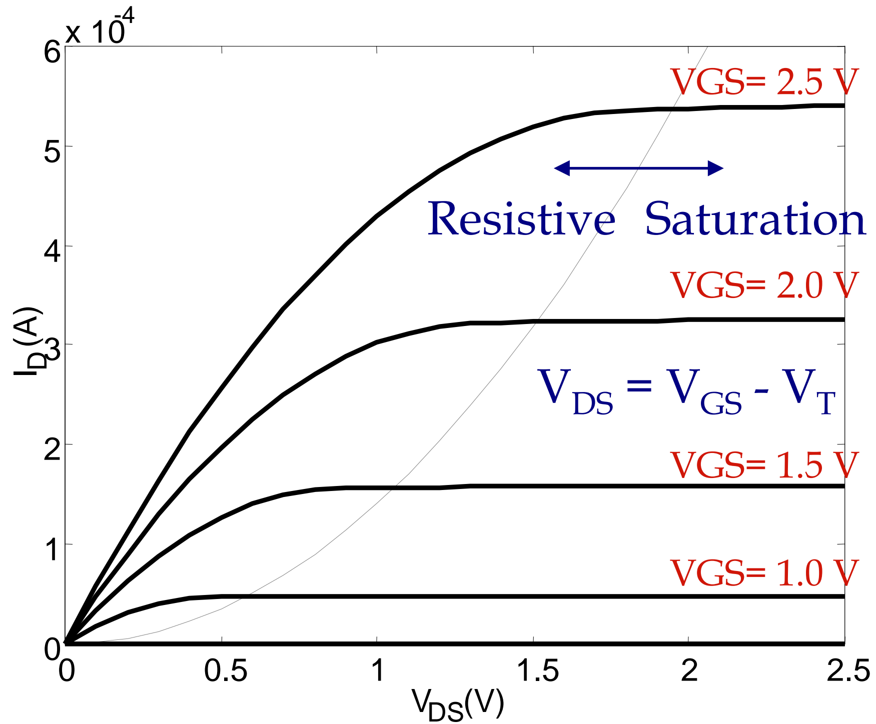


Long Channel

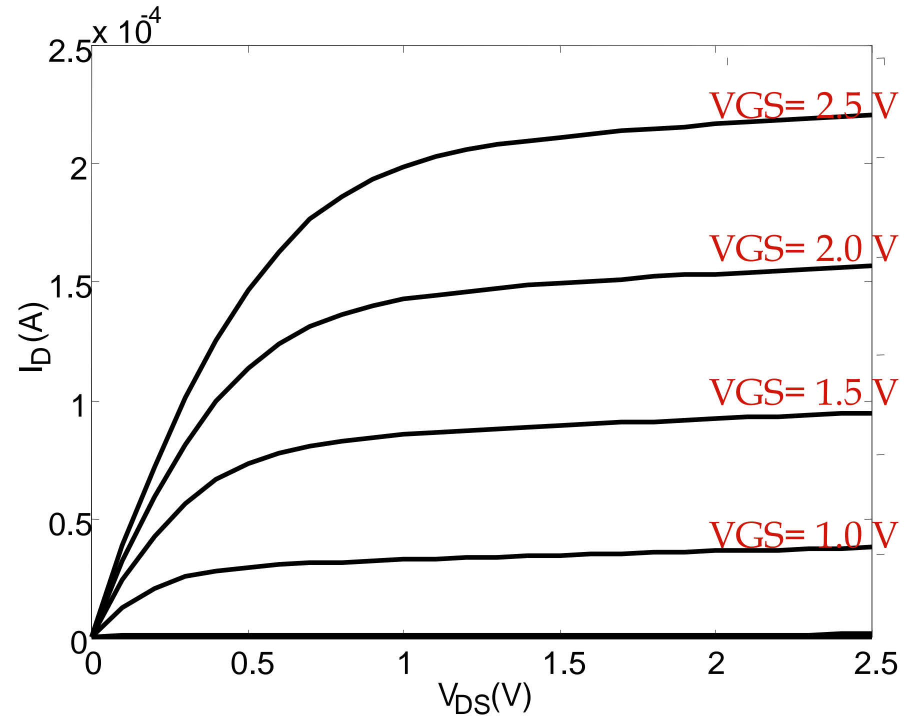


Short Channel

I_D versus V_{DS}

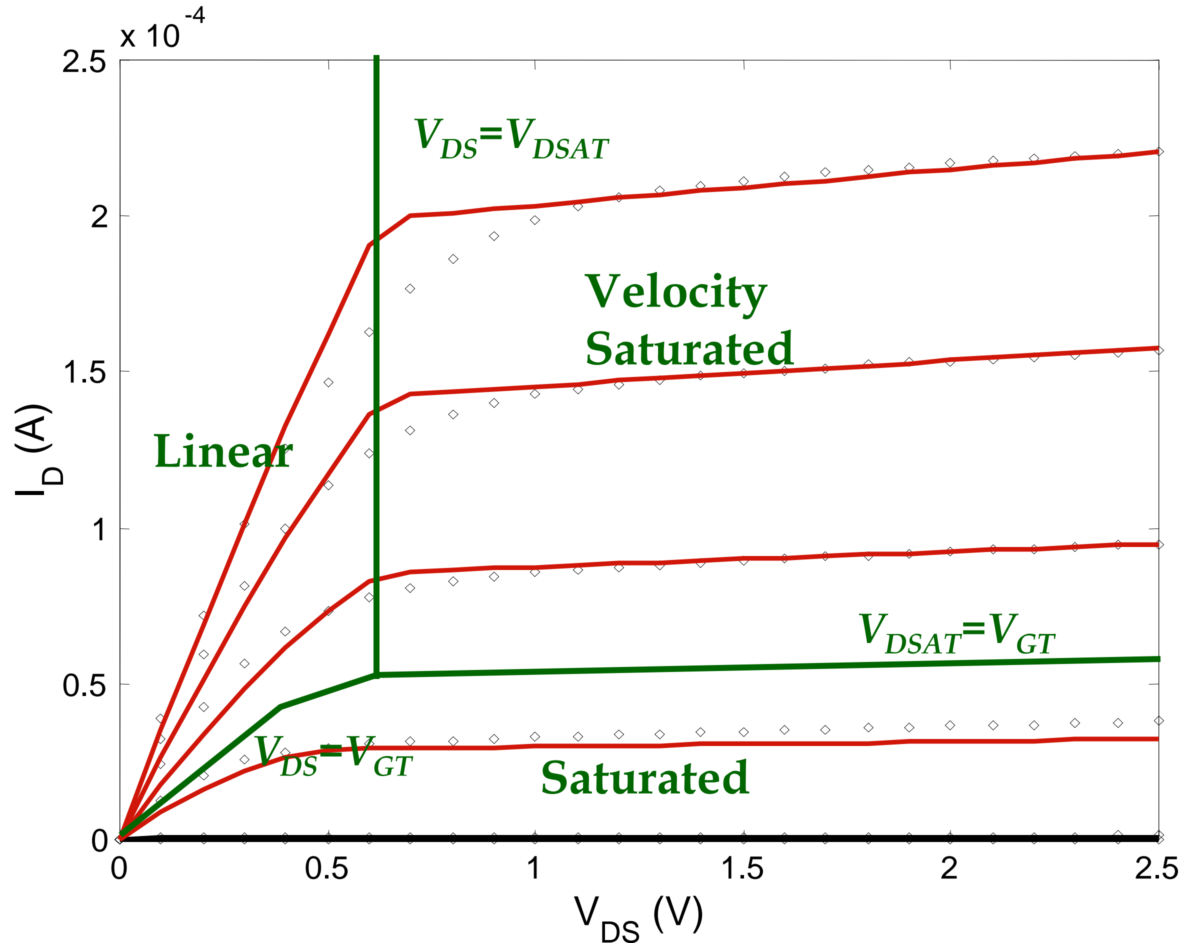


Long Channel

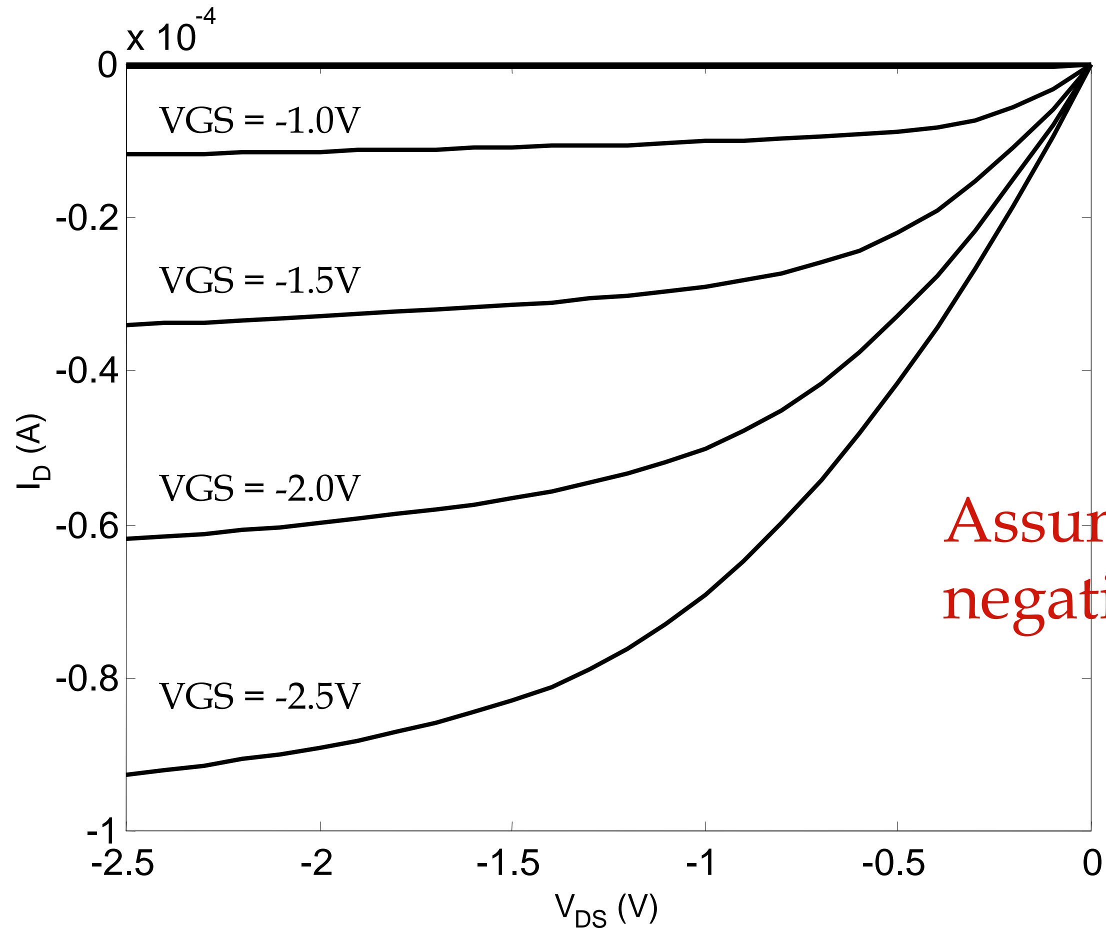


Short Channel

Simple Model versus SPICE



A PMOS Transistor



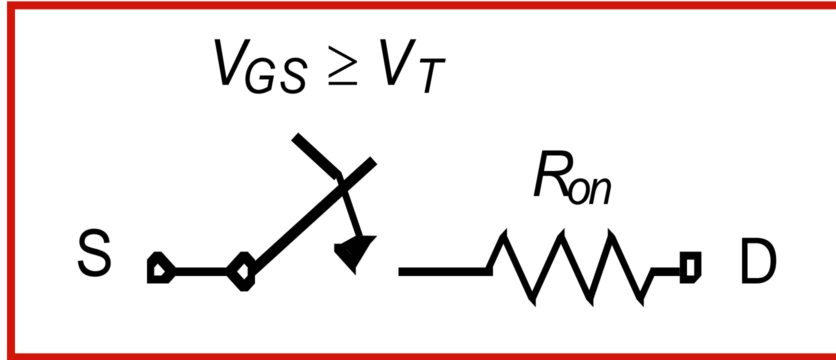
Assume all variables negative!

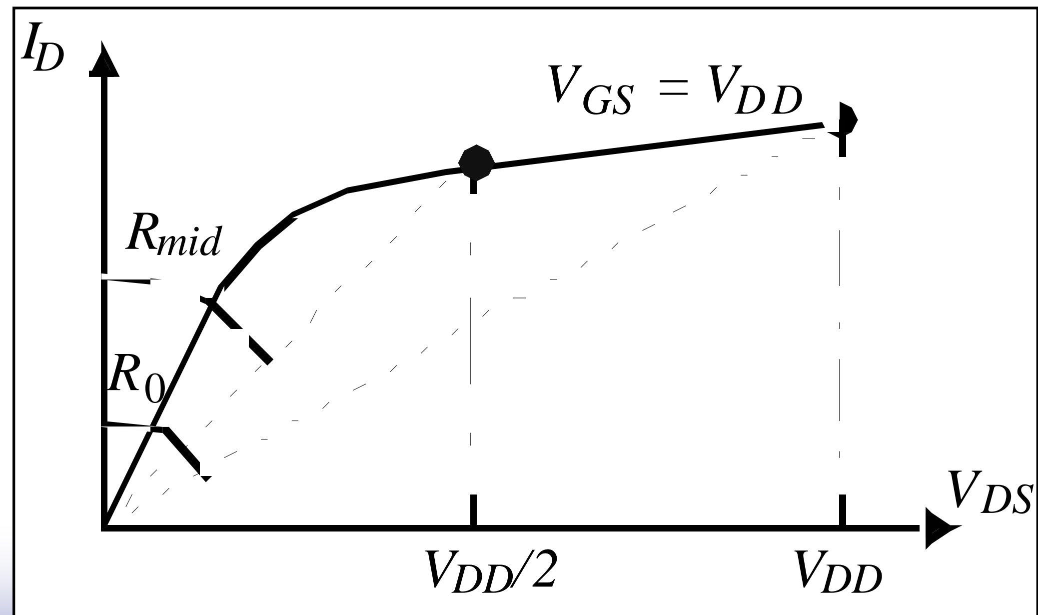
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	–0.4	-0.4	-1	-30×10^{-6}	-0.1

The Transistor as a Switch





The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31