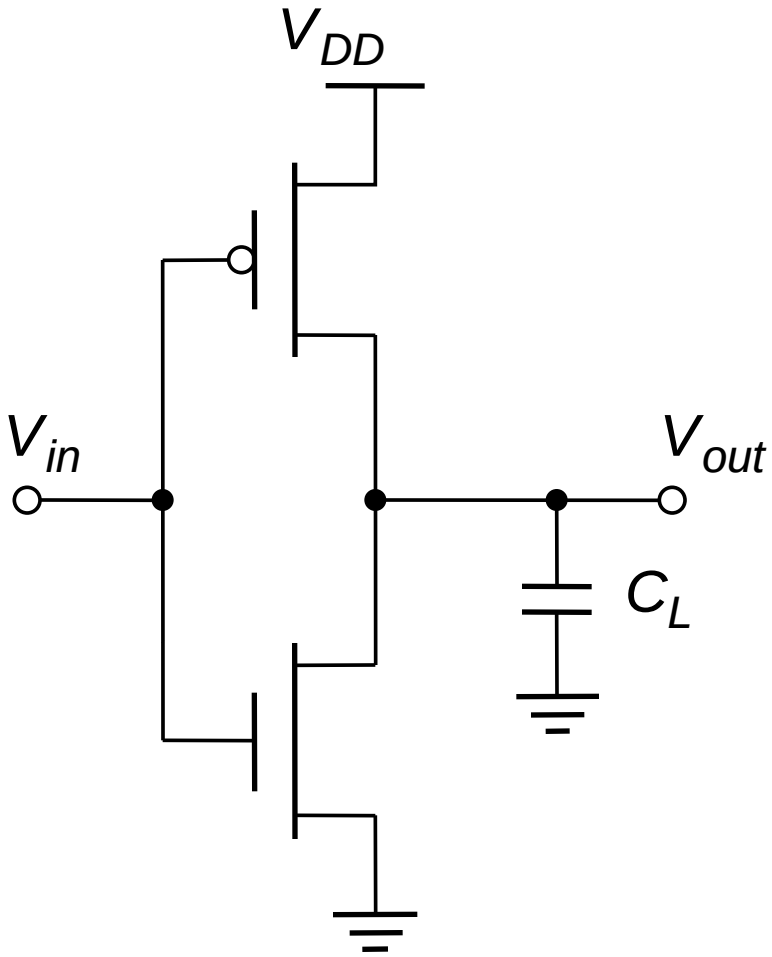
EE586
VLSI Design

Partha Pande
School of EECS
Washington State University
pande@eecs.wsu.edu

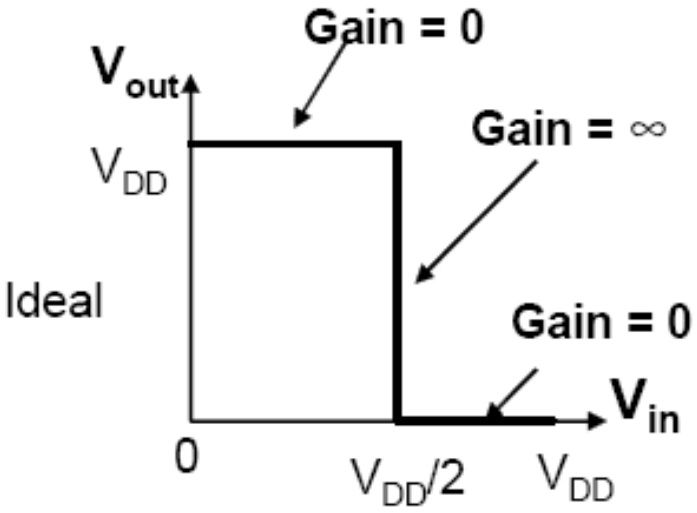
Lecture 4

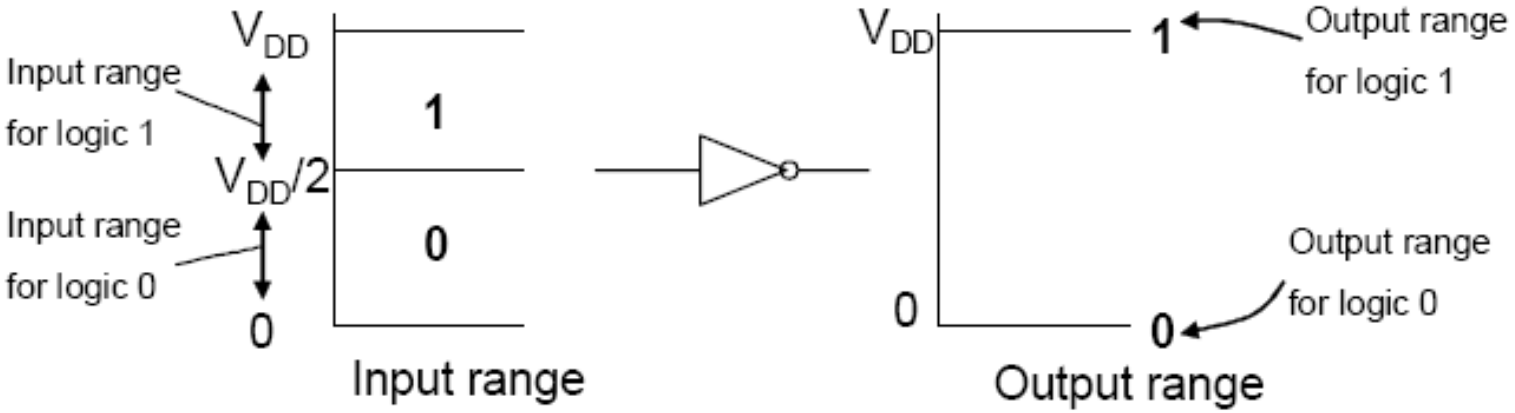
MOS Inverter Circuits

The CMOS Inverter: A First Glance



Ideal Voltage Transfer Characteristics (VTC)

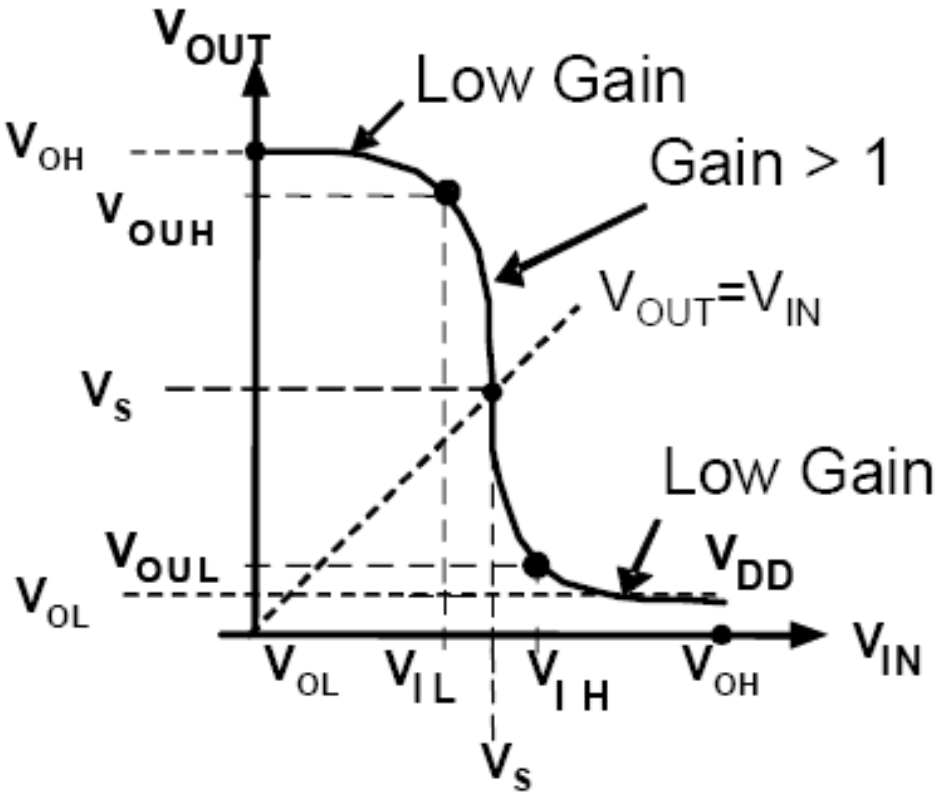




Characteristics of Ideal VTC

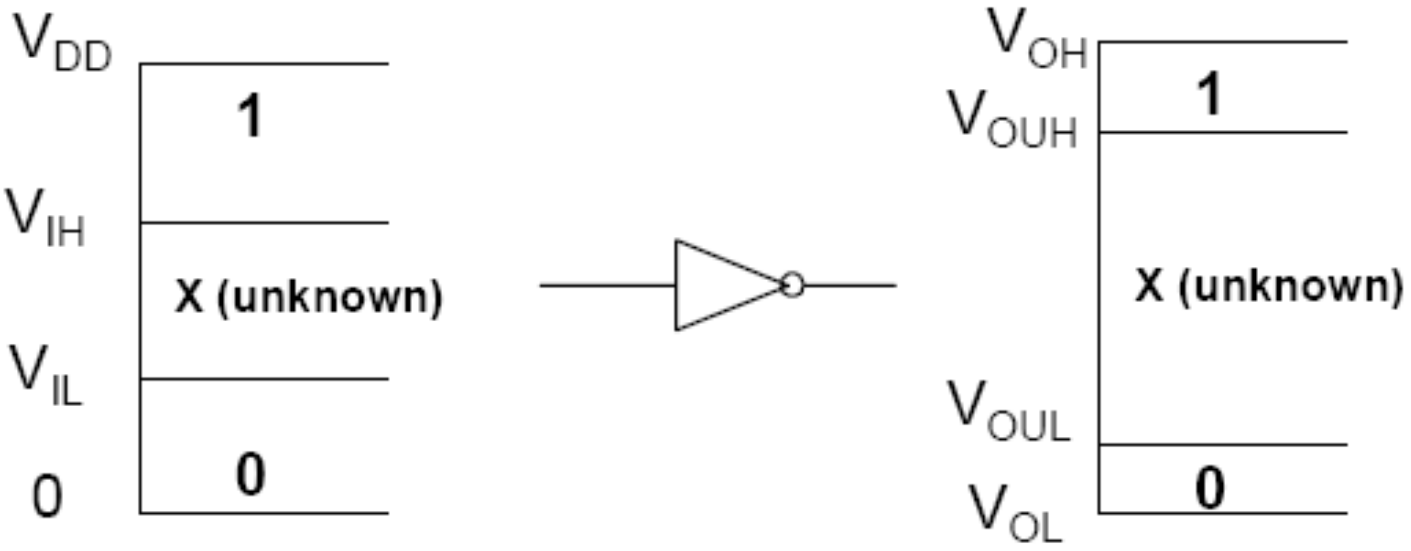
- Switching point occurs at VDD/2.
- Three gain regions in the ideal inverter VTC
  - Two zero gain regions and one infinite gain region
- The high gain region, separating the high output from the low output, is a feature required by all useful logic gates to reject noise in the system.
- The input range is very large while the output range is small for the ideal inverter.
  - The range refers to the voltage interval over which a signal is considered to be a logic 0 or logic 1
- Having a large input range and small output range is a desirable characteristic of a logic gate for noise immunity.
  - It implies that the input can vary significantly with little or no effect on the output.

Realistic VTC



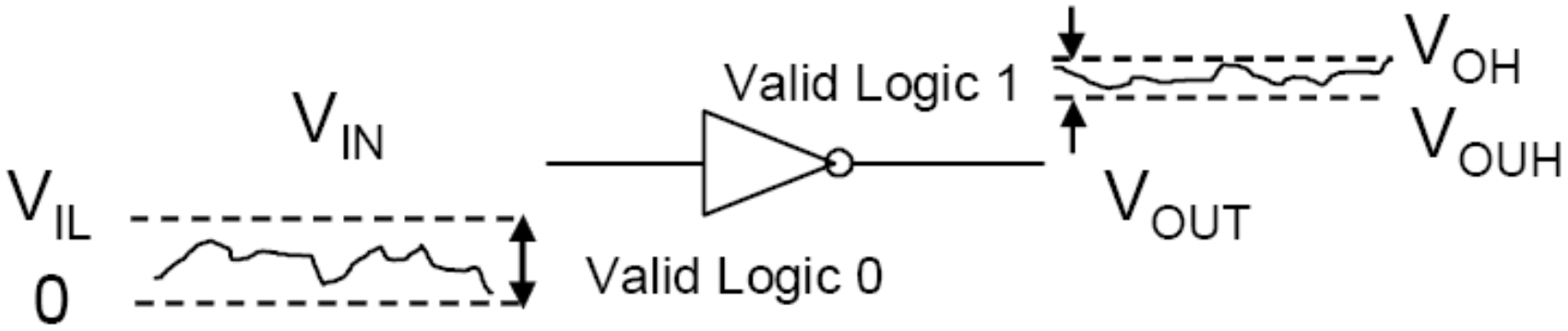
- *In practical inverters, the low output voltage, VOL, may not reach Gnd, and the high output voltage VOH, may not reach VDD.*
- *The output does not abruptly switch from VDD to Gnd at VDD/2.*
- *Switching point, VS, is defined as the point where VOUT=VIN*

Realistic VTC



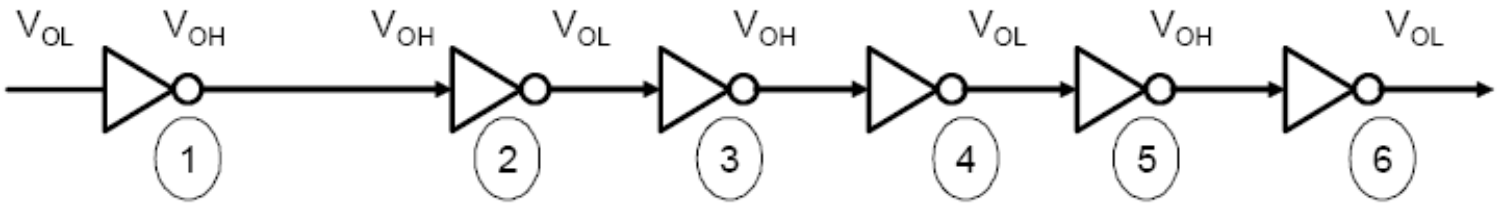
- ***The input range for logic 0 is from 0V to a point called VIL where the input is still considered to be low.***
- ***The input range for logic 1 is the interval from VOH to VIH, where the input is still considered to be high.***
- ***The output ranges are from VOL to VOUL for logic 0 and VOH to VOUH for logic 1***

Effects of Noise

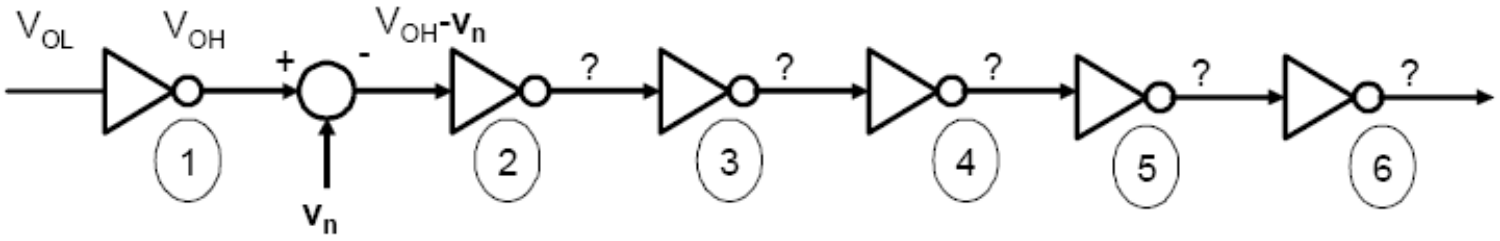


- ***Input variation remains within the valid logic 0 range.***
- ***The output varies by a smaller amount but remains in the range considered to be a valid logic 1***
- ***Input is varying in the range where the logic gate acts as a low-gain amplifier, from VOL to VIL.***
- ***This attenuates the noise since the gain is less than one in this range.***
- **the output remains in the range VOUH to VOH**
- **The next few inverters in the chain will attenuate the noise even further and eventually the noise is damped out of the system.**

Noise Margin

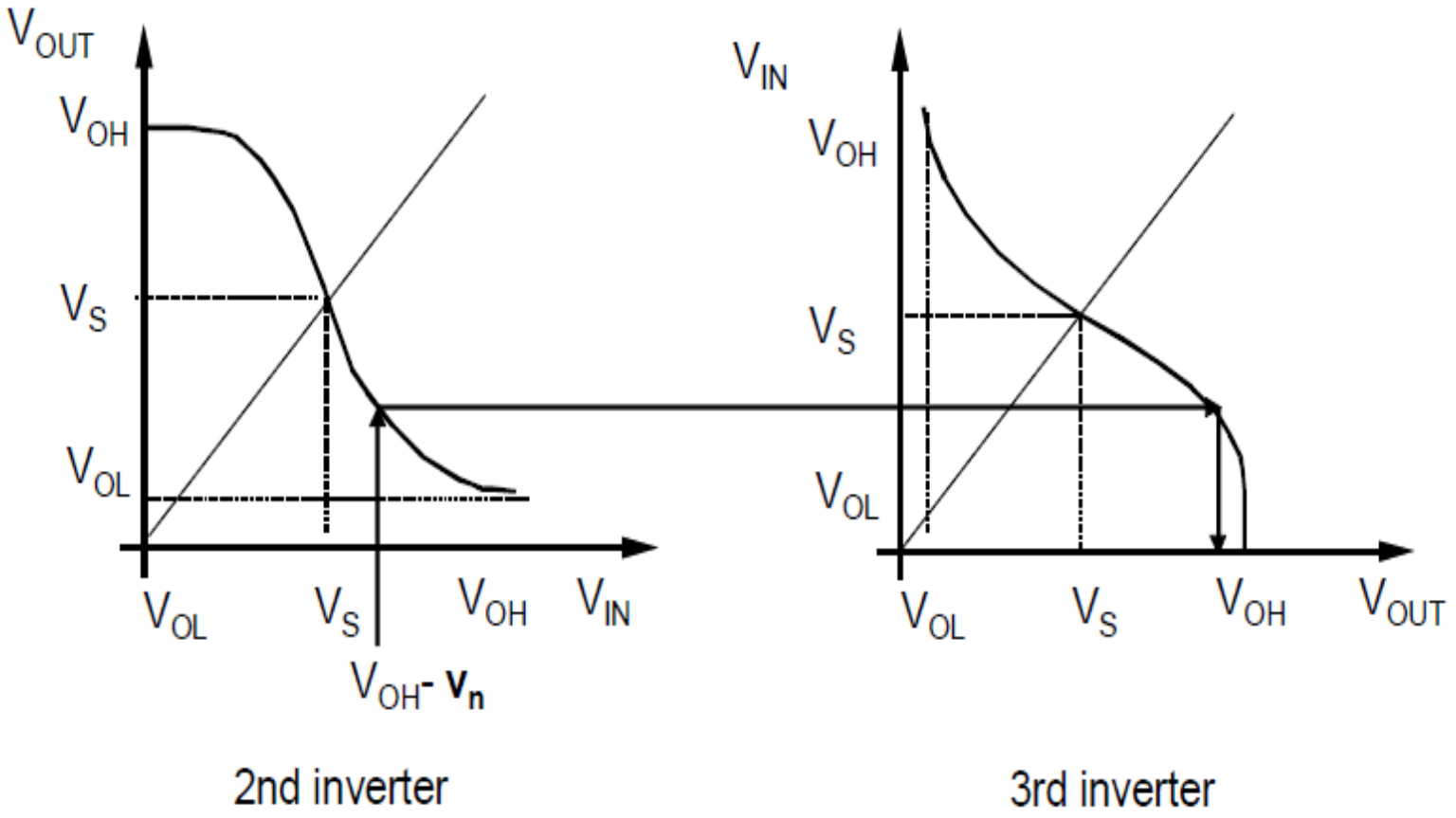


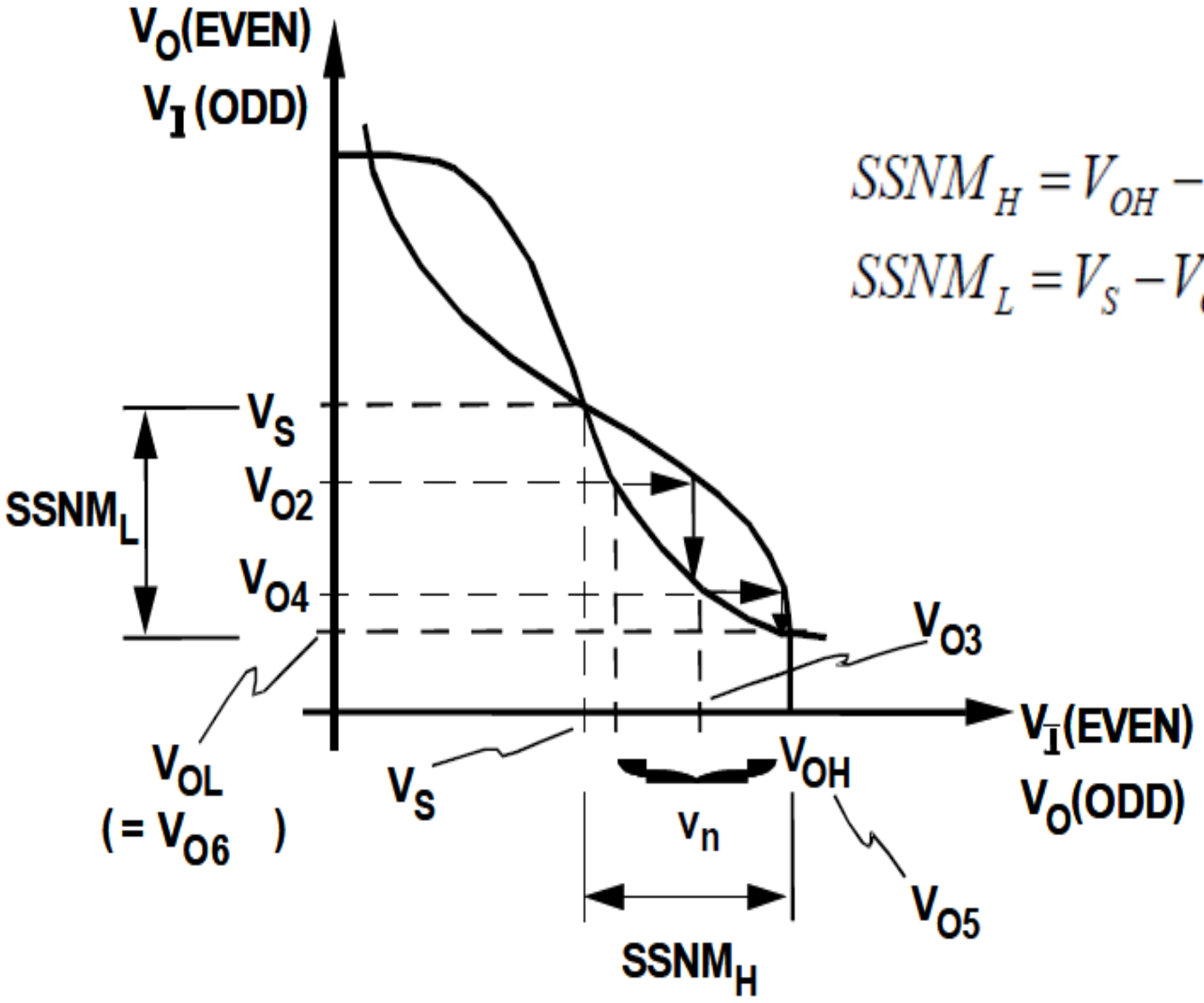
(a) Noiseless System



(b) System with Single Stage Noise of Magnitude v_n

Noise Margin (Cont'd)

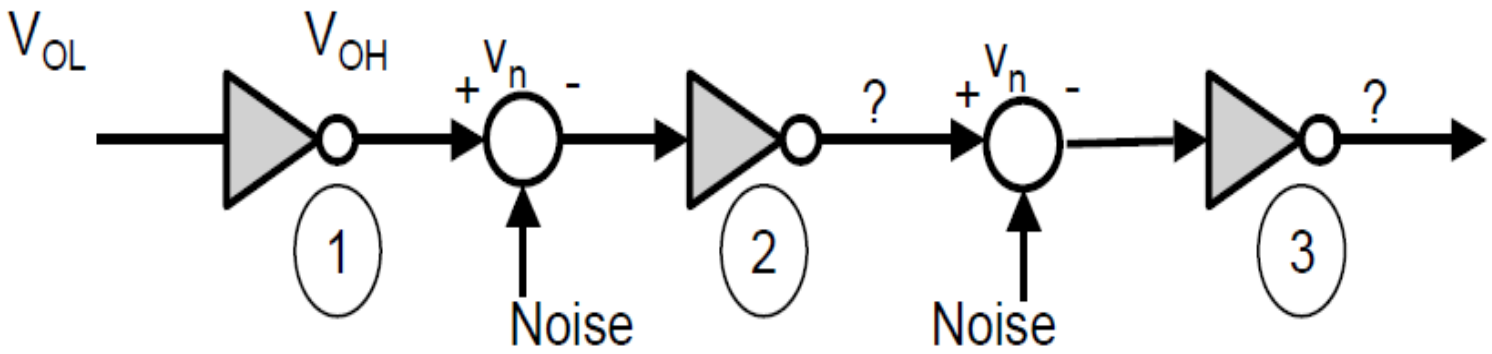




$$SSNM_H = V_{OH} - V_S$$

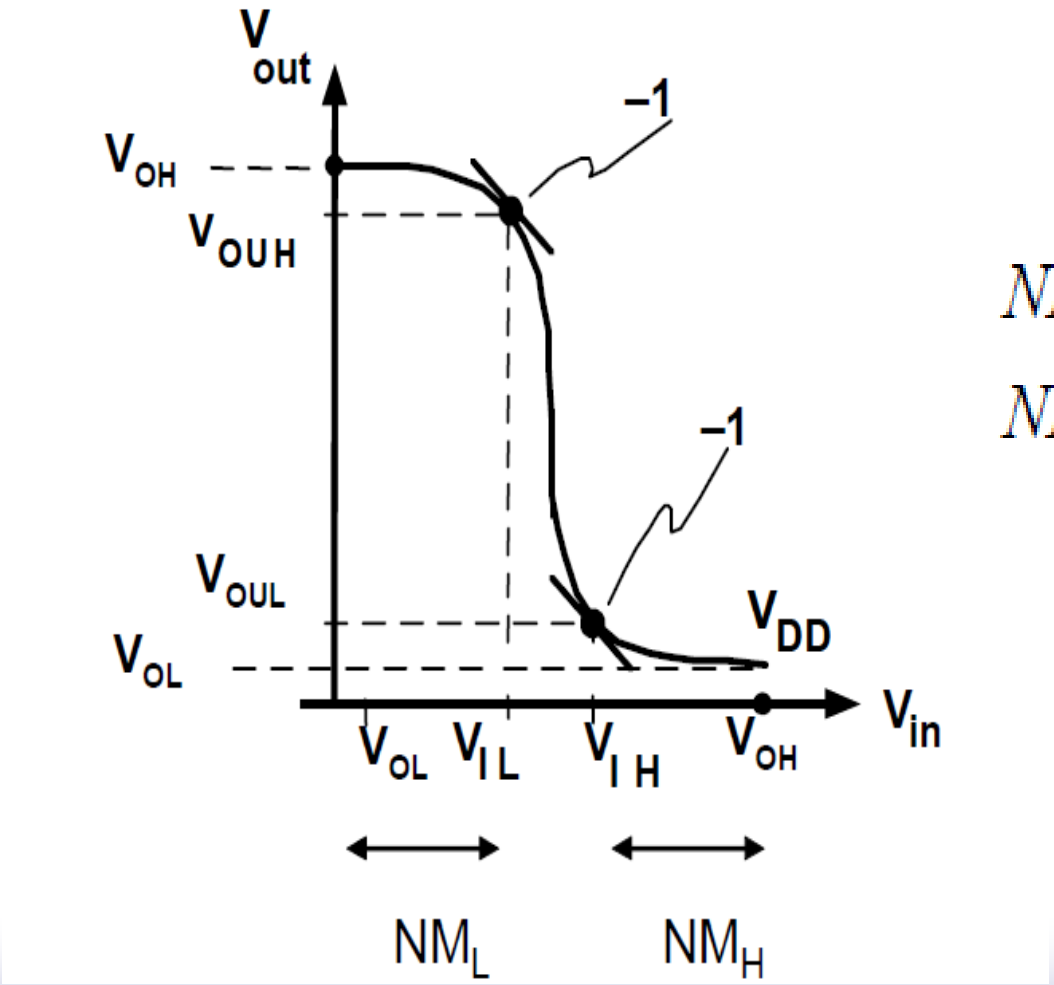
$$SSNM_L = V_S - V_{OL}$$

Multiple-Source Noise Margin (MSNM)



- *Follow board notes*

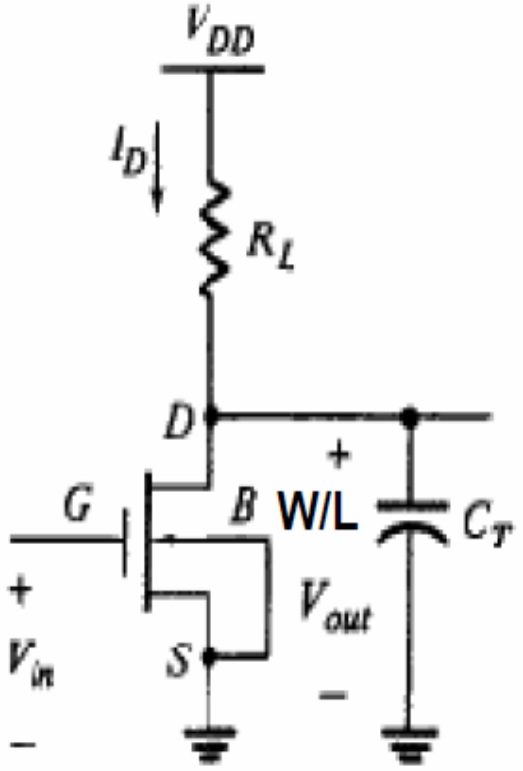
Multiple-Source Noise Margin (MSNM)



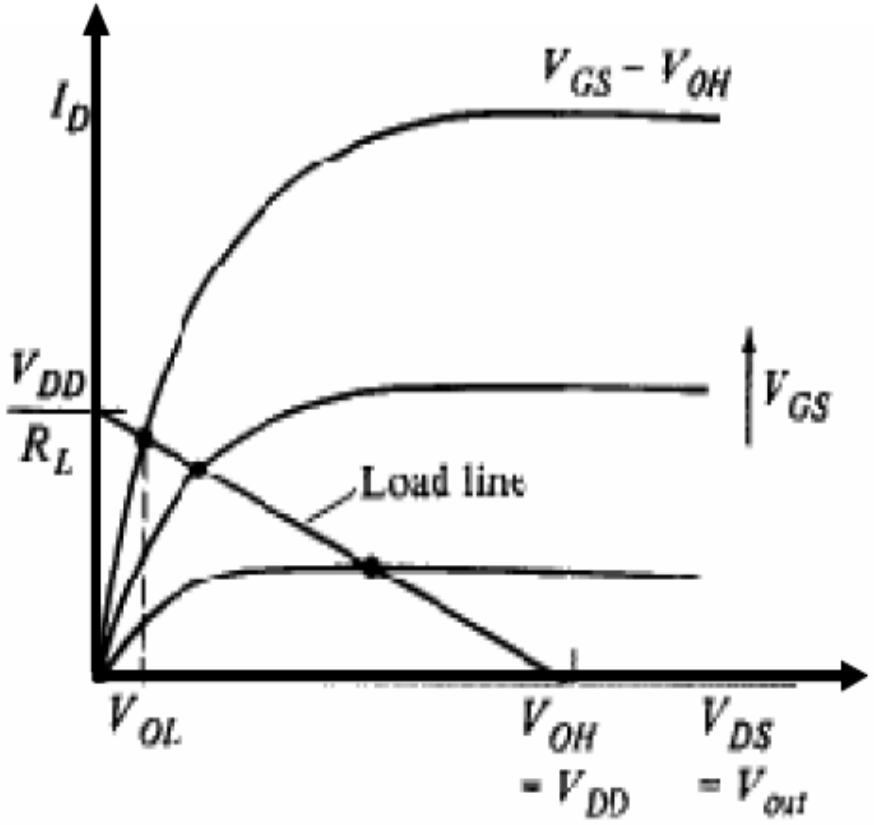
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

RESISTIVE-LOAD INVERTER DESIGN



(a) Inverter



(b) Drain characteristics and load line

VTC

- The value of V_{OH} can be obtained by setting the input voltage below the transistor threshold voltage V_T.
- No current flows and inverter output voltage V_{out} remains at V_{DD}. The nominal voltage representing a logic high level is $V_{OH} = V_{DD}$
- When a logic value of 1, represented by V_{OH}, applied at the input of this inverter, the transistor is driven into the linear region of operation
- Follow board notes

VTC (Cont'd)

- At $V_{in} = V_{IL}$, the output voltage is near V_{DD} and the transistor is operating in the saturation region.
- Follow board notes

VTC (Cont'd)

- At the other unity gain point, where $V_{in} = V_{IH}$, the output voltage is near 0 V and the transistor is operating in the linear region.
- Follow board notes

VTC (Cont'd)

- Switching threshold
- NMOS transistor is in saturation

$$\frac{W v_{sat} C_{ox} (V_S - V_T)^2}{(V_S - V_T) + E_C L} = \frac{V_{DD} - V_S}{R_L}$$