EE 466/586
VLSI Design

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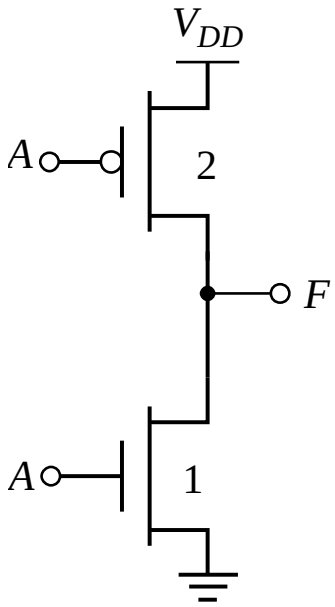
Lecture 7

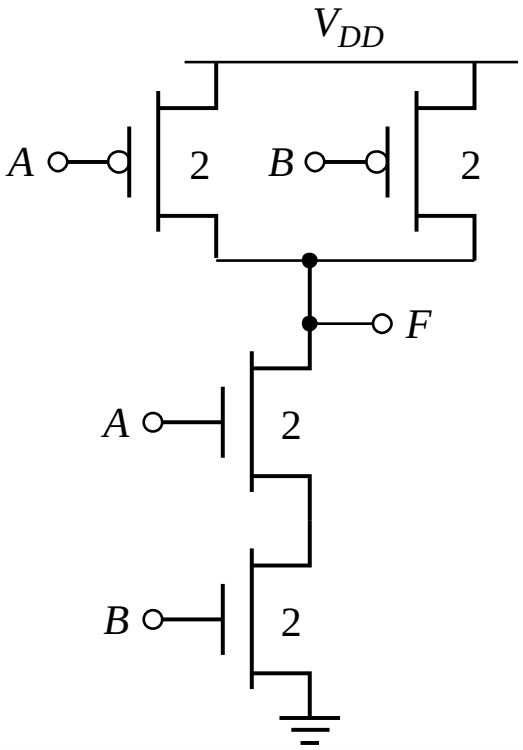
Static MOS Gate Circuits

CMOS Gate Sizing

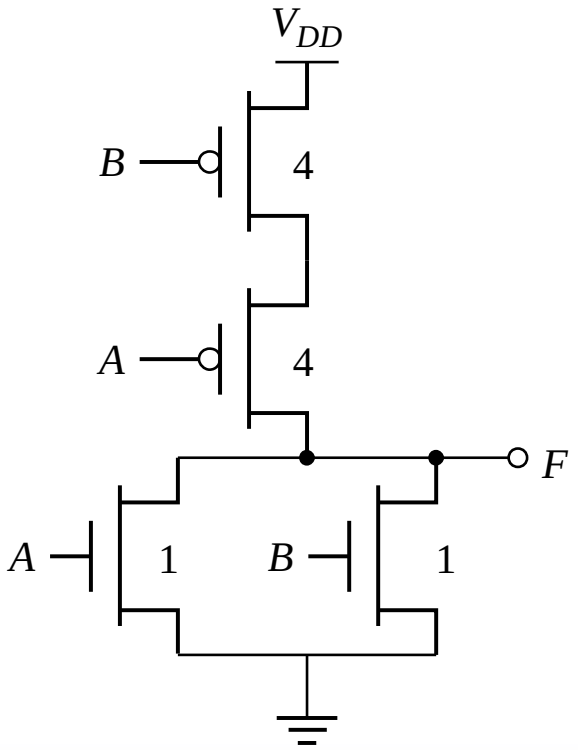
- NAND and NOR gate sizing
- Follow board notes



Inverter

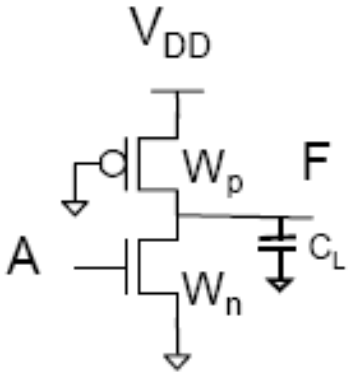


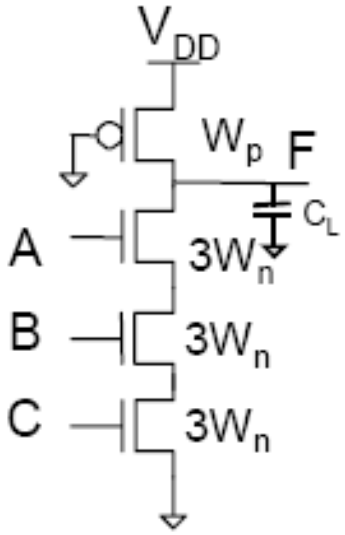
2-input NAND

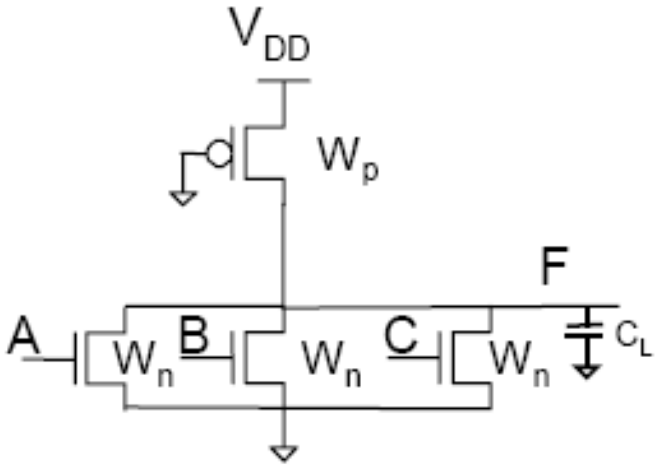


2-input NOR

Pseudo-NMOS Gate Sizing



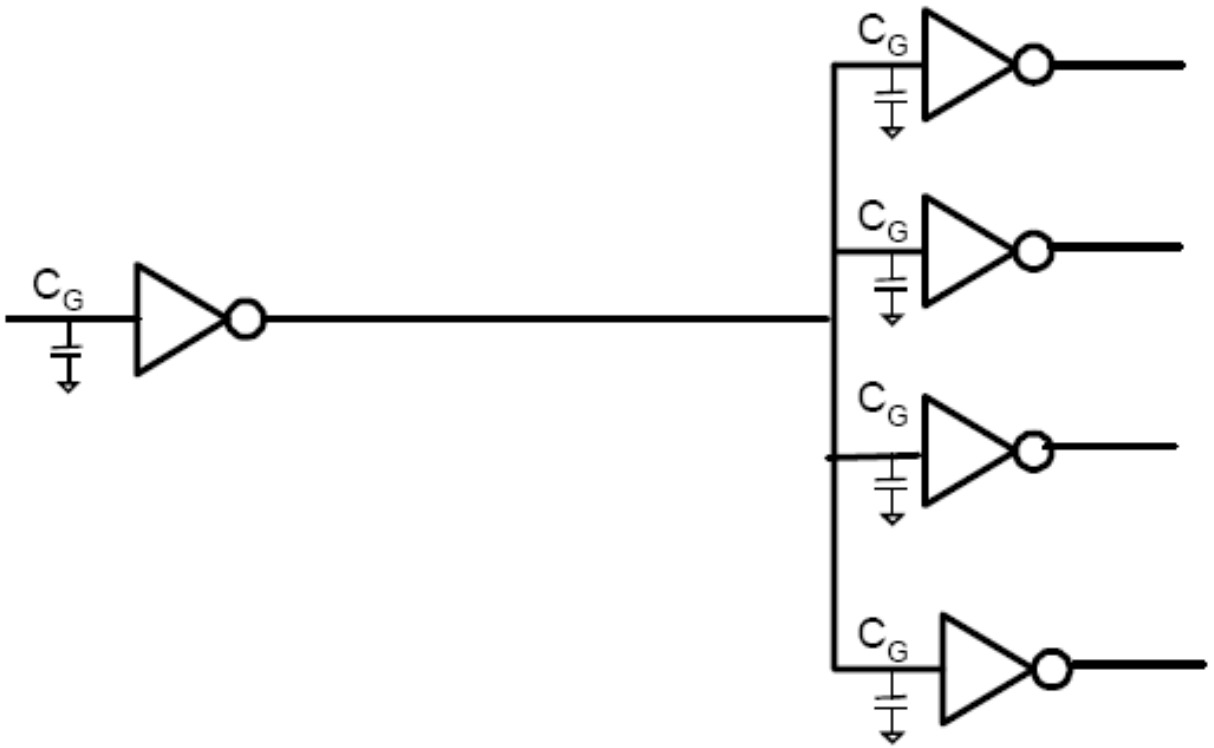




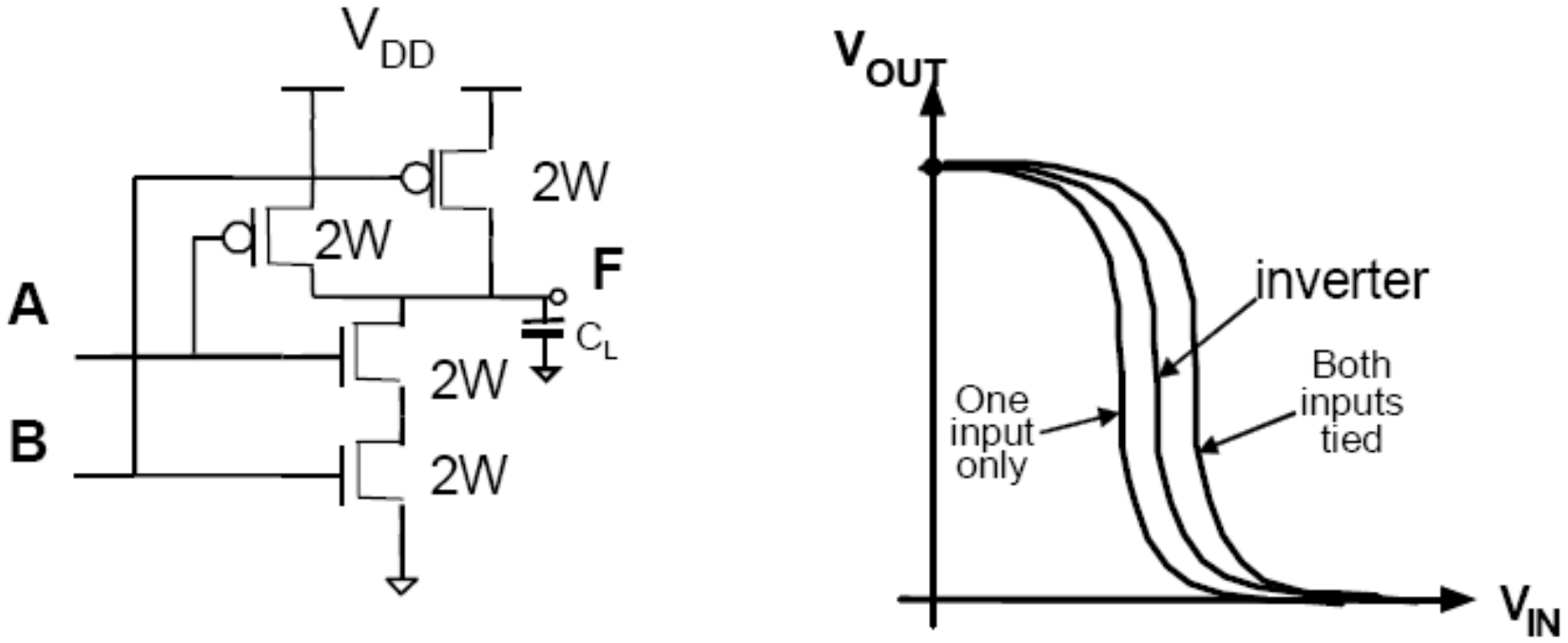
Fanin and Fanout Considerations

- Gates with a large number of inputs (high fan-in gates)
  - Too high resistance
  - Area penalty
- Follow board notes
- Fan Out
  - Output driving capability

Fan Out

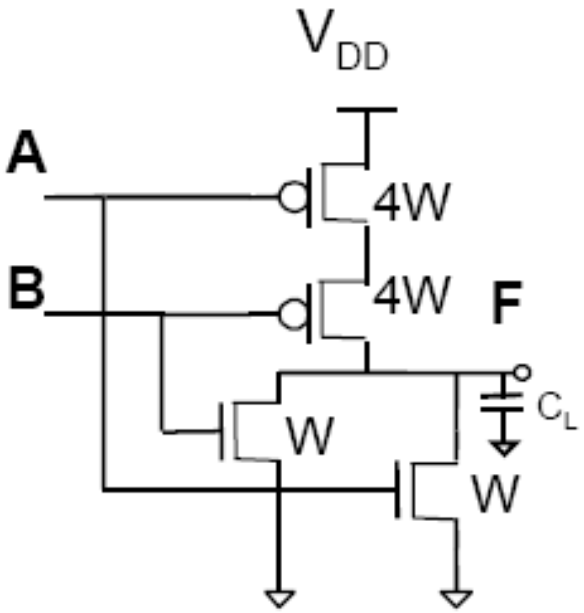


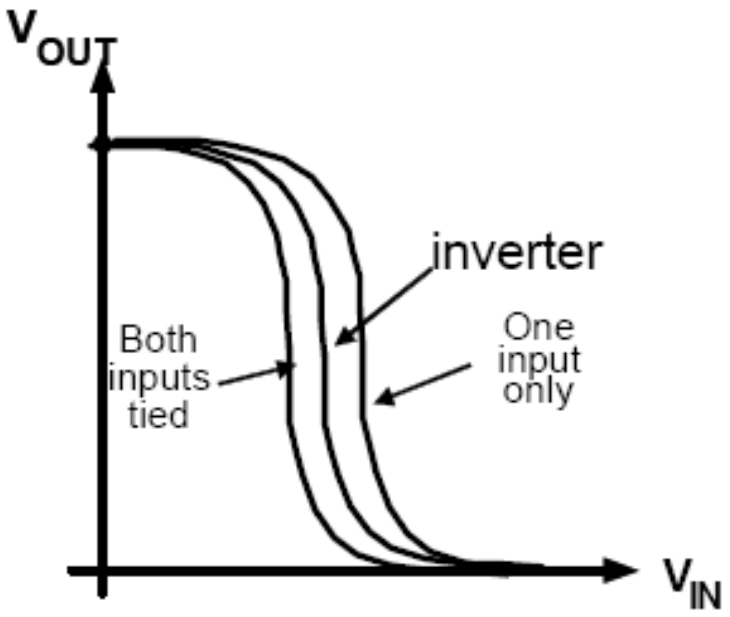
VTC of NAND Gates



- *If input A is held high while input B switched from low to high, the gate is equivalent to an inverter with a 2W pull-up device and a 2W pull-down device. The resulting transfer characteristic would shift to the left of the standard inverter.*

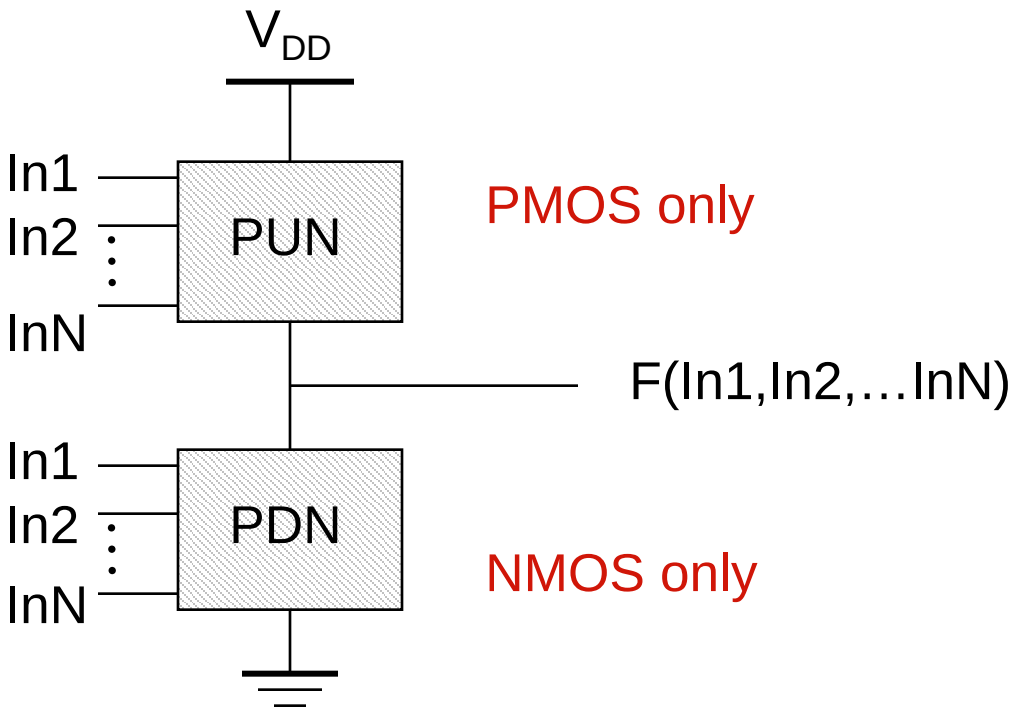
VTC of NOR Gates





Static Complementary CMOS

- The function of the PUN is to provide a connection between the output and Vdd anytime the output of the logic gate is meant to be 1
- Similarly the role of the PDN is to connect the output to GND when the output is meant to be 0

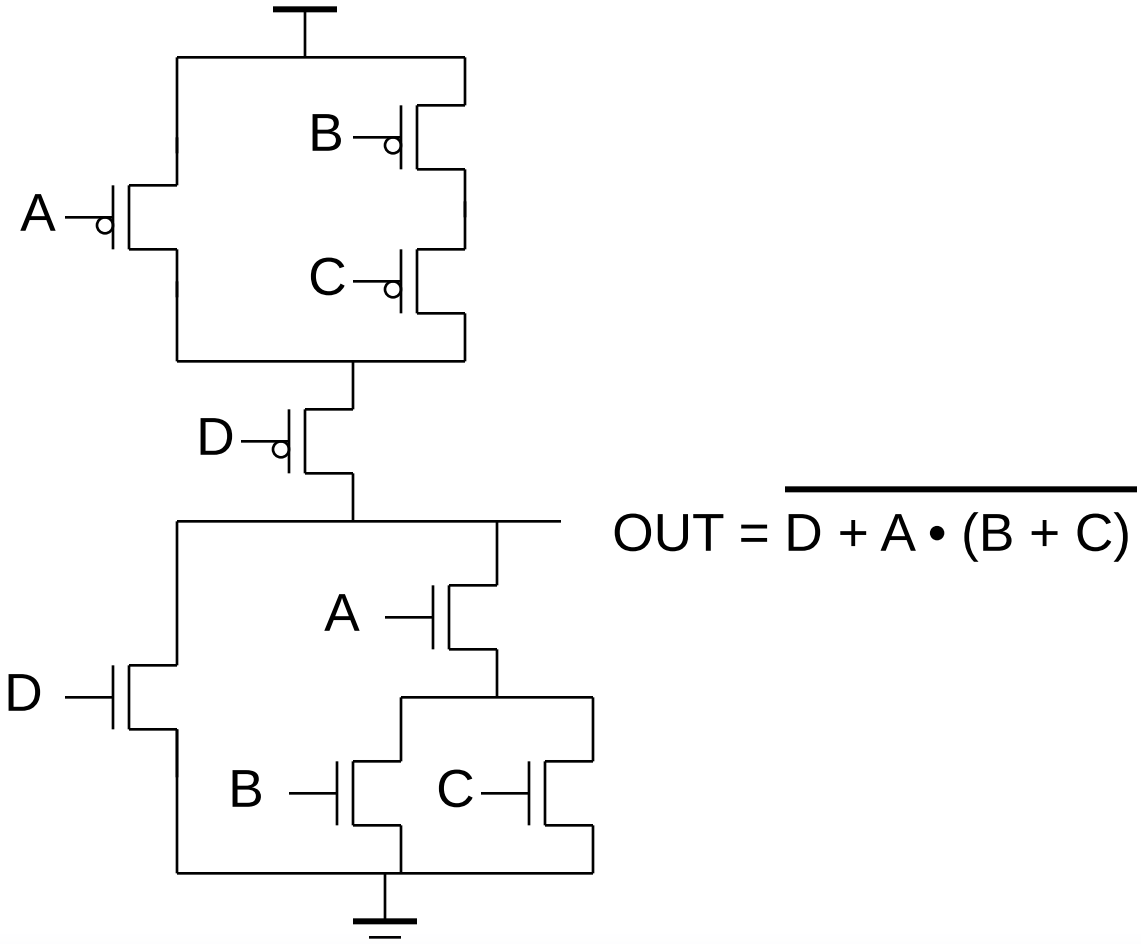


PUN and PDN are dual logic networks

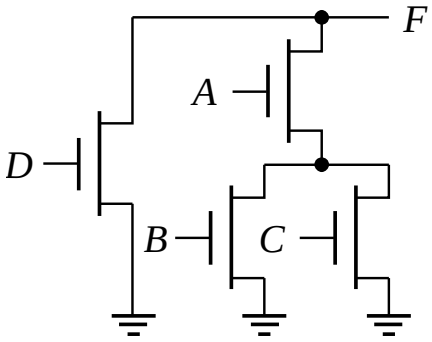
NMOS as PDN & PMOS as PUN

- NMOS device can pull the output all the way down to GND, but the PMOS device can pull it down to Vtp
- NMOS transmits a strong 0
- PMOS transmits a strong 1

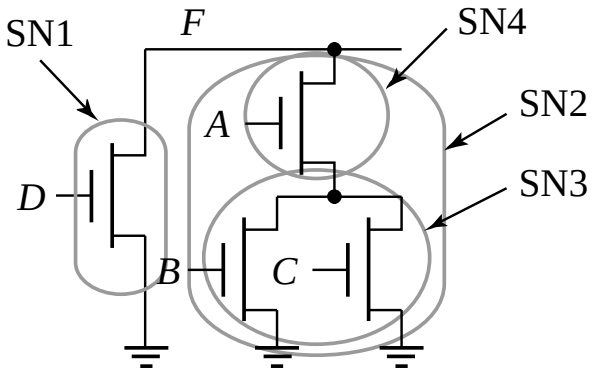
Complex CMOS Gate



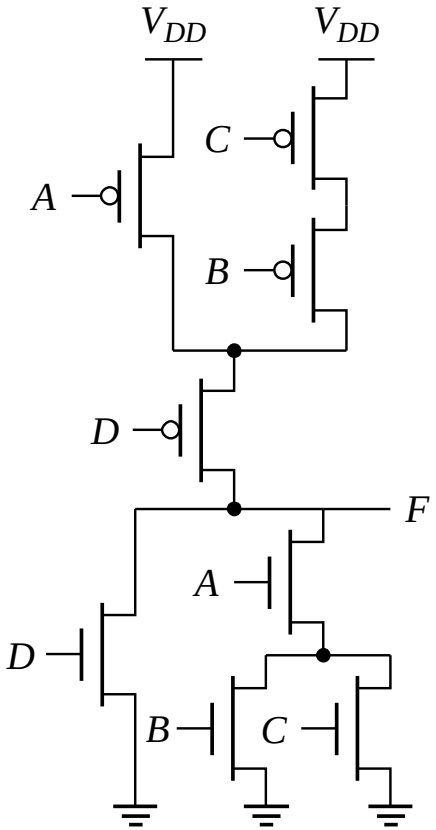
Constructing a Complex Gate



(a) pull-down network

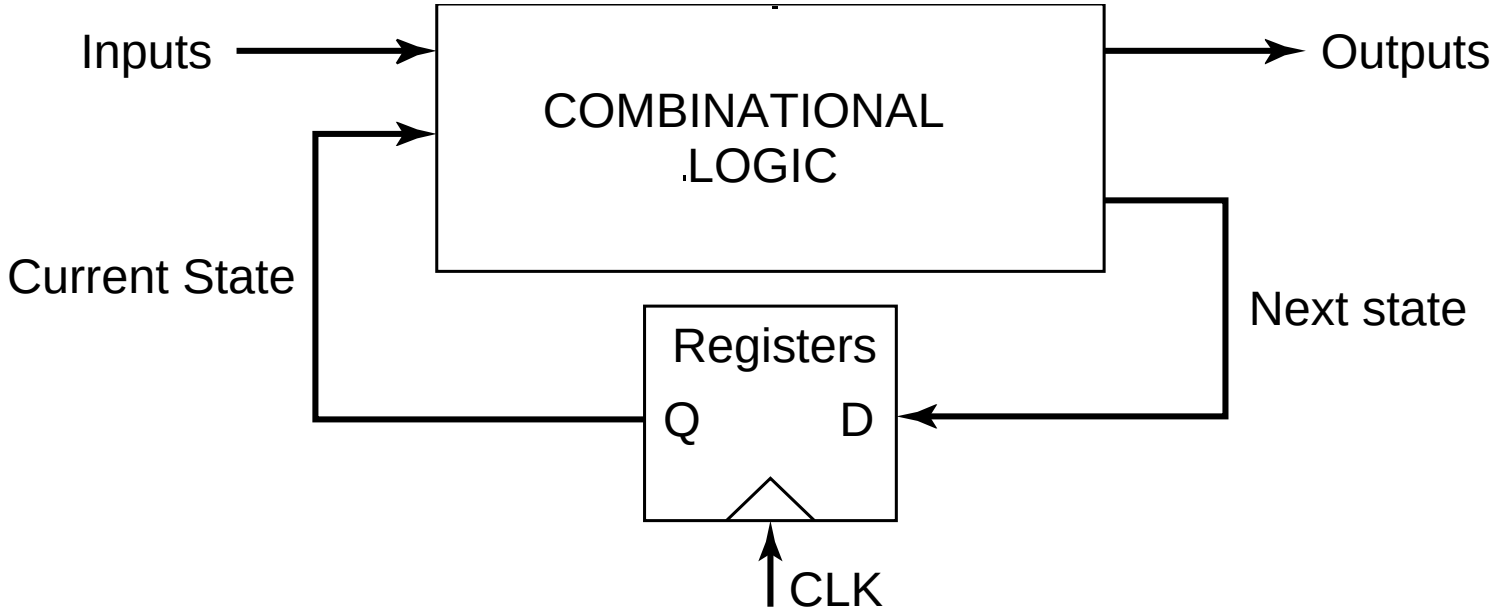


(b) Deriving the pull-up network hierarchically by identifying sub-nets



(c) complete gate

Sequential Logic



2 storage mechanisms

- **positive feedback**
- **charge-based**

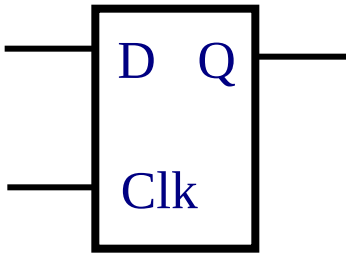
A latch is level sensitive

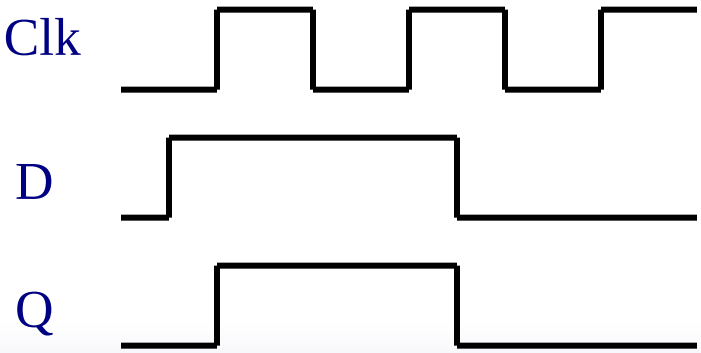
A register is edge-triggered

Latch versus Register

- Latch

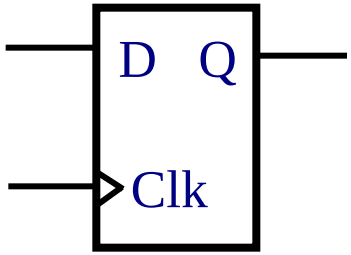
  Stores data depending on the level of the clock

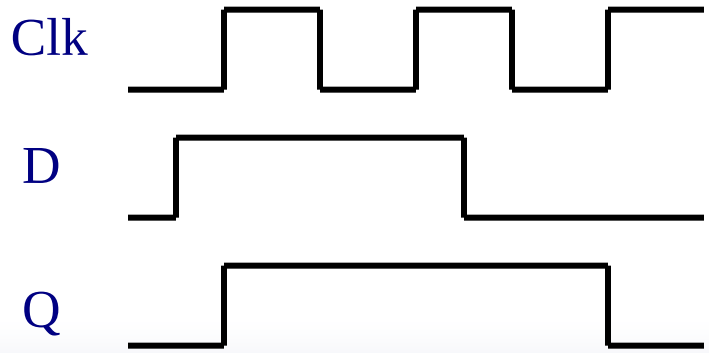




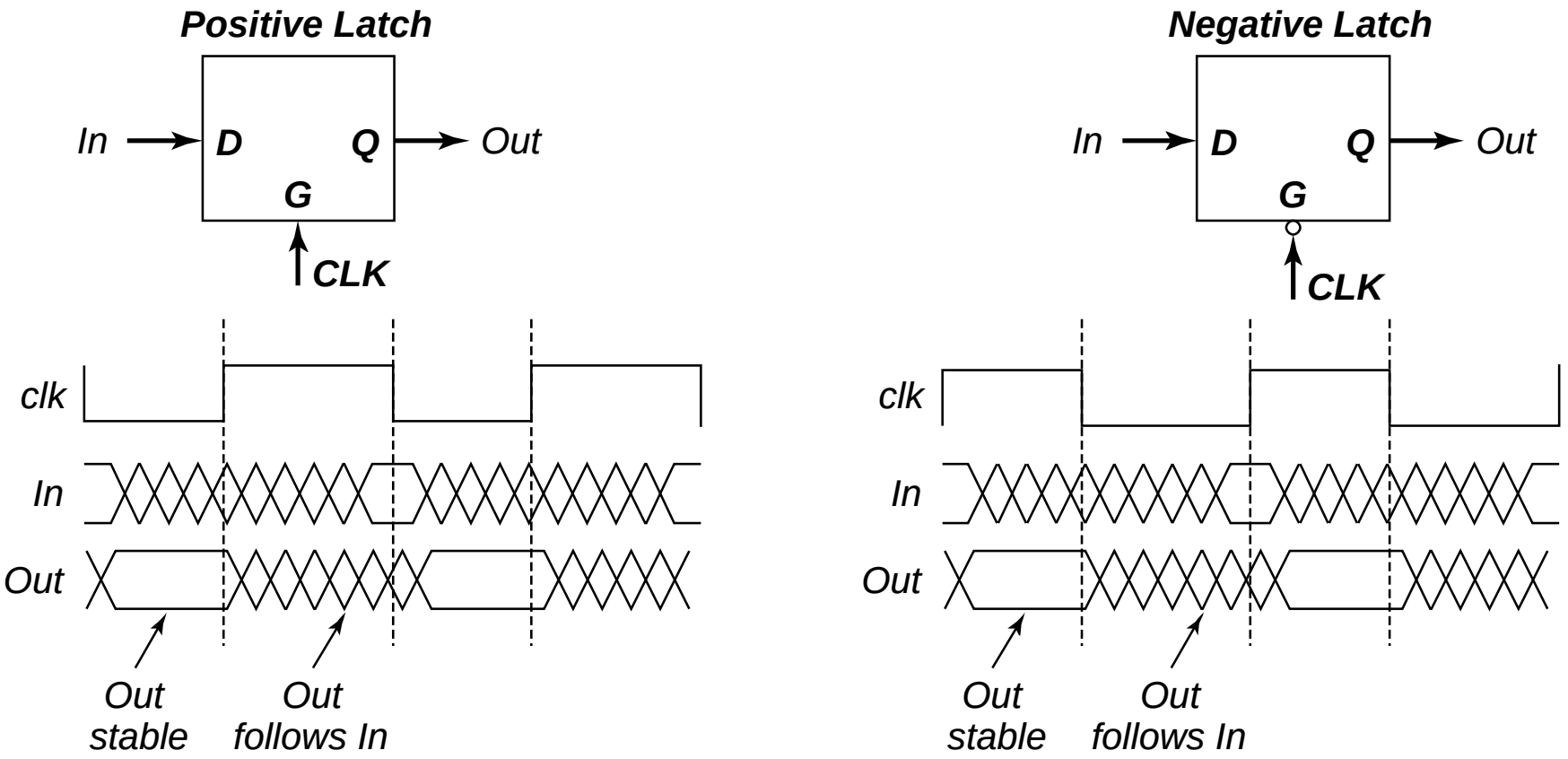
- Register

  stores data when clock rises





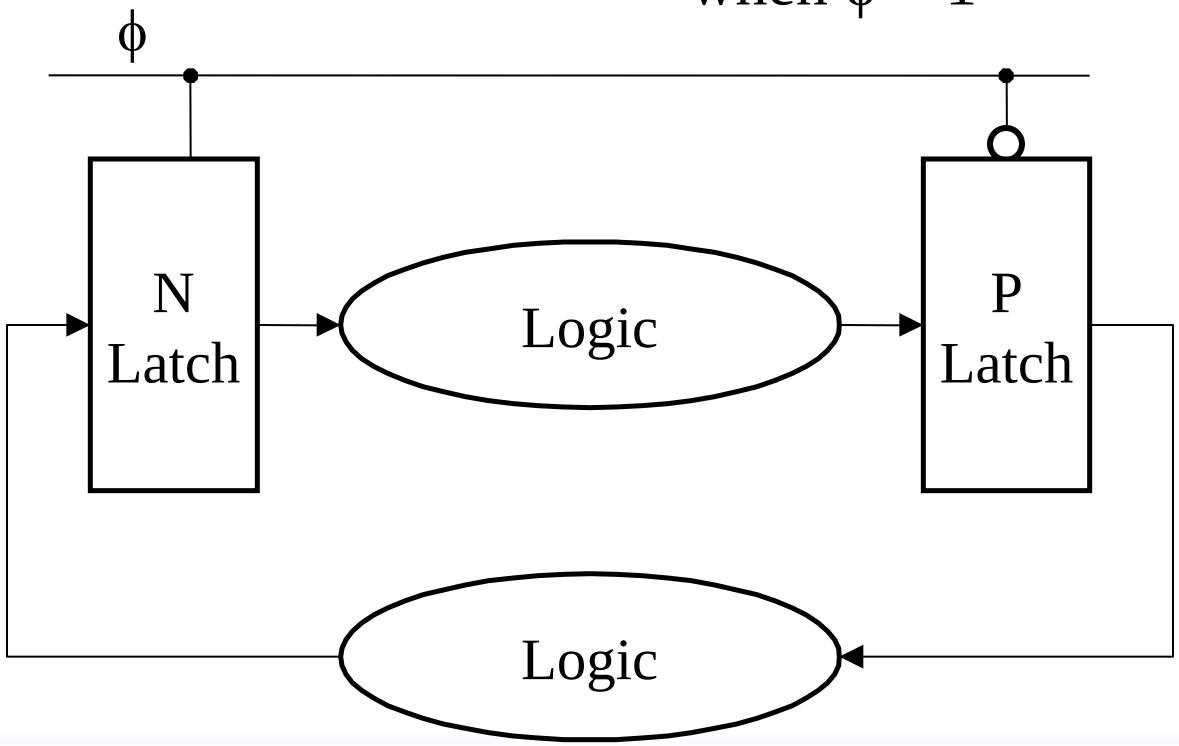
Latches


Positive Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In
Negative Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In

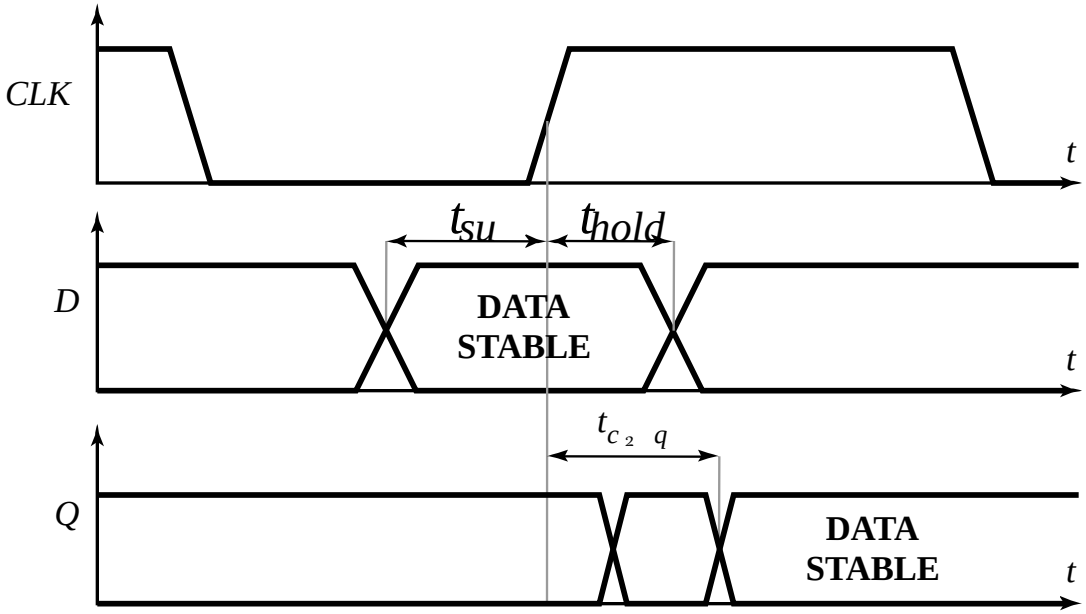
Latch-Based Design

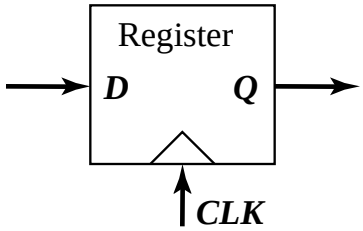
• N latch is transparent when $\phi = 0$

• P latch is transparent when $\phi = 1$



Timing Definitions

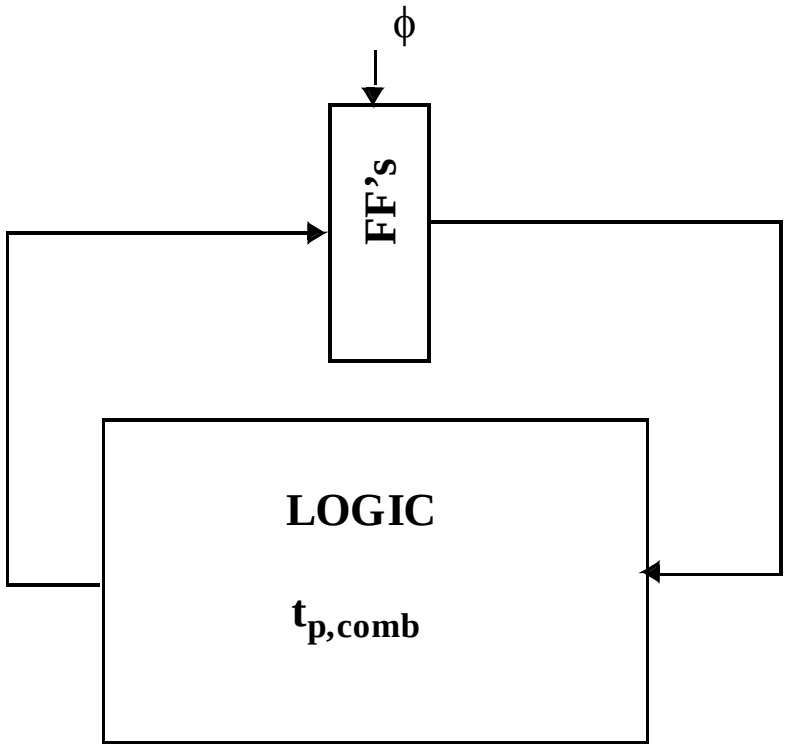




Timing Definitions

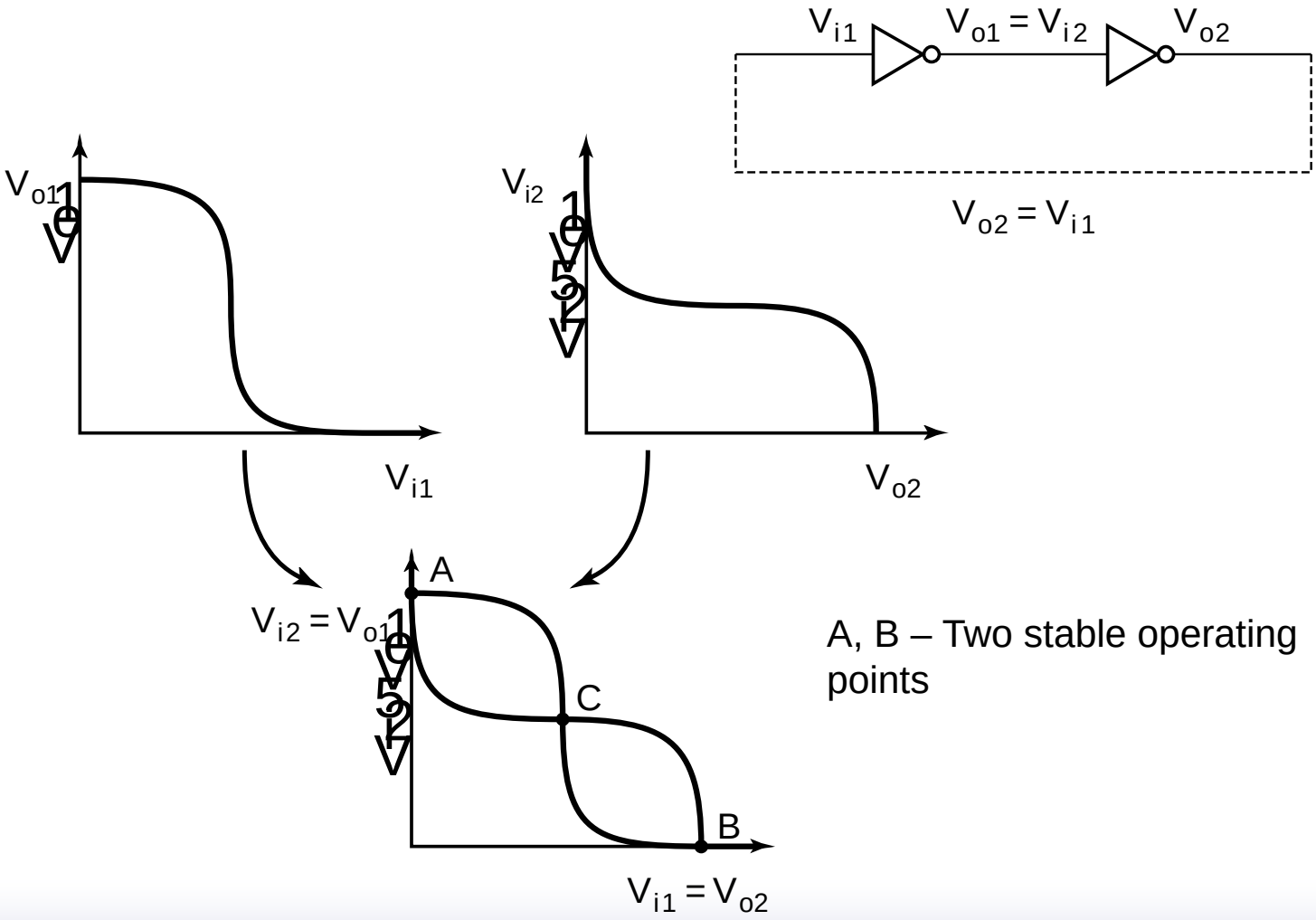
- T_{su} (Setup time)
  - Incoming data must be stable before the clock arrives
- T_{hold} (Hold time)
  - The length of time the data remains stable after the clock arrives for proper operation
- If the data is stable before the setup time and continues to be stable after the hold time, the register will properly capture the data
- $T_{clk\text{-}Q}$ (clk to Q delay)
  - This is the delay from the time the clock arrives to the point at which the Q output stabilizes

Maximum Clock Frequency



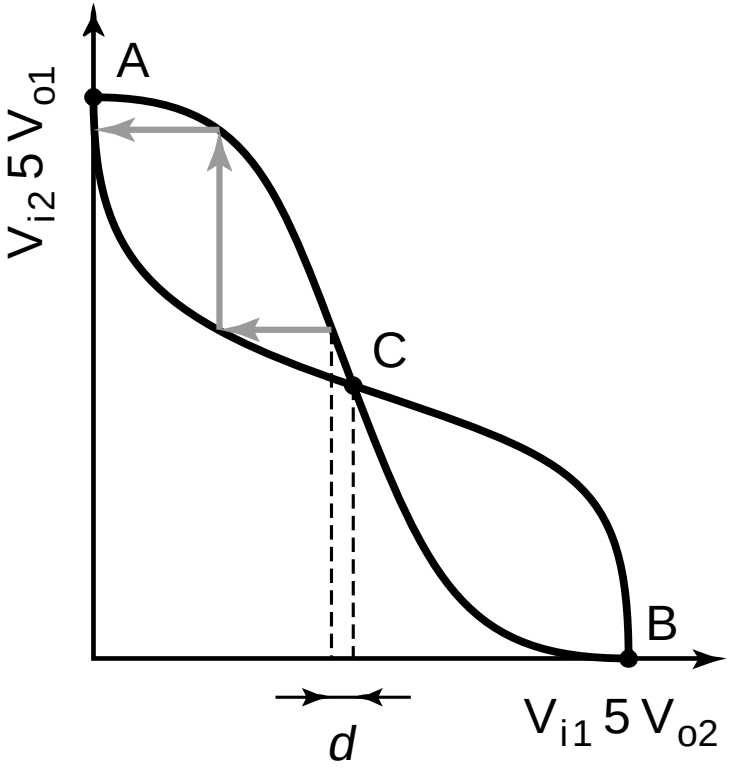
$$t_{clk\text{-}Q} + t_{p,comb} + t_{setup} = T$$

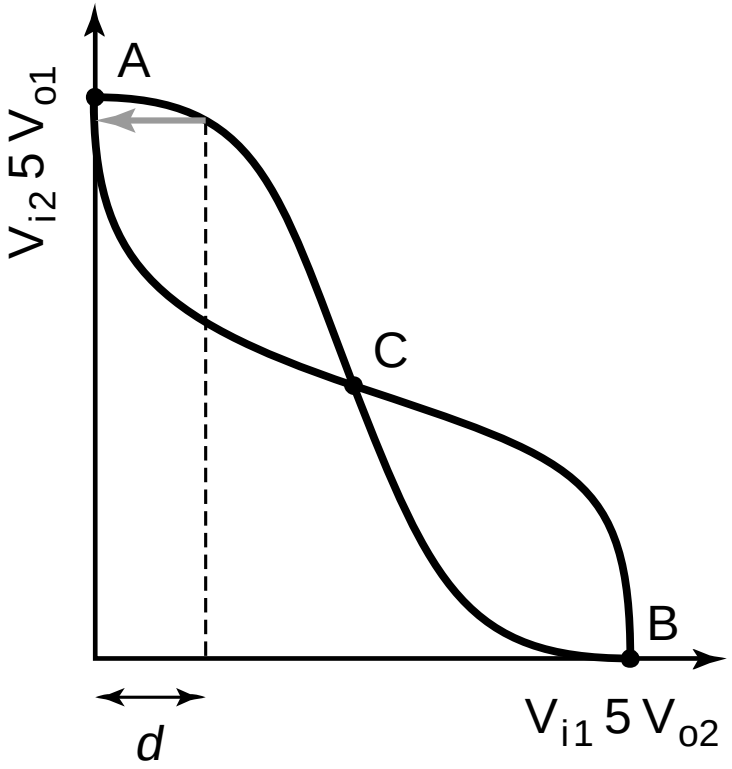
Positive Feedback: Bi-Stability



A, B – Two stable operating points

Meta-Stability

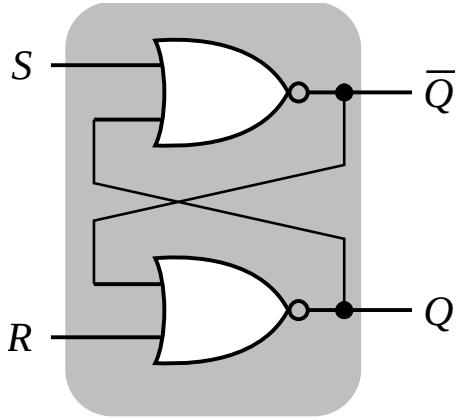


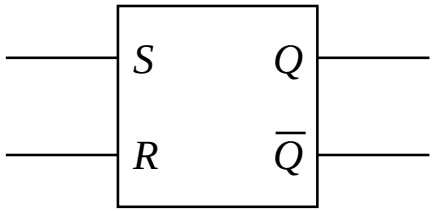


Gain should be larger than 1 in the transition region

Cross-Coupled Pairs

NOR-based set-reset



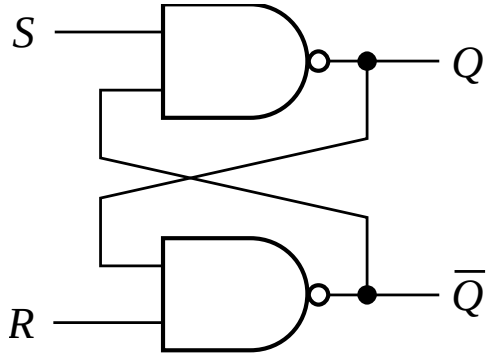


S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

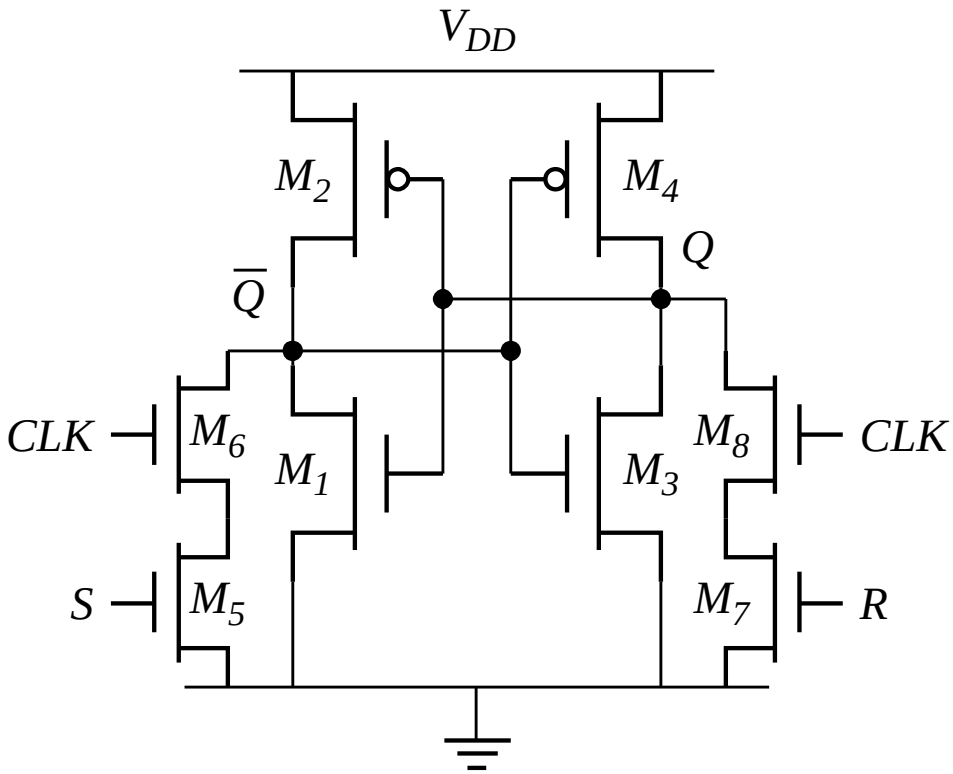
Forbidden State

Cross-Coupled NAND

Cross-coupled NANDs



Added clock



This is not used in datapaths any more, but is a basic building memory cell