EE 466/586
VLSI Design

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Lecture 10

Propagation delay (Cont'd)

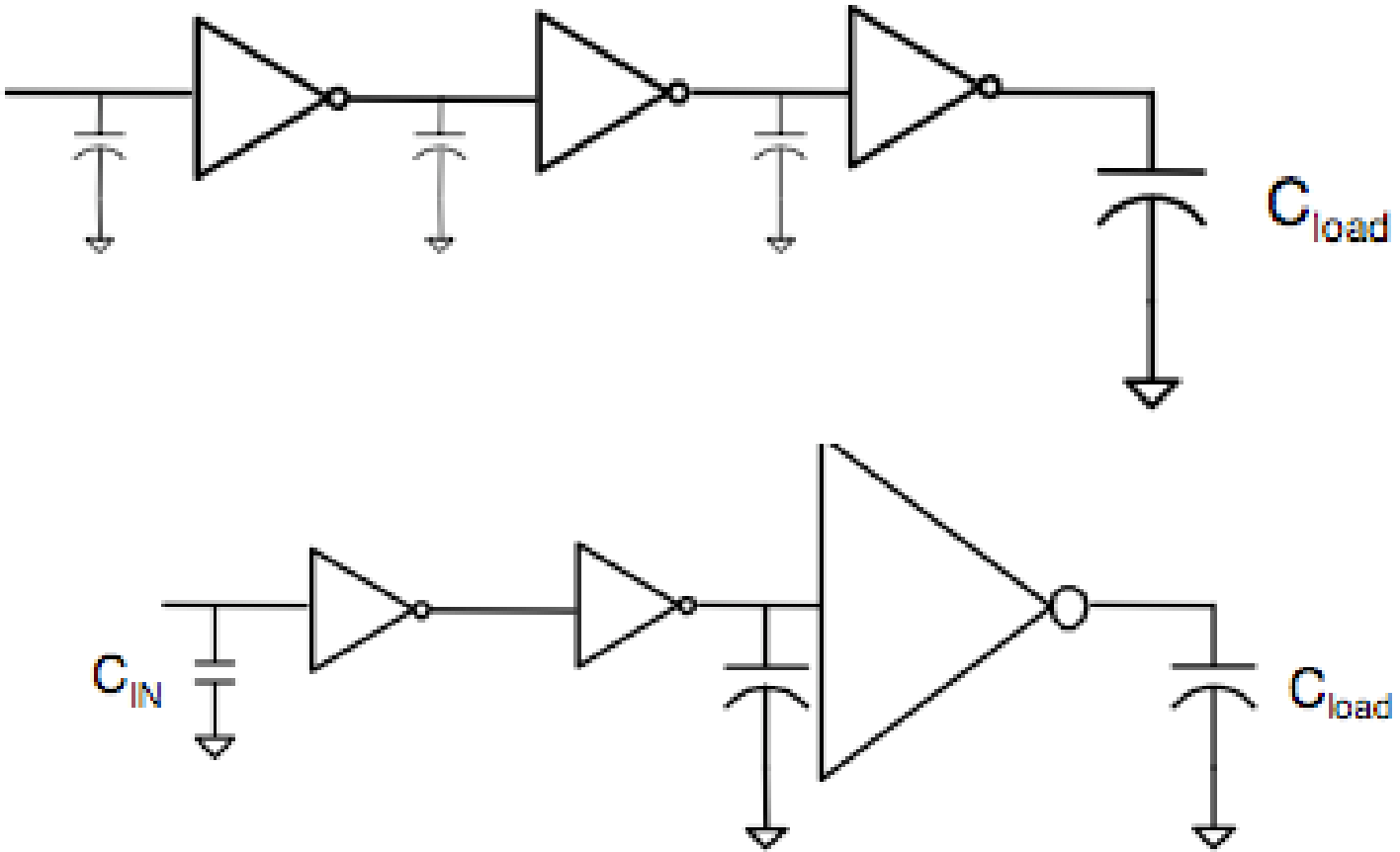
Driving large loads

- Sometimes, large loads must be driven:
  - off-chip;
  - long wires on-chip.
- Sizing up the driver transistors only pushes back the problem—driver now presents larger capacitance to earlier stage.

Sizing Logic Paths for Speed

- Frequently, input capacitance of a logic path is constrained
- Logic also has to drive some capacitance
- Example: ALU load in an Intel's microprocessor is 0.5pF
- How do we size the ALU datapath to achieve maximum speed?

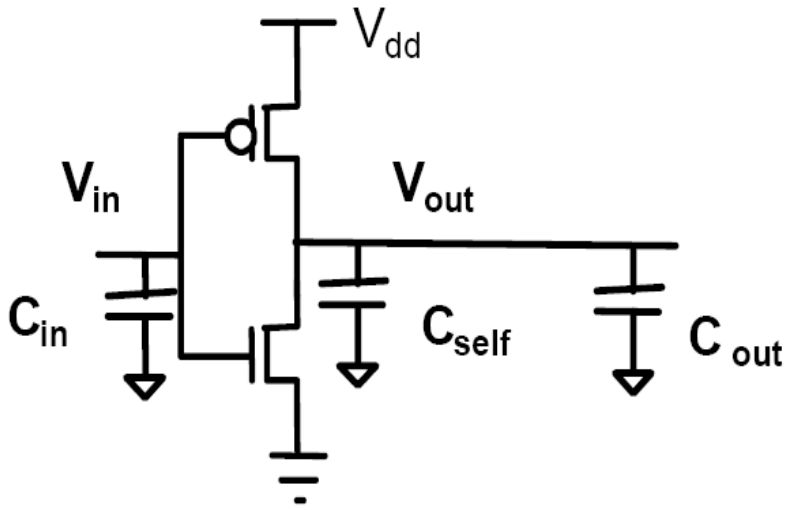
Gate Sizing for Optimal Path Delay



Inverter Characteristics

- Follow board notes

Delay of an Inverter



$$t_{delay} = R_{eff}\left[C_{out} + C_{self}\right]$$

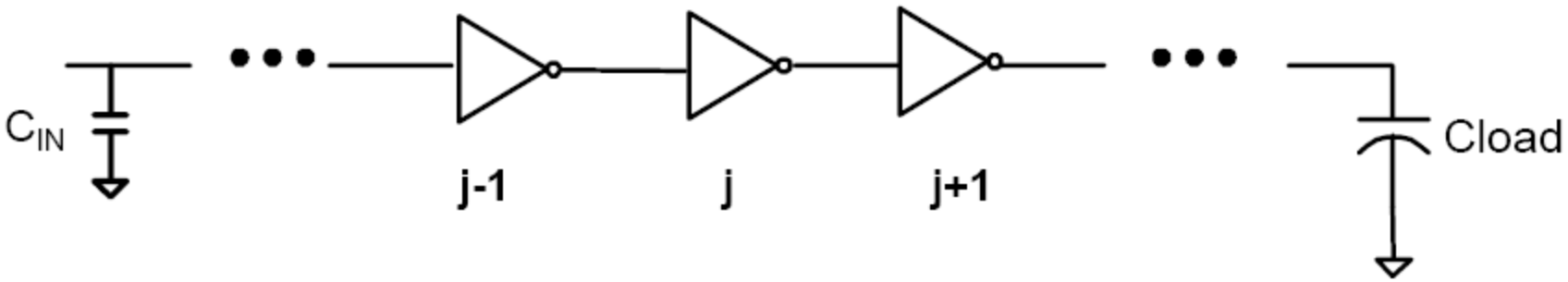
$$t_{delay} \approx R_{eff} C_{in}\left[\frac{C_{out}}{C_{in}} + \frac{C_{self}}{C_{in}}\right]$$

$$\approx \tau_{inv}\left[\frac{C_{out}}{C_{in}} + \gamma_{inv}\right]$$

where γ_{inv} is the ratio of self-capacitance to input capacitance for the inverter:

$$\gamma_{inv} = \frac{C_{self}}{C_{in}}$$

Delay of an inverter chain



$$total\_delay = \sum_{j=1}^{N} \tau_{inv} \left(\frac{C_{j+1}}{C_j} + \gamma_{inv} \right)$$

$$total\_delay = \sum_{j} \tau_{inv} \left(\frac{C_g W_{j+1}}{C_g W_j} + \gamma_{inv} \right) = \sum_{j} \tau_{inv} \left(\frac{W_{j+1}}{W_j} + \gamma_{inv} \right)$$

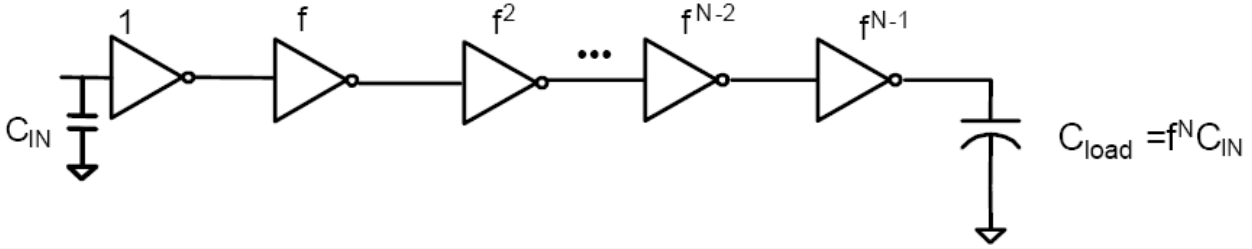
Scaling up of inverters

$$D_j = \tau_{inv}\left(\frac{W_j}{W_{j-1}} + \gamma_{inv}\right) + \tau_{inv}\left(\frac{W_{j+1}}{W_j} + \gamma_{inv}\right)$$

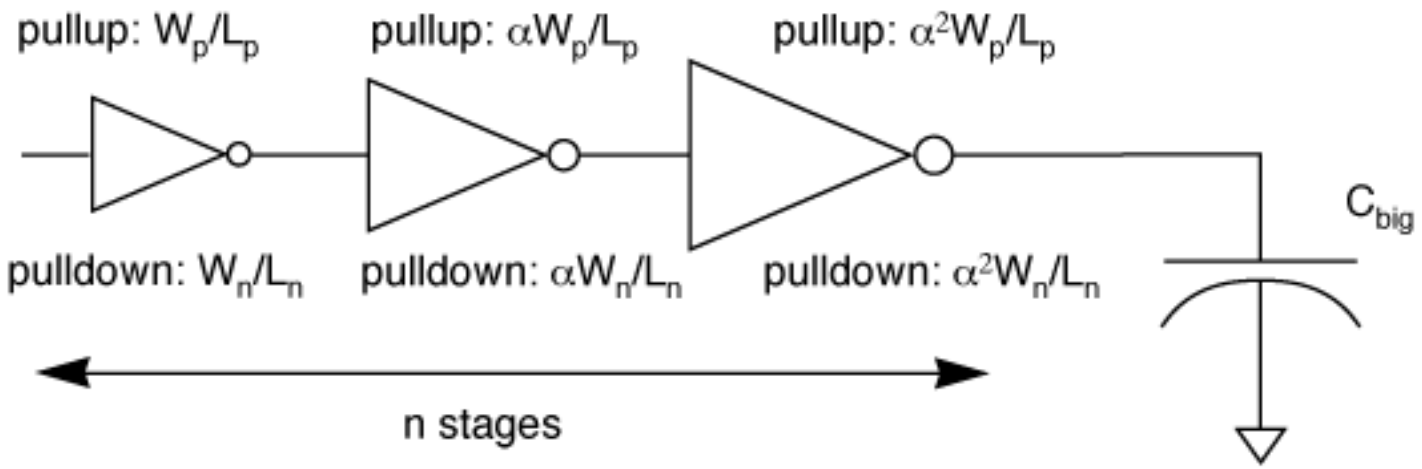
$$\frac{\partial D_j}{\partial W_j} = \tau_{inv}\frac{W_j}{W_{j-1}} - \tau_{inv}\frac{W_{j+1}}{W_j} = 0$$

$$\therefore \frac{W_j}{W_{j-1}} = \frac{W_{j+1}}{W_j}$$

$$\therefore W_j = \sqrt{W_{j+1}W_{j-1}}$$



Cascaded driver circuit



Optimum Delay

$$f^N C_{IN} = C_{load}$$

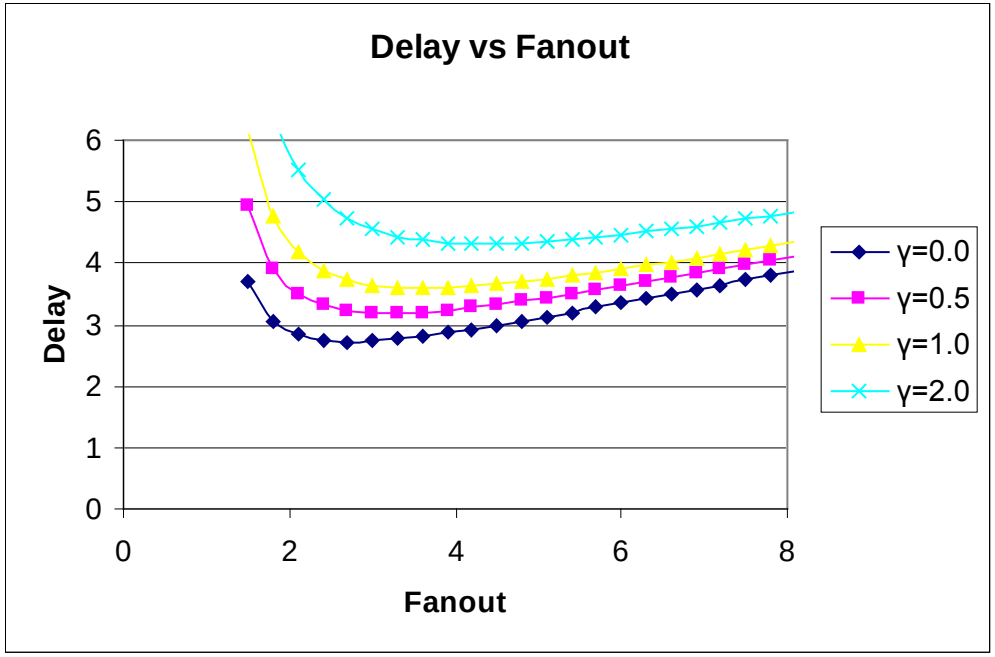
$$\therefore N = \frac{\ln\left(C_{load} / C_{IN}\right)}{\ln f}$$

$$gate\_delay = \tau_{inv}\left(\frac{C_j}{C_{j-1}} + \gamma_{inv}\right)$$

$$total\_delay = N \times \tau_{inv}\left(\frac{C_j}{C_{j-1}} + \gamma_{inv}\right)$$

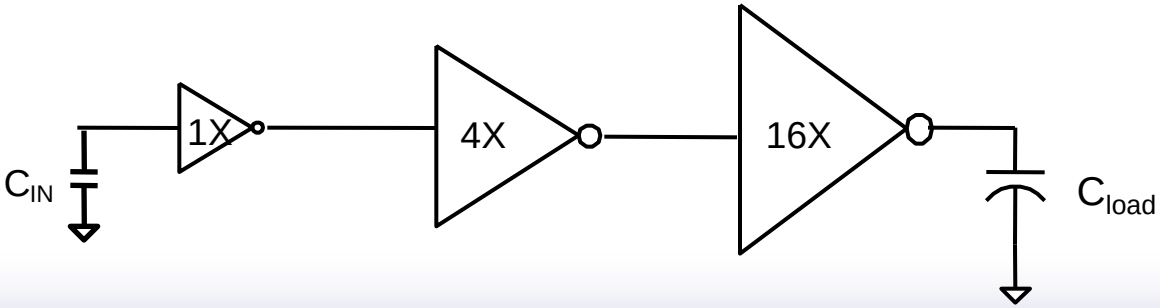
$$total\_delay = \frac{\ln\left(C_{load} / C_{IN}\right)}{\ln f} \times \tau_{inv}\left(f + \gamma_{inv}\right)$$

Optimal Sizing - FO4 Concept



where γ **is ratio of Parasitic output Capacitance to gate capacitance**

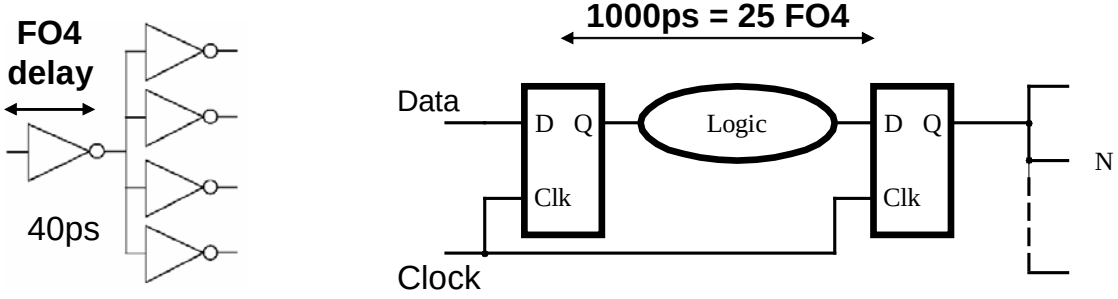
Use FO4 delay as optimal delay



Older Technology

- In older technologies, the optimal value of f was found to be e, the exponential value.
- Using the previous formulation, it is clear that this value is obtained when gamma=0 which implies that the junction capacitance is ignored.
- The junction capacitance and interconnect capacitance can act to increase the needed drive of the inverter.
- In a 0.13µm technology, gamma=0.5. Therefore, the use of f=3 or f=4 is more suitable in today's technology.

Clock cycle trend



(a) (b)