# EE 466/586
# VLSI Design

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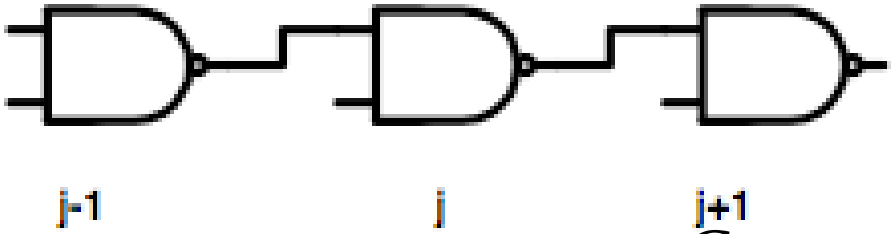
# *Lecture 11*

# *Propagation delay*

# Optimizing Paths with NANDs and NORs

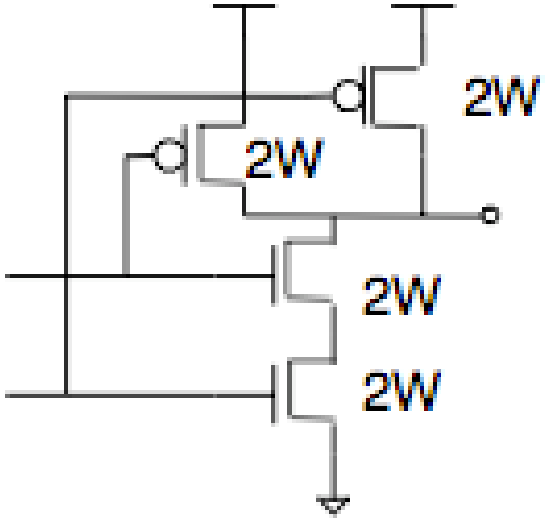


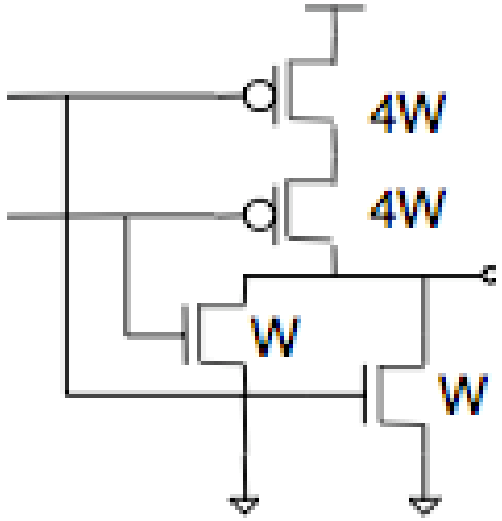

$$total\_delay = \sum \tau_{nand}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right)$$

- $\tau_{nand}$ *is the intrinsic time constant for the NAND gate*
- $\gamma_{NAND}$ *is the ratio of the self-capacitance to the input gate capacitance.*
- *For a chain of NOR gates*

$$total\_delay = \sum \tau_{nor}\left(\frac{C_{j+1}}{C_j} + \gamma_{nor}\right)$$

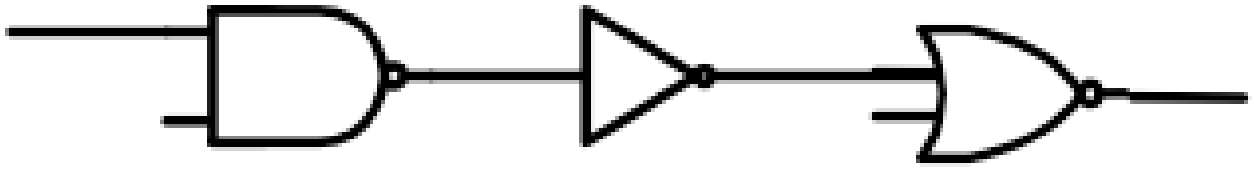
# Intrinsic Time constants




- *Follow board notes*

# Mixed Gates in a Logic path




$$total\_delay = \tau_{nand}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right) + \tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}} + \gamma_{inv}\right) + \tau_{nor}\left(\frac{C_{j+3}}{C_{j+2}} + \gamma_{nor}\right)$$

- *Optimization of Delay*
- *Follow board notes*

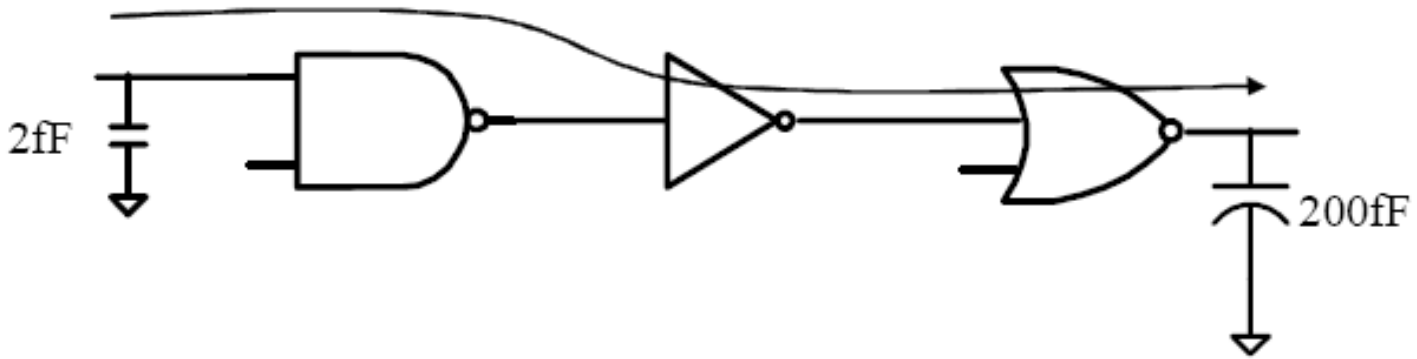
# Minimum Delay

$$\tau_{nand} FO_j = \tau_{inv} FO_{j+1}$$

- *The delay is minimized when the τ ×FO of a given gate is equal to τ ×FO of the next gate*
- *Fanout portions of the delays must be equal to reach the optimum solution.*
- *Follow board notes*

# Example

- Find the device sizes that optimizes the delay through the indicated path




- Follow board notes

# Logical Effort

- Logical Effort (LE) is the ratio of the intrinsic time constant for a gate to the intrinsic time constant of an inverter.

$$\frac{total\_delay}{\tau_{inv}} = \frac{\tau_{nand}}{\tau_{inv}}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right) + \frac{\tau_{inv}}{\tau_{inv}}\left(\frac{C_{j+2}}{C_{j+1}} + \gamma_{inv}\right) + \frac{\tau_{nor}}{\tau_{inv}}\left(\frac{C_{j+3}}{C_{j+2}} + \gamma_{nor}\right)$$

$$D = (LE_{nand}FO_1 + P_{nand}) + (LE_{inv}FO_2 + P_{inv}) + (LE_{nor}FO_3 + P_{nor})$$

$$D = \sum(LE \times FO + P)$$

- Follow board notes.

# Delay in a Logic Gate

**Gate delay:**

$$d = h + p$$

**effort delay** — **intrinsic delay**

**Effort delay:**

$$h = g\,f$$

**logical effort** — **effective fanout = $C_{out}/C_{in}$**

**Logical effort is a function of topology, independent of sizing**
**Effective fanout (electrical effort) is a function of load/gate size**

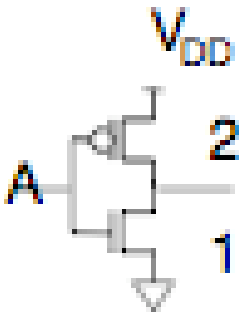
# Logical Effort

- Inverter has the smallest logical effort and intrinsic delay of all static CMOS gates
- Logical effort of a gate presents the ratio of its input capacitance to the inverter capacitance when sized to deliver the same current
- Logical effort increases with the gate complexity

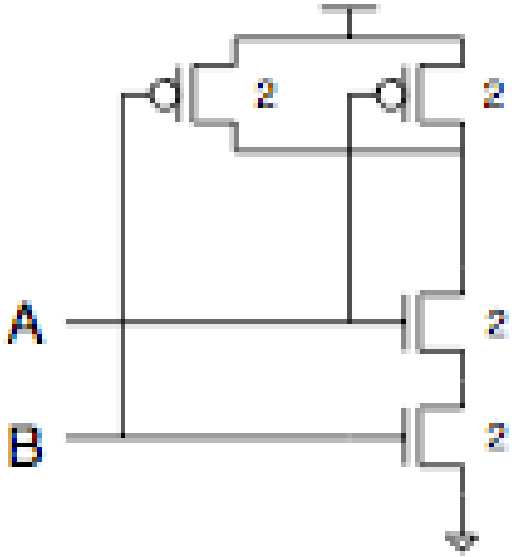
# LE Calculation

- Set the delays of the inverter and the gate to be the same; then, take the ratio of the input capacitances.
- Set the input capacitances to be same; then, take the delay ratio

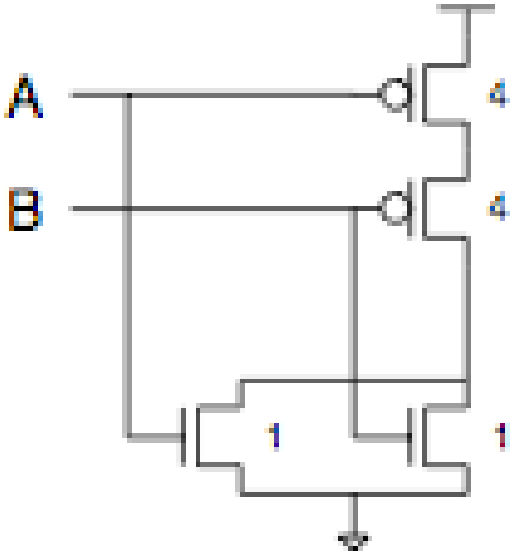
# Logical efforts for gates with equal delays




LE=1

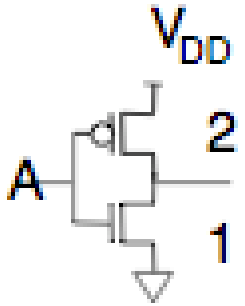



LE = 4/3

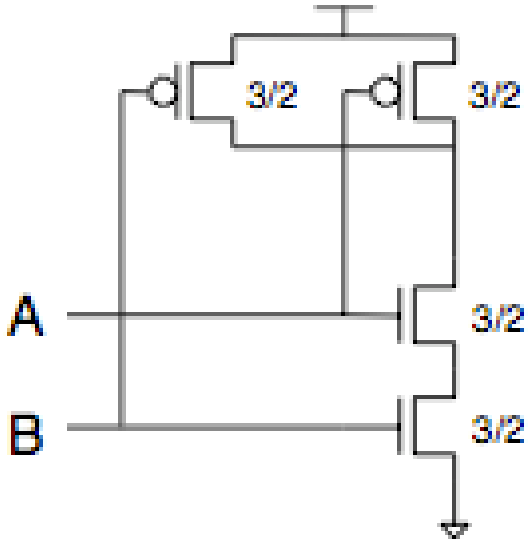



LE=5/3

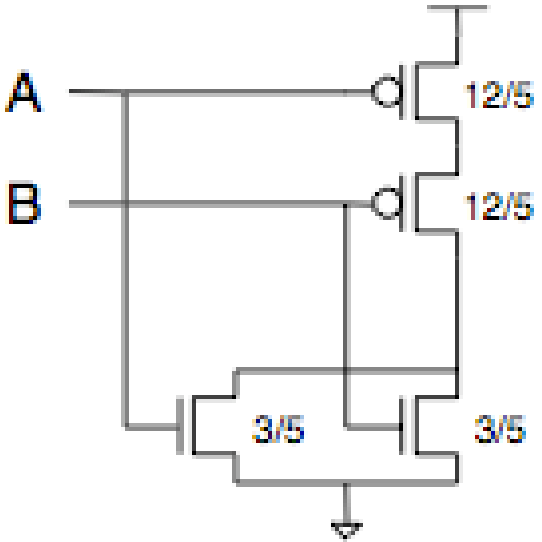
# Logical Effort Using Equal Input Capacitances




LE=1




LE = 4/3




LE=5/3

- *Why NAND is better?*

# LE of simple gates

| Type of Gate | 1 input | 2 inputs | 3 inputs | 4 inputs |
|---|---|---|---|---|
| Inverter | 1 | - | - | - |
| NAND | - | 4/3 | 5/3 | 6/3 |
| NOR | - | 5/3 | 7/3 | 9/3 |

# Computation of parasitics

| Type of Gate | 1 input | 2 inputs | 3 inputs | 4 inputs |
|---|---|---|---|---|
| Inverter | $P_{inv}=1/2$ | - | - | - |
| NAND | - | $2P_{inv}=1$ | $3P_{inv}=3/2$ | $4P_{inv}=2$ |
| NOR | - | $3P_{inv}=3/2$ | $4.5P_{inv}=9/4$ | $6P_{inv}=3$ |

- *Follow board notes*